The Handiman's Guide to

MOSFET "Switched Mode" Amplifiers

Part 2

Gate Input & Drive Requirements

(Or, Mosfets for the Obsessive Compulsive)

by Paul Harden, NA5N

Part 2 is for those with a desire to design and build Class D/E/F amplifiers. The following information, of a more technical nature than Part 1, may be found to be useful for understanding the gate input requirements and some driver circuits.

MOSFET Capacitances

Figure 10 Is a graphical representation of the capacitances in a switching MOSFET. An understanding of these capacitances is important for properly driving a class D/E/F PA. **Figure 11** shows the nominal values of these parameters for the IRF510.

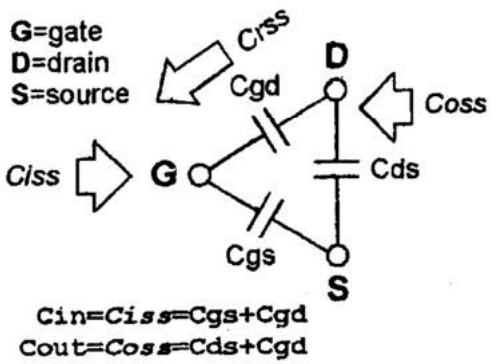


Fig. 10 – MOSFET Capacitances

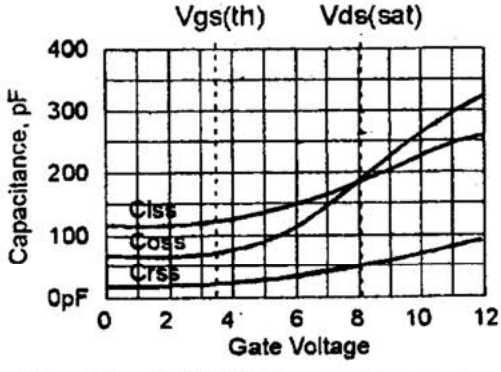


Fig. 11 – IRF510 Capacitances

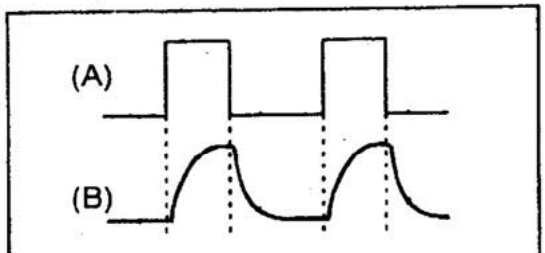


Fig. 12 – Effects of gate Ciss

Input Capacitance, *Ciss*, is the gate-source capacitance, *Cgs*, plus the reverse transfer capacitance, *Crss*. For the IRF510, *Ciss* is ~120pF when the device is OFF, increasing to ~180pFwhen the device is ON, due to the influence of *Crss* and the drop in drain voltage.

Applying a square wave to the gate, *Ciss* must charge before the voltage appears across the gate-source junction. This is illustrated in **Figure 12**, where (A) is the input square wave, and (B) is the true gate voltage, that is, the voltage impressed across the internal gate capacitance. The resulting drain current would appear virtually the same as waveform (B).

Once *Ciss* charges to Vgs(th), about 4v for the IRF510, drain current begins to flow and a portion of the output capacitance, *Coss*, is reflected back to the gate in the form of the reverse capacitance parameter, *Crss*. This

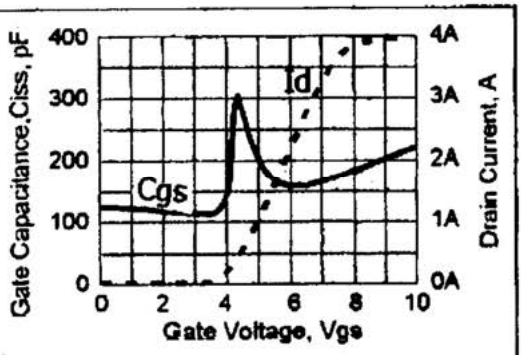


Fig. 13 – gate voltage vs. Ciss and Drain Current (Id)

(and other factors) causes a sudden increase in the gate capacitance at Vgs(th). This is illustrated in **Figure 13**, with Vgs(th) at 4.0v. The graph is derived from the data sheets, application notes, and measurements I have made on the IRF510.

This rather complex input capacitance graph is not shown in **Fig. 11**, as most data sheets show only the *average* capacitance over the gate or drain voltage range, not the aberration that occurs when drain current first begins to flow. This is important to realize, as it alters the actual gate voltage waveform one will observe on an oscilloscope when driving with a square wave.

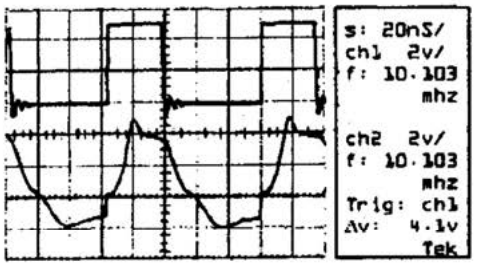


Fig. 14 – Gate Input Waveforms

Figure 14 is an oscilloscope display showing the waveforms one can expect. The gate waveform serves as a great diagnostic tool in evaluating your class D/E/F transmitter.

I drive the mosfet with a low-Z emitter follower. The top trace (Ch.1) shows the input to the emitter follower, a fairly pure square wave at 10.103 MHz on a 30M transmitter. The bottom trace (Ch.2) is the gate waveform. The gate is biased at 3vdc, such that the TTL square wave drives the gate from about 3v, below Vgs(th), to a little more than 8v for saturation. When the square wave goes from LO to HI, the gate voltage immediate rises to 4.2v, where it hesitates – a visual indication of the actual gate threshold voltage, Vgs(th) for this device. This is the point where drain current begins to flow. The slower slope between Vgs(th) and 8v is due to the increased *Ciss* above Vgs(th) on **Fig. 11**. This is also the area of maximum gain of the device. The desired flattening out of the gate drive at 8v indicates the mosfet is in saturation, although this is confirmed by monitoring the drain voltage, as discussed later.

When the gate drive goes from HI to LO, gate voltage returns to the 3v bias level rather sluggishly, due to *Ciss* discharging. Note that at Vgs(th), the falling waveform again changes it's slope – due to *Ciss* being altered by the gate junction storage charge effect when gate voltage falls below Vgs(th).

Gate Driver Considerations

Of importance in class D/E/F is the time to reach Vgs(th), the gate threshold voltage, after application of the gate drive going HI. This is described by:

$$t = \frac{Ciss \times Vgs(th)}{Ig}$$

Solving for gate current, Ig:

$$Ig = \frac{Ciss \times Vgs(th)}{t}$$

The above equation indicates that the higher the gate current, provided by the driver stage, the faster *Ciss* will charge, and the higher the efficiency of the PA.

For class D/E/F, the point of the square wave drive is to get through the linear region as soon as possible. This

means *Ciss* should be charged as quickly as possible.

I recommend striving for 15–20nS. See **Figure 15**. This is also consistent with the ~16nS rise time, tr, of the IRF510. "Tr" is theoretically the fastest *Ciss* can be charged.

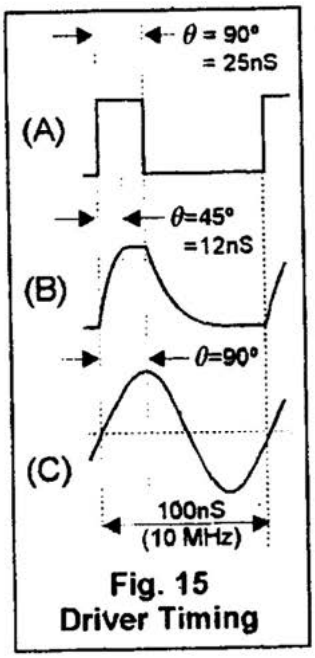


Fig. 15
Driver Timing

The figure shows the input gate drive (A) being a 25% duty cycle, or 90° of the RF cycle. At 10.1 MHz, the gate drive "pulse" would be about 25nS, and to charge *Ciss* two times faster would indicate 12nS, as shown in (B). From the previous equation, this would indicate a gate current of 50mA is required. This is a bit high for QRP!

I have found a driving current of 25-30mA to be a nice compromise to charge *Ciss* sufficiently fast for high efficiency. Referring to **Fig. 15 (B)**, if the gate waveform does not flatten out at the 8v level (looks more like a sine wave), the driver is not providing sufficient current to the gate. Driving the gate voltage to saturation quickly, by providing sufficient gate drive current, *is paramount in achieving the high efficiency of class D/E/F.* The 25mA of drive current will save 200mA or more of PA current at 5W QRP. Observing the o-scope drive waveform in **Fig. 14**, note that *Ciss* charges in 18-20nS at 10.1 MHz This 30M transmitter has an overall efficiency of 82%, which *includes* the 40mA of key-down current due to the TX mixer, comparator and emitter follower driver providing the gate current. This same 18-20nS Ciss charge time will cause a lower efficiency on 20M, as it's approaching the period of the RF. At 40/80M, this 18-20nS rise time will produce higher efficiencies, since it is a smaller percentage of the RF cycle at lower frequencies..

Also note that the input gate square wave in **Fig. 14** is about a 30% duty cycle – 30% ON and 70% OFF. The output power from the class D/E/F PA is determined by the duty cycle. With the IRF510, a 15% duty cycle produces about 1W output; about 5W at 30%, and 8W at 45%. Efficiency begins to drop above 45% duty cycle.

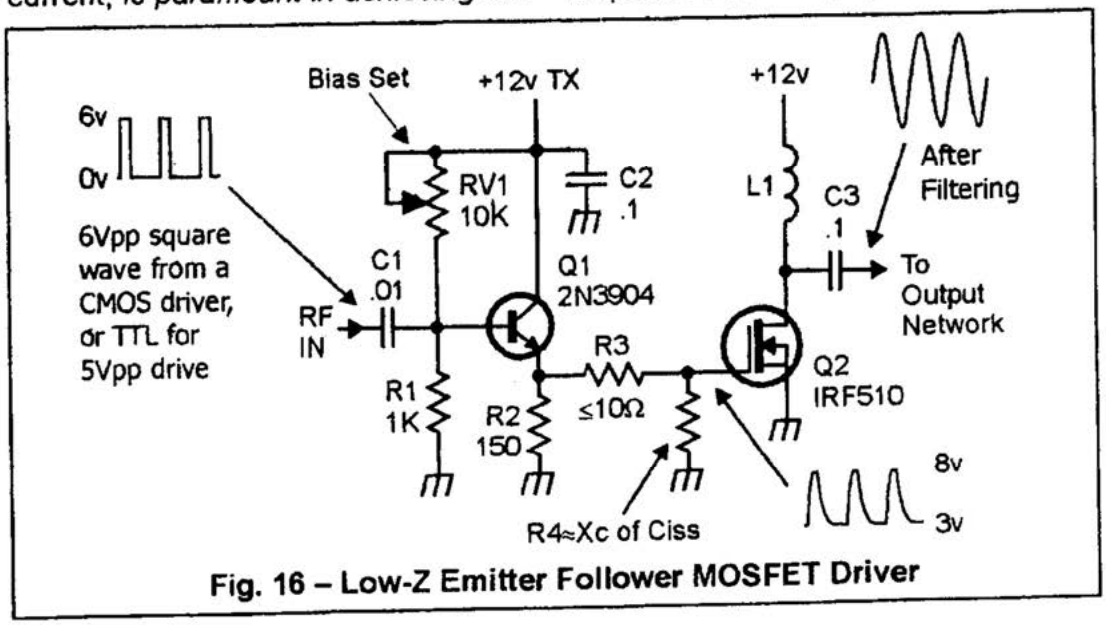


Fig. 16 – Low-Z Emitter Follower MOSFET Driver

25mA Emitter Follower Driver

The square wave drive can be developed by some type of CMOS or TTL gate. These alone do not have the current sinking capabilities needed to properly drive the IRF510. Some type of current booster, plus the ability to shift the dc level of the input square wave is required. The emitter follower circuit in **Figure 16** is one approach. This works best if you provide a 6V square wave to Q1, such as from a 6–8v CMOS gate, rather than 5V TTL. This is due to the 0.7v drop in the emitter follower, leaving only about 4V from a TTL drive. This may not drive the IRF510 into saturation.

The input square wave is dc shifted by C1 (dc blocking) and the RV1–R1 bias network. Adjust RV1, by monitoring the gate on an oscilloscope, as follows: when the input square wave is LO, the voltage on Q2 gate should be about 3v; when the input goes to +6v HI, the gate voltage should be between 8–9v, depending upon the loading to the circuit. This 3–8v output is developed across R2 and R4. The 3v level is to ensure the IRF510 is OFF, <Vgs(th), and 8v for saturated ON.

Q1 is powered from the +12v TX term to shut down the driver in receive, in the event RV1 is misadjusted to cause mosfet drain current to flow when the mosfet should be OFF.

R3 is 3.9–10Ω to de-Q the gate and prevent VHF oscillations. The value is not critical. R4 is a resistive load to both the Q1 emitter follower and Q2 gate. The value should be about the Xc of the mosfet *Ciss*, ~120–180pF, or a few hundred ohms, depending upon the transmit frequency. Initially, you can make R4 a trim pot and adjust for the best possible square wave (**Fig. 14**) to match to the *Ciss* of the IRF510. This value will vary from device-to-device.

If the rise time is slower than 25-30nS, then more gate current is needed by decreasing the value of R2. In this example, if a 3v-to-8v signal is formed across R2, then the output drive current would be about 33mA on the drive peaks. (I=5V/150Ω). Ohms law is thus used to determine R2 for the drive current desired.

In the technical literature, the following equation is used to calculate the driver resistance, Rd, needed (R2 in **Fig. 16**):

$$Rd = \frac{-t}{Ciss\,Ln(1-V2/V1)}$$

Where, t is the desired rise time of the gate signal (usually 15-20nS), V1 is Vg at saturation, V2 is the peak-to-peak gate voltage, or V1 minus Vgs(on), and Ln is the *natural* logarithm. For the driver in **Fig. 16**:

$$Rd = \frac{-t}{Ciss\,Ln(1-5v/4v)}$$

$$= \frac{-20nS}{120pF(-1.38)} = 120\Omega$$

Keep in mind, this value of Rd is based on the ideal current to charge *Ciss*, about 50mA. Again, I have found 25-30mA to be sufficient. This exercise does show that using Ohms Law for R2 is close enough (and a lot easier!).

The NA5N Mosfet Driver

Another driver scheme developed for my class D/E transmitters is shown in **Figure 17**. It is similar in some regards to the emitter follower driver in **Fig. 16**.

The low-level RF output from the TX mixer is applied to a high speed comparator, which converts the RF sinewave into a square wave. The operation of the TX mixer and comparator is beyond the scope of this part of the article, but will be presented in a class D & E transmitter construction project in Part 3. Suffice it to say that the duty cycle of the square wave is variable from about 15–45%. The

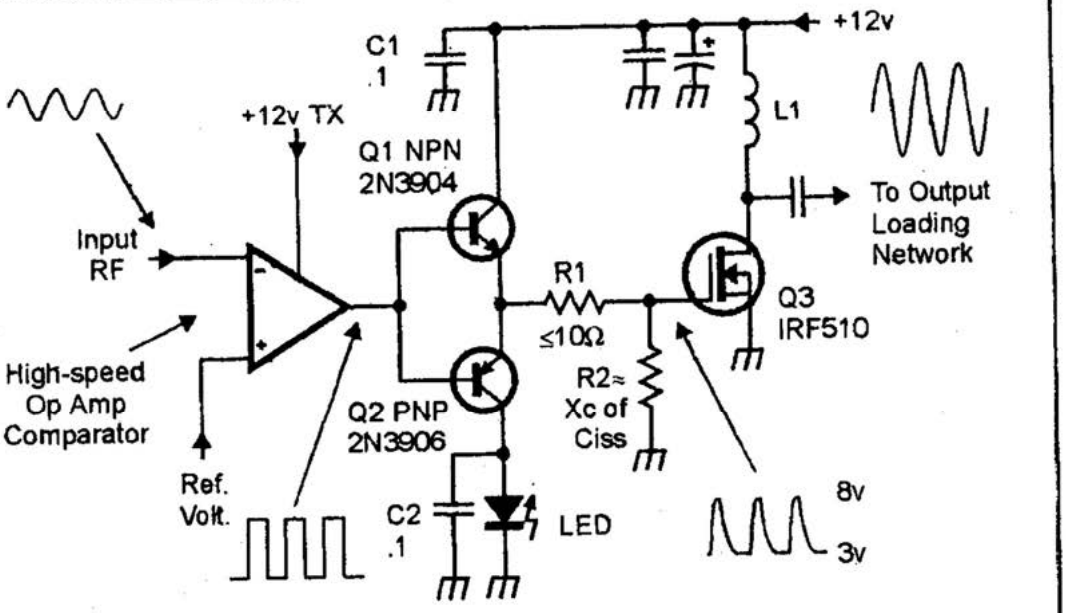


Fig. 17 – NA5N NPN-PNP Emitter Follower Mosfet Driver

comparator is powered from +12v TX, so that during receive, the output is 0v, disabling the IRF510 drive circuitry.

On transmit, the comparator output is an 8Vpp square wave at the RF frequency, such that the dc output levels are about +1v LO to +9v HI.

This emitter follower is an NPN-PNP pair, commonly called a "totem pole" configuration. Since the base voltage is an 8v square wave, the transistors are driven nearly into saturation and cutoff, acting as switches. When the comparator output goes from LO to +9v HI, both the NPN and PNP are turned on. Q1 emitter voltage is the +9v base voltage, minus the 0.7v junction drop. This 8.3 volts is applied to the emitter of Q2, allowing it to be forward biased as well. The 8.3v is also the PA gate drive. R1+R2||Xc is the output load to Q1 and the input impedance to the IRF510, such that the impedance is self matching. This yields 25–30mA of gate current drive from Q1. About 8mA passes through Q2, illuminating the LED.

When the square wave goes to +1v LO, Q1 and Q2 are barely forward biased and conducts ~8mA due to the LED. This causes a 2v drop across the LED, and ~1v across Q2, leaving +3v at the Q1-Q2 emitters – and the mosfet gate – turning off the IRF510.

Even though there is only 2.5v drive to the IRF510 gate, the +8v previously on the gate *Ciss* is now discharging. This decaying gate voltage also appears on the Q1-Q2 emitters. The low Q2 emitter-collector resistance, which is in parallel to R2, gives *Ciss* a lower resistance to discharge into. When *Ciss* is discharged, Q2 turns off. Thus, the purpose of Q2 is to place a low-Z load across the IRF510 gate to quickly discharge *Ciss* when the mosfet turns off.

For class D/E/F efficiency, the drain

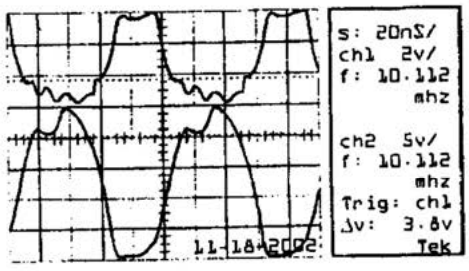


Fig. 18 – Gate/Drain Waveform

current must be zero before the next square wave LO to HI transition occurs.

Figure 18 is an oscilloscope display of this circuit driving a class E transmitter. The top trace is the **gate voltage** at 2v/div. Vgs(th) of this particular device is 3.8v, shown by the dotted line marker on the oscilloscope. Gate voltage rises fairly quickly to saturate at 8v. When the drive signal switches from HI to LO, the action of Q2 discharges *Ciss* and drops the gate voltage below Vgs(th) faster than the emitter follower version in **Fig. 16**. In this case, R1=3.9Ω and R2=220Ω.

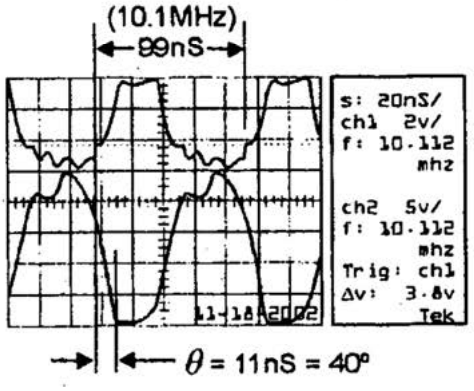
Gate voltage settles out around 2.5v, due to the LED and Q2, keeping the IRF510 turned off. If the gate were allowed to discharge to 0v, it would take longer to charge *Ciss* when the next gate drive goes HI. This saves 2.5v of *Ciss* charging. The main purpose of the LED is to provide this gate bias when the mosfet is off. Of course it does make for a nice XMIT indicator as well, indicating RF is being supplied to the IRF510, rather than simply coming off the key line.

The bottom trace is the **drain voltage** (Vd) at 5v/div. The peak-to-peak voltage is about 25v, the 2Vcc (or 2Vdd) expected. Note that when the gate voltage reaches +3.8v Vgs(th) going HI, the drain voltage is just passing through 12v Vcc – the point when drain current is zero. This is exactly the point you want the gate voltage to reach Vgs(th) to start drain current to flow. Vd drops from 12v down to 0v, indicating drain current is increasing. When the gate voltage reaches 8v, drain current should be saturated, evidenced by Vd reaching ~0v. In this case, Vd=0.4v, certainly indicating the IRF510 is in saturation, or the "full-ohmic on" region. This is important, as the closer to 0v at maximum drain current, the smaller the power losses across the drain–source junction. The lower the loss, the higher the efficiency. The drain current is also building up the current field in inductor L1 at this time. If drain voltage does not reach <1v, the mosfet is not in saturation.

When the gate voltage begins it's HI to LO transition, to turn OFF the mosfet,

Calculating PA Efficiency

PA efficiency of class D/E/F can be easily measured on an oscilloscope by measuring the LO to HI gate drive transition to the point the drain current first saturates (when drain voltage hits the lowest value). This accepted method is basically a measure of how long you spend in the linear region. The time to reach saturation is compared to the time of the RF cycle to determine the phase delay, in degrees. The steps to calculate PA efficiency, based on the NA5N driver and PA waveform in **Fig. 18**, are shown below. Calculating efficiency based on measuring PA currents (input vs. output power) yielded 91%.



❶ Measure time difference (in nS)

❷ Convert to phase difference (degrees)

$$\theta = \frac{11nS}{99nS} = .11 \times 360^\circ = 40^\circ$$

❸ Calculate PA efficiency, η

$$\eta = \frac{\sin\theta \times 360^\circ}{2\pi\theta} \quad \text{where } \sin 40^\circ = .64$$

$$\eta = \frac{.64 \times 360^\circ}{6.28 \times 40^\circ} = \frac{230}{251} = 92\%$$

drain voltage begins to rise, indicating drain current is turning off as desired. Gate voltage drops from +8v to +3.8v Vgs(th) faster than the single emitter follower waveform in **Fig. 16**, due to the loading effect of Q2. Drain voltage rises above 12v Vdd as the current stored in L1 now dumps into the output network when drain current stops.

In class E, L1 is also part of the output tuned circuit, resonant at the transmit frequency by the shunt capacitor in conjunction with the internal *Coss*. See "Cv" in **Fig. 6, Part 1**. When the current stored in L1 is depleted, drain voltage will begin to decrease. However, in class E, the energy stored in the capacitor parallel to L1 will provide voltage when the current in L1 is depleted, causing the familiar "fly-wheel" effect of the resonant circuit. In **Fig. 18**, the hesitation in drain voltage at 20v is when L1 runs out of current, and the voltage peak to 25v is the voltage being supplied by the shunt capacitor, which has been charged to 2Vdd. Two or three peaks may be seen at the 25v level, depending upon the harmonic power present. With this waveform, the transmitter had a power range of 1W to 9W (by varying the duty cycle from 15% to 45%) with an overall efficiency of 85% and a PA efficiency of 92%.

Class D Drain Output Efficiency

The output capacitance, *Coss*, lowers efficiency, since it must be charged to ~2V_{DD} by the mosfet. The equations below show how efficiency, η, is based on the switching power, Ps, lost across *Coss*. The following math only serves to make two important points below.

At V_{DD}=12v, for a 20M 5W transmitter, with Cs=120pF and Vsat=0.5v (where Ps is the switching loss in watts):

$$Veff = V_{DD} - Vsat = 12v - 0.5v = 11.5v$$

$$Ps = Coss(2Veff)^2 \times 2fo =$$
$$= 120pF(2*11.5)^2 \times 2(14MHz) = 1.78W$$

$$\eta = \frac{Po}{Po+Ps} = \frac{5W}{5W+1.78W} = 74\%$$

In some of the amateur literature, the recommendation is sometimes given to raise the mosfet drain voltage for higher efficiency. Let's see if this is true.

At V_{DD}=18v, to produce 5W output power:

$$Veff = 18v - 0.5v = 17.5v$$

$$Ps = 120pF(2*17.5)^2 \times 2(14MHz) = 4.1W$$

$$\eta = \frac{5W}{5W+4.1W} = 55\%$$

Increasing V_{DD} to 18v does produce 5W with less drain current. However, charging *Coss* to 36v (2V_{DD}) greatly increases the switching power loss, lowering efficiency from 74 to 55%. This should dispell the rumor that increased V_{DD} lowers efficiency – and that the +12v customarily used by homebrewers is actually quite ideal for switching mosfet QRP PAs.

The second point with the above equations is how the *switching losses are frequency dependent*, due to the term "2fo." The lower the frequency, the lower the losses, and hence higher efficiency. Therefore, a Class D/E/F PA will be much more efficient on 80M than 20M. This is why most Class E circuits on the internet are only for 160M or 80M, as even a sloppy job of designing the circuit and using a sinewave drive will still yield high efficiency. Re-calculating the 20M 12v QRP example to 160M yields an astounding 96%.

$$Veff = 12v - 0.5v = 11.5v$$

$$Ps = 120pF(2*11.5)^2 \times 2(1.8MHz) = .23W$$

$$\eta = \frac{5W}{5W+.23W} = 96\% \text{ !!!}$$

This is also why those scaling these amplifiers for 20M have had disappointing results, as the switching power losses double as you double the operating frequency.

A few loose ends ...

IRF510 vs. IRL520

The IRL520 is a logic family mosfet, meaning it is designed to saturate with only 5V (TTL logic HI) on the gate. It would therefore seem the IRL520 would be ideal for a class D/E/F PA for QRP, since it can be turned on with only a 2v swing on the gate. However, the input capacitance, Ciss, for the logic drive devices is very high – in the order of 300-400pF. This is tolerable for their intended purposes in 50-100 KHz switching power supplies, but virtually impossible to drive at HF frequencies. I have built some fairly successful Class C PAs with IRL520's, but efficiencies at Class D/E/F never much more than 50%. Theoretically, one can drive the gate with a parallel inductance to cancel out this huge capacitance through resonance, but I have not yet tried this. There are some SMC SOT-23 logic mosfets with a lower *Ciss* worth experimenting with.

Other switching MOSFETs

Just look through the Mouser or Digi-Key catalog and you will see listings for legions of cheap, switching mosfets. Many can be used in lieu of the IRF510. In order to use them for Class D/E/F, you need to know primarily the Vgs(th), Vg(sat), and output capacitance, *Coss* or *Cds*. Maximum drain current is also important. For QRP power levels, you want a device with a Id(max) of 1-2A for smooth power control with a 50% duty cycle, since you are forcing maximum Id for some period of time. The IRF510 Id(max) is about 4A. Such a high Id(max) actually makes the IRF510 a bit difficult to control in the 5W or less range.

Surface Mount MOSFET's

Some of the switching mosfets that meet the above requirements are only available in surface mount packages, such as SOT-23's with Id(max) around 1.5–2A. I have built a class D and E PA with these devices with good success, and surprisingly, the high efficiency causes little heating of these very small packages. However, operating them Class C causes excessive heating above about 2W. There is just very little room for error with a SOT-23 due to the low power dissipation of such small physical packages.

Other available literature

There is plenty of available information on Class D/E/F transmitters on various websites, engineering magazine articles and the application notes in National and Motorola data books. However, this information needs to be used with caution for QRP, as most are based on RF type switching mosfets, deal with power ranges in the hundreds of watts, push-pull circuits, or frequencies below HF, such as for AM broadcasting or ultrasonic use. Still, these articles are worth further study for those wishing to learn more, keeping the application of the article in mind.

Interpretting the IRF510 Data Sheet

The data sheet for the International-Rectifier IRF510 is in **Appendix B**. This is extracted from their complete data sheet.

Maximum Ratings. Continuous drain current is important, as this is about the drain current for the period of time the IRF510 is in saturation. This should stress why controlling output power with a small duty cycle is important. Maximum gate-to-source voltage is ±20v, which will easily handle the +10v required for saturation.

Electrical Characteristics. **RDS(on)** is the "on-resistance," which only occurs when fully saturated. Note the Test Conditions define the saturated state with VGS=10v. When in the linear region, RDS is the standard equation for $R_L = Vdd^2/2Po$.

Vgs(th) is the gate voltage where drain current begins to flow. Note the huge range - typical of mosfets. Most devices will be about 3.5-4v. **LD** is the internal inductance that adds to the external inductance on the drain. In class E, where the drain inductance forms a tuned circuit, the value of LD is sufficiently low to not alter calculations. **Ciss** and **Coss** are the input and output capacitances. These are very important, especially for class D/E/F. Note the test conditions are for Vgs=0v, that is, with no drain current flowing. With drain current, Vds will drop from +12v to 0v (at saturation) and these values change, as shown in **Fig. 3** on the data sheet. Timing parameters, **Td(on)**, **Tr** and **Td(off)** are defined in **Fig. 6**. For class D/E/F, the faster the better. Theoretically, the fastest a mosfet can switch is the time of Tr+Tf+Td(on)+Td(off), which equals 54nS for the IRF510. Tf is assumed to be about Tr if not listed. The maximum frequency would thus be 1/54nS = 18.5MHz. Tr and Tf define the typical time to charge and discharge Ciss and Coss. These times can be increased a bit by increasing the gate drive current, as discussed in the article, and raising fmax to some extent.

Fig. 1 shows drain current (Id) vs the drain-source voltage (Vds) at 25°C. This is similar to the transfer characteristic curves for a BJT. **Fig. 2** is the same, except at a device temperature of 175°C. Note that as the IRF510 gets hotter, drain current gets less, protecting itself from thermal runaway. This is opposite the effect of a BJT, where the BJT gets hotter, more collector current flows, producing more heat, then more current, until the device destroys itself by thermal runaway. Again, a mosfet protects itself from thermal runaway. This explains why your class C IRF510 PA drops in output power as the device gets hot.

Fig. 4 is the transfer characteristics of the IRF510. This shows how much drain current flows vs. the gate voltage. Note that the graph begins at 4v, as less than that, the mosfet is in "cut off." Also note the drain current is less at 175°C. This shows how device saturation occurs around Vgs=8v, where little further increase in drain current occurs with increasing Vgs. Below Vgs=8v is the linear region, although it is not very linear (more "curved" in shape). The transfer curve is steepest between about 4 to 5v Vgs. This is the area of maximum gain. This shows why IRF510s have also been used as very high gain RF amplifiers or mixers, by exploiting a gate voltage only slightly above Vgs(th).

Fig. 5 shows the maximum drain current vs. temperature. For class C QRP transmitters, device temperature can quickly rise to 150°C on key down, but still in the safe operating region for 1A of drain current. Class D/E/F runs considerably cooler. In fact, a barely warm IRF510 after 30 seconds of keydown is the ultimate proof of the increased efficiency. Try that with class C and you'll loose your fingerprint!

In **Part 3** of this series will be two construction projects for you to build – a QRP Class D and E transmitter using the IRF510. Both can be added to about any QRPp transmitter to produce 5W output, or for a "roll-your-own" transmitter.

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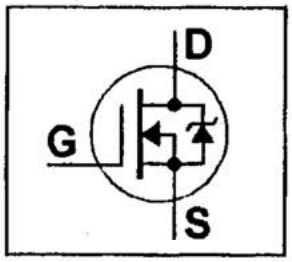
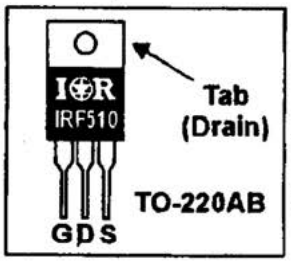
Appendix B – IRF510 Data Sheet

International
IOR Rectifier HEXFET® Power MOSFET **IRF510**

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- 175°C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements





Description

Third generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

Absolute Maximum Ratings

	Parameter	Maximum	Units
I_D @ Tc = 25°C	Continuous Drain Current, V_{GS} @ 10V	5.6	A
I_D @ Tc = 100°C	Continuous Drain Current, V_{GS} @ 10V	4.0	A
I_{DM}	Pulsed Drain Current	20	A
P_D @ Tc = 25°C	Power Dissipation	43	W
V_{GS}	Gate-to-Source Voltage	±20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C

Electrical Characteristics @ TJ = 25°C

	Parameter	Min.	Typ.	Max.		Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS}=0V
$R_{DS(on)}$	Drain-to-Source On-Resistance	—	—	0.54	Ω	v_{GS}=10V, I_D=3A
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=VGS
g_{fs}	Forward Transconductance	1.3	—	—	S	V_{DS}=50V, I_D=3A
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{GS}=0V @25°C
$I_{GSS(fwd)}$	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS}=20V
$I_{GSS(rev)}$	Gate-to-Source Reverse Leakage	—	—	-100	nA	V_{GS}=-20V

Electrical Characteristics @ TJ = 25°C – Cont'd

	Parameter	Min.	Typ.	Max.		Test Conditions
LD	Internal Drain Inductance	—	4.5	—	nH	Lead to die
LS	Internal Source Inductance	—	7.5	—	nH	Lead to die
Ciss	Input Capacitance	—	180	—	pF	VGS=0v, f=1MHz
Coss	Output Capacitance	—	81	—	pF	VGS=0v, f=1MHz
Crss	Reverse Transfer Capacitance	—	15	—	pF	VGS=0v, f=1MHz
Td(on)	Turn-on Delay Time	—	6.9	—	nS	VDD=50v,ID=5.6A
Tr	Rise Time	—	16	—	nS	VDD=50v,ID=5.6A
Td(off)	Turn-off Delay Time	—	15	—	nS	VDD=50v,ID=5.6A

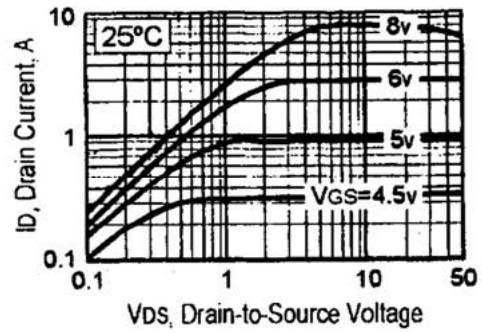


Fig. 1. Typical Output Characteristics (25°C)

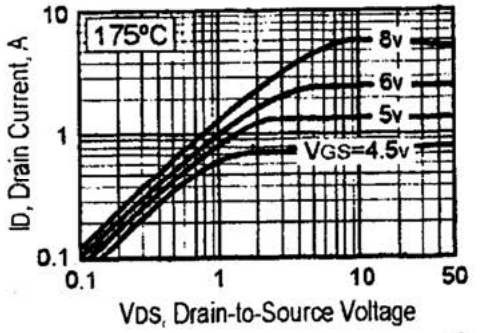


Fig. 2. Typical Output Characteristics (175°C)

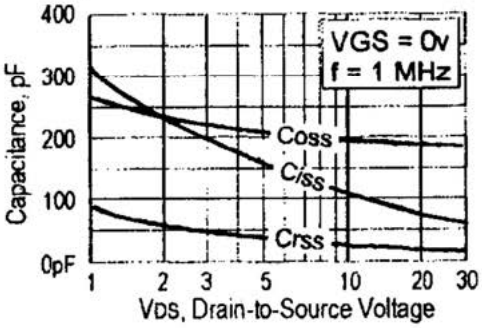


Fig. 3. Typical Capacitance vs. VDS

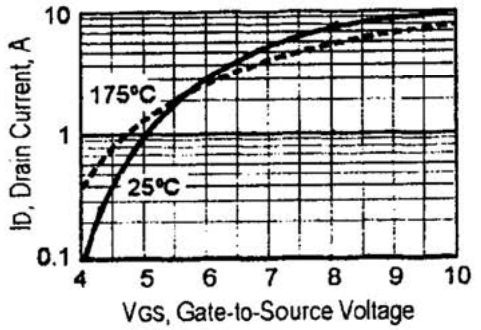


Fig. 4. Typical Transfer Characteristics

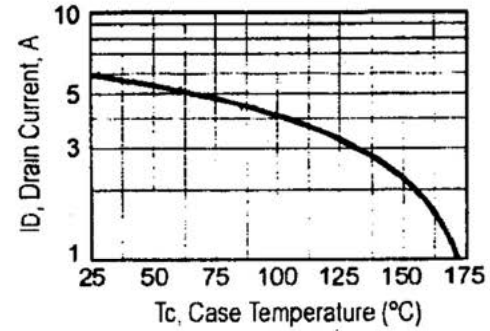


Fig. 5. Maximum Drain Current vs. Case Temperature

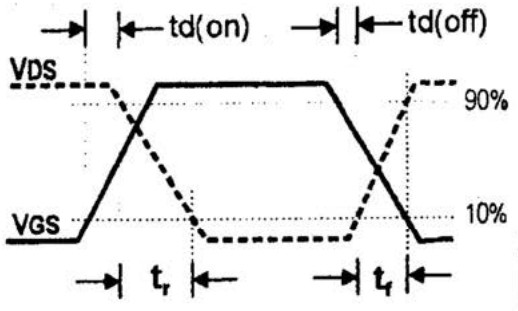


Fig. 6. Switching Time Waveforms