

Tyler Creelan de Laguna

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Software Engineer

EDUCATION

Bachelor of Science in Computer Science with Honors, Oregon State University

Master of Science in Computer Science, Oregon State University

EXPERIENCE

Code for America

2020-2021

Volunteer contributor for civic tech non-profit sponsored by Gates Foundation.

Intel Corporation

Software Design Engineer - Mobile

2013-2017

Optimized design of the Intel Atom SoC, focus on low power interactions:

- Added experimental Linux kernel driver support for low-power Display Engine and frame compression in drm/i915 module, extending battery life to attain a prospective Internet of Things (IoT) customer.
- Expanded LLVM-derived C++ framework (Maestro) to stress interconnect hardware with machine code.
- Emulated tablet designs on Mentor Graphics Veloce platform, selectively dispatching Linux flows to Simics to achieve tractable regressions for pre-tapeout confidence.

Software Design Engineer - Simulation

2010-2013

Improved prototypes of Core i7 power controller (PCU) as extended tour of duty:

- Rendered new algorithms into C++ for memory power limits and Turbo Boost 2.0, comparing to proprietary Harvard arch assembly microcode. Created model in Specimen 'e' to find 11 firmware path bugs before tapein.
- Resolved power spike with running power limits (RAPL); analyzed verilog to create experimental patch and satisfy blade server customers, receiving Division Recognition award.

Software Engineer - Post-Silicon

2004-2010

Team lead for power analysis of new CPUs, creating strategy at tape-in to meet biannual product qual:

- Built new Win7 app in Qt C++ for wattage telemetry, heading off 400mW routing bug in Xeon boards.
- Tamed unresponsive I/O Hub by reordering QuickPath Interconnect (QPI) packets: prototyped with Focused Ion Beam (FIB) edits: revealed new catastrophic C-state bug in time for emergency stepping.

Graduate Technical Intern

2002-2003

Designed new analyzer to verify sleep protocols on prototype Intel Pentium processors:

- Updated 50k line Microsoft Visual C++ test harness on host/target coupled with JTAG probe.
- Traced firmware flows in physical memory with linear debug registers over test access port (TAP).
- Scanned ACPI machine language to find wake vector, placing cacheline breakpoint to trap on OS wake. Detected new circuit logic bug in Pentium 4, in time to fix for Intel64 launch

Oregon State University

Graduate Research Assistant

2003-2004

Performed research into reliability engineering under NSF grant:

- Designed novel system for usability studies, expanding 5k line Common Lisp (CLOS) engine connected to Java AWT interface over tcp/ip. Added new lookahead LR parser with yacc.
- Led classroom recitations for introductory CS courses; created homework and projects.
- Designed machine learning network analyzer in Perl with decision trees to detect four intrusion attack types.

OPEN SOURCE

- Advanced Component Platform Architecture (acpi.sourceforge.io): C, Linux, System states, BIOS
- Gnumeric (gnumeric.org), Testmeric module: Corba C++, gtk, glibc.
- Debian GNU/Linux, Sarge Release (debian.org): archives, Bash, automation

PUBLICATIONS

- 1) “Power vs Debug: Solving IEEE JTAG Observability with Deep Powerdown™ (C6) active”, Intel Design Technology and Test Conference (2007). Tyler Creelan, N Ashraf and Jeff Maxwell.
- 2) “Reporting CPU Frequency: The Challenge of Intel Turbo Boost™ Technology”, Intel Design Technology and Test Conference (2007). Tyler Creelan and Todd Baird.
- 3) “Scaling a Dataflow Testing Methodology”, IEEE International Symposium on Software Reliability Engineering. (2006) p13-22. M Fisher, G Rothermel, T Creelan and M Burnett.
- 4) “Educators Have Hard Choices; Nationally”. Science (Letters). Vol 289 (2000). Tyler Creelan.

CERTIFICATIONS

Google: Project Management | Linux Debug: Intel Open Source Technology Center
Win10 Kernel Debug | PCIE-3, USB-3 - MindShare

PROFESSIONAL ASSOCIATIONS

Microsoft TEALS Tutor | ACM International Programming Contest State Champion Team
Portland C++ User Group | ACM University Student Chapter Officer | Techqueria

TECHNICAL SKILLS

- **Software Programming Skills:** C/C++, Java, Bash, Posix, Sus, Qt, Linux modules, x86 asm
- **Hardware Design and Debug Skills:** Specman, Intel microarchitecture, Test Access Port (TAP)
- **Tools:** Github, Subversion, Vim, clang, kernel debug, adb, WinDbg
- **Operating Systems:** Debian GNU/Linux, Android, MacOS X
- **Interface Protocols:** ACPI, Extensible Firmware Interface (EFI), JTAG