# Still Benchmarking After All These Years

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## ABSTRACT

Circuit benchmarks for VLSI physical design have been growing in size and complexity, helping the industry tackle new problems and find new approaches. In this paper, we take a look back at how benchmarking efforts have shaped the research community, consider trade-offs that have been made, and speculate on what may come next.

## CCS CONCEPTS

• **Hardware → Electronic design automation**.

## KEYWORDS

benchmarking; circuit placement; metrics

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## 1 INTRODUCTION

Integrated circuits have evolved at a breakneck pace for decades. The first MOSFET transistors were created at the end of the 1950's, with Moore[1] making his bold prediction for exponential growth in 1965. While it might have seemed far-fetched or wildly optimistic at the time, Moore's Law has been a relentless juggernaut. In 1960, only a handful of transistors could be integrated into a single device, but by 1980, just twenty years later, the Motorola 68000 had roughly sixty-eight thousand transistors. Twenty years after that, the Intel Pentium 4 featured roughly forty-two million transistors. Twenty years after that, in the era in which this paper is being written, the Apple M1 processor has in excess of sixteen billion transistors.

The technological advances required for this progress have not been spontaneous. At each step along the way, researchers from both academia and industry, and from a wide range of fields, have been quietly identifying and overcoming technological barriers. The massive electronics industry, which has impacted almost every aspect of modern life, is the product of decades of hard work.

Benchmarking, the practice of using example problems to compare different solution approaches, has been critical to this progress. Benchmarks with well defined metrics, and that are widely available, are most helpful; they can engage a broad audience, drawing in contributions and ideas. The market forces that have driven the electronics industry forward have also in some ways been a barrier; secrecy around process technologies, circuit designs, and design methodologies give a competitive advantage, and groups at the leading edge of technology are often reluctant to reveal their secrets.

In this paper, we look back on benchmarking in physical design, with an emphasis on circuit placement. Following something of a rocky start, the physical design community has found workable solutions that protect the intellectual property of industry leaders, while also opening up design benchmarks for the general public. This has allowed physical design to evolve to a state where sustained, regular progress can be made. The annual ISPD contests have been a catalyst for research, and have also served as an excellent way strengthen and grow the research community.

## 2 PLACEMENT BENCHMARKING

The very earliest circuits were designed by hand, each one a custom creation. As design sizes increased, and semiconductor fabrication technologies became more refined, automation became essential and designers converged on a few common conventions and abstractions. Lambda-based design rules and standard cell libraries[2] allowed the physical design of circuits to be handled by software. A design flow of logic synthesis, to placement, and to routing, enabled interchangable design automation tools and encouraged common design file formats.

In circuit placement, there are a number of different metrics used to evaluate solutions. The simplest is a *half perimeter wire length estimate*; for a standard cell design, the cells are placed into horizontal rows, with the bounding boxes of the pins for each net being used as an estimate of routing distances. With the simple metric, determining which placement is "best" can be done by simply comparing total lengths.

Complete circuit routing, rather than wire length estimation, can complicate matters considerably, however. If the wiring demand


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**Table 1: The original MCNC standard cell benchmarks[4].**

| Name | # cells | # nets | # I/O |
|---|---|---|---|
| fract | 125 | 147 | 24 |
| primary1 | 752 | 985 | 81 |
| struct | 1888 | 1920 | 64 |
| industry1 | 2271 | 2593 | 814 |
| primary2 | 2907 | 3136 | 107 |
| biomed | 6417 | 5742 | 97 |
| industry2 | 12142 | 13419 | 495 |
| industry3 | 15059 | 21940 | 375 |

in an area of the chip is high, this can result in routing detours – which increase wire lengths – or even result in routing failure. To address this, placement metrics often include a *density* constraint – limiting the number of cells or pins in any area of the design.

The metrics can be improved further, taking into account the wiring produced by a complete run of a global and detail router. With information about cell functionality, circuit timing, power consumption, and other metrics can be evaluated.

There is something of a balancing act with placement metrics. A simple metric such as wire length can give a clear indication of "winners" and "losers" – but this may miss key performance concerns. If multiple metrics are in place, which approach can be considered "best" is much less clear.

## 2.1 Early Benchmarks

There were few commonly available circuits and benchmark problems in the early days. In 1987, a panel discussion[3] highlighted the need for good benchmarks for standard cell design, and a few years later in 1991, the MCNC benchmarks[4] were presented and quickly gained prominence. The benchmarks are shown in Table 1 – while they were not comparable in size and complexity to the leading edge of industrial design, they filled a vacuum, and were a catalyst for academic research. The availability of circuits that could be used as physical design benchmarks sparked a wave of circuit placement research; there was heavy competition between simulated annealing[5], numerical methods[6], and recursive bisection[7].

There was hope that more benchmarks would become available, with Kozminski[4] noting the following:

> It seems apparent that more benchmarks for layout synthesis are needed, they should be more fully described, as discussed earlier in the paper. In the opinion of the author, distributing pure geometrical data is no longer sufficient for meaningful benchmarking of algorithms used in real-life applications to produce working chip layouts. The circuit's function as well as its speed and timing requirements should be supplied together with technological data required to verify the performance of the completed design. As an unavoidable consequence, future benchmarks will have to come from sources willing to put the information about logical functions of the benchmark circuits in the public domain.

A decade later in 2001, however, the original MCNC benchmarks were still in wide use, and the gap between academic research and industrial practice had widened. The lack of new benchmarks resulted in many groups adapting the MCNC benchmarks in one way or another. Cell sizes were adjusted and mapped to new libraries, to keep track of changing process technologies. Routing models shifted from a channel-based approach to over-the-cell, as additional routing layers became available. The files originally released were translated from one format to another, to take advantage of new design automation tools, and to provide compatibility with new software.

All of these changes undermined one of the original objectives of the benchmarks – comparison of different placement strategies. Rather that having a clear indication of which techniques were effective, and highlighting key problems to solve, the research literature was cluttered with results that were unintentionally ambiguous[8].

## 2.2 From Partitioning to Placement

Researchers in both academia and industry were troubled by a lack of up-to-date physical benchmarks. It was broadly understood that good benchmarks were necessary for academic research – but intellectual property constraints limited what any leading-edge company could release. A benchmarking break-through for circuit placement arrived in the form of the release of the "ISPD98" partitioning benchmarks by Alpert[9].

Alpert noted the following:

> All information relating to circuit functionality, timing and technology is removed. Unfortunately, this limits the direct applicability of these circuits (e.g., functional replication for partitioning); yet, the release of these circuits would have been impossible otherwise.

Intellectual property concerns were addressed by stripping away functionality, and by removing some portions of the circuit. With the net list structure, however, it was possible to construct a placement benchmark that could be used for an objective such as wire length minimization – Wang[10] did this for standard cells, with Adya[11] taking the idea further to create placement benchmarks that mixed standard cells and macro blocks.

After a number of years of little change, there was a burst of activity. The GSRC supported GTX project[12] provided an excellent platform to work from, with many researchers from academia and industry becoming involved. The GSRC "bookshelf[13]" became stocked with a variety of design benchmarks and design automation tools.

# 3 THE ISPD CONTESTS

With new "anonymized" net lists and simplified file formats, many pieces were now in place to accelerate research in physical design. The physical design community, and in particular those active within ISPD, collaborated to create new benchmarks, and to have a forum for their dissemination. This evolved into the ISPD contest series, with the first contest focusing on circuit placement.

Typically, an ISPD contest involves the following.

**Table 2: The ISPD Contests.**

| Year | Contest |
|---|---|
| 2005/2006 | Placement |
| 2007/2008 | Global Routing |
| 2009 | Clock Network Synthesis |
| 2010 | High Performance Clock Network Synthesis |
| 2011 | Routability-Driven Placement |
| 2012/2013 | Discrete Gate Sizing |
| 2014 | Detailed Routing-Driven Placement |
| 2015 | Blockage-Aware Detailed Routing-Driven Placement |
| 2016 | Routability-Driven FPGA Placement |
| 2017 | Clock-Aware FPGA Placement |
| 2018/2019 | Initial Detailed Routing |
| 2020 | Wafer-Scale Deep Learning Accelerator Placement |
| 2021 | Wafer-Scale Physics Modeling |

- An industry-affiliated research group defines a contest problem, and associated metrics. This is often aligned with a research challenge faced internally.
- A handful of sample problems are provided - contestants use these for initial experiments and design tool development.
- Prior to ISPD, the contestants provide executable versions of their tools to the industrial research group. The industrial group then performs experiments using both the public benchmarks, and also a set of benchmarks kept secret.
- At ISPD, the results of the contest are announced, and all benchmarks are made publicly available.

This practice has been of tremendous benefit. First, researchers with access to leading-edge technology can reveal their most pressing challenges, and make it possible for the broader community to contribute – while also protecting proprietary information. The problems faced are simplified so that new students can gain an understanding of the field, and try new ideas and approaches in a low-risk manner. Comparisons, performed by the industrial group, are balanced – there is no tuning or cherry picking of results. The competition also helps build the research community; students from different groups around the world have a shared experience, develop friendships, and find potential research collaborators.

The ISPD contests are shown in Table 2. In the remainder of this section, we will discuss placement-related contests in more detail.

## 3.1 Mixed Size Placement, 2005, 2006

The ISPD contests began with a focus on placement, using net lists with a mixture of standard cells and macro blocks[14]. As most placement tools were unable to handle movable macro blocks, these were fixed in place for the contest.

A new set of benchmarks – derived from industrial designs, but with fewer modifications than found with the ISPD '98 partitioning benchmarks – were released. These benchmarks were several orders of magnitude larger than the MCNC set, testing the scalability of different algorithmic approaches. The largest benchmark, bigblue4, contained more than 2.1 million movable objects, and more than eight thousand fixed macros. The benchmarks also had a great deal of internal white space; the chips had fixed outlines, and not all silicon area was utilized.

**Table 3: ISPD 2005 Placement Benchmarks**

| Circuit | # Objects | # Movable | # Fixed | Nets |
|---|---|---|---|---|
| adaptec1 | 211447 | 210904 | 543 | 221142 |
| adaptec2 | 255023 | 254457 | 566 | 266009 |
| adaptec3 | 451650 | 450927 | 723 | 466758 |
| adaptec4 | 496045 | 494716 | 1329 | 515951 |
| bigblue1 | 278164 | 277604 | 560 | 284479 |
| bigblue2 | 557866 | 534782 | 23084 | 577235 |
| bigblue3 | 1096812 | 1095519 | 1293 | 1123170 |
| bigblue4 | 2177353 | 2169183 | 8170 | 2229886 |

The contest organizers also provided scripts to check legality of solutions, ensuring that comparisons would be unbiased. For 2005, the only metric considered was half-perimeter wire length; in 2006, the contest was extended to consider routing congestion. Nine teams competed in 2005; the next year, the number of teams increased to ten.

## 3.2 Routability, 2011

Although half-perimeter wirelength and placement density are important first-order metrics for evaluating placement quality, they do not address a key design requirement – routability. Excessive wirelength, potentially due to over-spreading or very good wirelength with excessive packing can both lead to unroutable designs. Additionally, probabilistic metrics for congestion prediction are not always accurate, especially on advanced designs with complex metal stacks, including a large number of metal layers. To address both these issues the focus of the 2011 contest [15] was routability-driven placement, where the routability of the placement algorithms was evaluated using a real global router [16].

The ISPD-2011 contest introduced the "superblue" series of benchmarks, which contained several placement features representative of industrial ASIC designs like non-rectangular fixed objects, fixed macro pins within the core area but on higher metal layers allowing "overlap" with standard cells, numerous large macros, regions with a large number of fixed standard cells, and varying design densities from 30–60%. A key feature of this benchmark suite was that it could also be used to perform global routing. Designs were configured with nine metal layers, with varying width and spacing across layers, complicating both placement and global routing.

Contestants were primarily evaluated using a hybrid metric comprised of placement routability and placer runtime. Instead of relying on indirect metrics, a real global router was used to measure the routability of the placement solutions. The routability metric used was the the total overflow of the routing solution generated by the global router across all metal layers. In case of a tie in the primary contest metric a secondary metric based on the routed wirelength and placer runtime was used.

Nine teams entered placement tools – and there was a "contest within a contest," with five teams entering a global routing competition for being picked as the "golden" router to evaluate the placement solutions. Many of the contest entries have matured, and

are part of the open-source design automation tool flow discussed in a following section.

As evidenced by several publications in subsequent years, the ISPD-2011 contest advanced academic research in several areas, such as, global and detailed routability-driven placement, global routing, and fast but accurate congestion analysis / routability prediction.

### 3.3 Detail Routing Driven Placement, 2014, 2015

Continuing the evolution of placement benchmarking, the contests in 2014 and 2015 examined the interactions of detailed routing with placement closely[17, 18].

Design rules for deep submicron circuitry are quite complex; spacing, alignment, and a variety of other factors make fabricating the wiring at the cell level difficult. The new benchmarks tracked minimum spacing rules, end-of-line rules, pin blockage, and more.

Because of the complexity, contest problems shifted from the simplified GSRC Bookshelf formats to industry-standard LEF and DEF; more challenging for the development of an academic tool, but necessary to capture the constraints of leading edge design.

Despite the difficulty of the problem, many teams competed, with a collaborative effort between the University of Calgary and the University of Waterloo taking first in the contest in 2014[19]; this team placed second in 2015[20]. The winner from 2015 was an effort from National Taiwan University[21].

### 3.4 FPGA Placement 2016, 2017

FPGA placement became the topic of the ISPD Contests for 2016 and 2017. As FPGA hardware technology advances and FPGA design sizes increase, the core EDA algorithms including place and route face greater challenges. Traditional academic FPGA placement study was primarily based on benchmarks from the VPR[22] era. From modern FPGA design point of view, these benchmarks are relatively small and the underlying FPGA architecture is overly simplified. A new set of benchmarks mapped to latest commercial FPGAs drew attention from academic research groups.

The ISPD 2016 Xilinx held Routability-Driven FPGA Placement Contest [23] was the first FPGA placement congest aiming on routability, with benchmarks mapped on state-of-the-art commercial FPGA architecture based on 20nm technology. The contest attracted 19 academic teams, while 12 of them submitted final placer into benchmarking. Contesters' placers were tested on a set of 12 testcases, with largest size at 1.1 million movable instances. The placement quality was measured by Vivado router in Xilinx tool flow. If the placement passes legality check and it is routed successfully, total routed wirelength is used as the key metric. The total runtime of place/route also matters. It serves as a scaling factor impacting the metric by +/-10 percent. UTPlacer[24] (from University of Texas Austin), RippleFPGA[25] (from Chinese University of Hong Kong) and GPlace[26] (from University of Guelph) won the first, second and third place, respectively.

The ISPD 2017 Clock Aware FPGA Placement Contest[27] was an extension from 2016's topic. Clocking networks in FPGA devices pose a major constraint to the placement problem, because FPGA architecture designers need to find a balance between reducing clock network area and giving place/route flexibility. The problem becomes very challenging for modern FPGA designs with many clocks. 9 teams submitted their placers to compete. The final winners are UTPlaceF 2.0 [28] (from University of Texas Austin), NTUfplace[29] (from National Taiwan University) and RippleFPGA[30] (from Chinese University of Hong Kong).

The two ISPD FPGA placement contests triggered a lot of academic research in the subsequent years. Benchmarks released in the contests, together with the industrial tool supported evaluation flow, set up a perfect platform for researchers to try out various placement algorithms. There are successes on better placement quality[31] , faster runtime, algorithm parallelization[32, 33] , machine-learning enhancement[34].

## 4 FROM BENCHMARKS TO FLOWS

The CAD contests have been important venues for stimulating research on modern design automation challenges. However, most of the past contests only tackle the point tool problems confined to a single design stage, e.g., global placement contest in the ISPD-2006 placement contest [35] and the ICCAD-2019 global routing contest [36]. In order to foster research on cross-stage optimization and flow-scale design methodology, the IEEE CEDA Design Automation Technical Committee (DATC) [37] has over the past five years developed a public reference design flow, named *DATC Robust Design Flow (RDF)*, based upon the winning tools and research outcomes from the CAD contests. As highlighted in a series of the RDF papers beginning at ICCAD-2016 [38–43], the mission of DATC RDF is towards (i) establishing a complete, academic RTL-to-GDS flow built upon the outcomes of past CAD contests and leading research codes; (ii) consolidating design benchmarks and leading point tool libraries; and (iii) connecting academic research to industrial practice and designs by supporting industry-standard design exchange formats.

Table 4 outlines the components included in the latest DATC RDF flow [43] with the tools from the winning entries and research outcomes of past CAD contests highlighted in boldface. DATC RDF provides multiple paths from Verilog to routed DEF; it includes paths that are composed of the point tools from the past CAD contests for the important physical design stages. Besides, it also provides RTL-to-GDSII paths entirely based on recently-developed open-source CAD tools, which are capable of delivering DRC-clean layout in a commercial foundry enablement.

In the past year, the scope and mission of DATC RDF have further been extended to bring attention to design analysis and verification research. Specifically, the latest RDF-2020 release includes *calibration datasets* for two important electrical analyses: parasitic estimation and static timing analysis (STA) [44]. Academic research on RC extraction and STA is often *uncalibrated* due to the lack of standard calibration against which improvements can steadily be evaluated. We envision that the calibration datasets of DATC RDF help boost the research advancement along the axes of accuracy and capacity for fundamental analyses that guide IC physical design.

Many of the tools used in the RDF flow are also part of the OpenROAD[45] project – much of the success of these efforts have come from active collaboration of academia, industry, and professional society groups.

**Table 4: RDF-2020 flow components**

| Component | Tool |
|---|---|
| Logic synthesis | Yosys+ABC |
| Floorplanning | TritonFP |
| Global placement | RePlAce, FZUplace, **NTUPlace3**, **ComPLx**, **Eh?Placer**, **FastPlace3-GP**, **mPL5/6**, **Capo** |
| Detailed placement | **OpenDP**, **MCHL**, **FastPlace3-DP** |
| Flip-flop clustering | Mean-shift, FlopTray |
| Clock tree synthesis | TritonCTS |
| Global routing | **FastRoute4-lefdef**, **NCTUgr**, CUGR |
| Detailed routing | **TritonRoute**, **NCTUdr**, **DrCU** |
| Layout finishing | KLayout, Magic |
| Gate sizing | Resizer, **TritonSizer** |
| Parasitic extraction | OpenRCX |
| STA | OpenSTA, **iTimerC** |
| Database | OpenDB |
| Libraries/PDK | NanGate45, SKY130, ASAP7, NCTUcell |

## 5 CONCLUDING COMMENTS

Certainly, much has changed over the years. Preas[3] noted in 1987 that some circuits with over 10,000 cells were becoming commonplace – challenging to handle because representing them "may require a substantial fraction of a megabyte for storage." Gaining access to benchmarks, even if they were "publicly available," required knowing who to ask, where to look, and the navigation of anonymous FTP servers. Often, data was exchanged with magnetic tapes sent through the physical mail. Disk space, processor cycles, and memory, were all in short supply.

In this era, there are pocket-sized processors with vast amounts of RAM, high speed wireless communications, and almost limitless storage and compute resources in the cloud. Design benchmarks, and even complete tool flows in open-source format, can be downloaded directly from the web. Many of the logistical barriers that hampered research have been eliminated, and the contests have provided a framework in which industrial groups at the leading edge of technology can provide benchmarks and metrics to the broader research community.

The 2021 edition of the International Symposium on Physical Design will be conducted virtually, with talks and events streaming to attendees around the world. This is possible *because* of the decades of effort in the electronics industry, and the collaborations of countless researchers in academia and industry.

Looking back, the changes are staggering. It is safe to assume that progress will continue, and the world of twenty, thirty, forty years from now is hard to imagine. Certainly, there will be a need for new benchmarks, new metrics, new problem definitions; we would hope that ISPD and the ISPD contests would continue to be a venue for framing the problems to solve, and an entry point for future generations of design automation researchers.

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