Sudheer Kumar

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Objective

An exciting and challenging opportunity in the field of multi-core platforms and performance optimization.

Work Experience

Assistant Professor, Department of Mathematics & Computer Science, Sri Sathya Sai Institute of Higher Learning, July 2011 - May 2013

Education

Ph.D., Computer Science, Sri Sathya Sai Institute of Higher Learning, April 2013
- Advisor: *Prof. Ashok Srinivasan, Florida State University*
- Thesis: *Topology and Routing Aware Mapping on Parallel Processors*

M.Tech., Computer Science, Sri Sathya Sai Institute of Higher Learning, March 2006
- Advisor: *Mr. Shakti Kapoor, STSM, IBM Austin*

B.Tech., Information Technology, RVR&JC College of Engineering, April 2004

Research Projects

Optimizing assignment of threads to SPEs on the Cell BE Processor
- The actual bandwidth obtained for inter-SPE communication is strongly inuenced by the assignment of threads to SPEs (thread-SPE afnity) in many realistic communication patterns.
- We identify the bottlenecks to optimal performance and use this information to determine good afnities for common communication patterns.
- Tools/programming methods used: Cell BE programming involving signals, DMAs and mailboxes, C and MPI.

Reducing the disk IO bandwidth bottleneck through fast floating point compression using sccelerators
- We proposed a compression technique based on time-series analysis, and investigate its effectiveness on floating point data from a variety of applications.
- We show that significant reduction in IO time can be achieved, even accounting for the compression overhead, on a Cell BE processor. In our experiments, the typical improvement was around 30%, varying from a slight loss in performance to a factor of seven improvement, depending on the type of application.
- Tools/programming methods used: Cell BE programming, GPU CUDA programming and C.

Topology and routing aware mapping tool for massively parallel processors
- Developed general mapping techniques by posing the hop-byte metric as a quadratic assignment problem (QAP). Rather than using the metric just for evaluation of the mapping quality, the idea is intuitive in optimizing the metric itself.
- A metric based on the idea of minimizing the number of bottleneck links, called the maximum contention metric, requires the routing information along with the topology details. We showed that our heuristics for optimizing this metric are more effective in reduction communication costs.
- Tools/programming methods used: C, C++, Cray MPI, Cray Scheduler, Python, OSU MPI benchmarks and large scale code profiler - HPC toolkit.

Design and implementation of an optimized Proc file system for a message passing operating system
- The aim is to design a process(proc) file system in the Minix OS by first understanding the implementation of it in Linux and then implement it for Minix OS running on PowerPC 405GP board.
- Tools/programming methods used: MINIX OS, PowerPC ISA and C.

Teaching Experience

Programming for Performance on multi-cores, http://progforperf.github.com
High Performance Computing with Accelerators, http://dmacssite.github.com

Parallel Computing, http://parallelcomp.github.com
Computer Organization and Design.

Journal Publications

Dynamic Load Balancing for Petascale Quantum Monte Carlo Applications: The Alias Method, **C.D. Sudheer**, S. Krishnan, A. Srinivasan, and P. R. C. Kent. Computer Physics Communciations, Feb 2013, Impact Factor : 3.268, (5-year Impact Factor: 2.812).

Conference Publications

Optimization of the Hop-Byte Metric for Effective Topology Aware Mapping, **C.D. Sudheer**, Ashok Srinivasan, Proceedings of the 19th IEEE International Conference on High Performance Computing (HiPC), 2012, (Acceptance rate: 25%).

Optimizing Assignment of Threads to SPEs of the Cell BE Processor, **C.D. Sudheer**, T. Nagaraju, P.K. Baruah, Ashok Srinivasan, 10th IEEE International Workshop on Parallel and Distributed Scientific and Engineering Computing (PDSEC), Proceedings of the 23rd International Parallel and Distributed Processing Symposium, IEEE, 2009, (Citations: SG - 5).

High Throughput Compression of Floating point numbers in GPUs, Ajith Padyana, **C.D Sudheer**, P.K. Baruah, Ashok Srinvasan, 2nd IEEE International Conference on Parallel, Distributed and Grid Computing - 2012 Himachal Pradesh, December 2012.

Investigating Algorithmic Techniques for Enhancing Application Performance on Multicore Processors, **C.D. Sudheer** (Advisor: Ashok Srinivasan), PhD Forum at IEEE International Parallel and Distributed Processing Symposium, 2009.

A Communication Model for Determining Optimal Affinity on the Cell BE processor, **C.D. Sudheer**, Sriram, S.: In: Proc. 16th IEEE International Conference on High Performance Computing (HiPC), Student Research Symposium, Dec 2009.

Invited Presentations

An Overview of the Global Arrays Toolkit, Five-days Technology Workshop on Heterogeneous Computing - Many Core/ Multi GPU - Performance of Algorithms, Application Kernels (HeMPa), 2011, at CMSD, UoHYD by C-DAC Pune & CMSD.

Programming for Performance on Cell BE processor, Performance Enhancement on Emerging Parallel Processing Platforms Workshop (PEEP), 2008, jointly organized by C-DAC and IUCAA.

Professional Service

Technical Program Committee member for the following conferences HPCC, ISPA, ICA3PP, HiPC SRS. Reviewer for Computing, Springer Journal.

Computer Access Time Grants

XSEDE Research Allocation: Scaling Communication Performance for Massively Parallel Applications, 800,000 SUs, PI: Prof. Ashok Srinivasan, Florida State University.

Technical Expertise

Experience in programming Cell BE, CUDA, OpenCL, Cilk, MPI, OpenMP and Global Arrays. Conversant with architectures ARM, Cell BE, PowerPC 405 Embedded, MIPS and x86. Familiar with the usage of massively parallel machines such as NICS Kraken and TACC Stamepede.

Academic Achievements

TCPP PhD Forum Travel Grant for attending the IPDPS 2009 conference in Italy.
Secured 96.84 percentile in Graduate Aptitude Test in Engineering (GATE-04) in CS stream.
University first rank in C programming theory and laboratory exam in the 1st year of B.Tech.

References

Prof. Ashok Srinivasan, *Florida State University* (asriniva@cs.fsu.edu)
Prof. P. Sadayappan, *Ohio State University* (saday@cse.ohio-state.edu)
Mr. Shakti Kapoor, *STSM, IBM Austin* (skapoor@us.ibm.com)
Prof. Pallav Kumar Baruah, *Sri Sathya Sai Institute of Higher Learning* (pkbaruah@sssihl.edu.in)