Sudheer Kumar

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Objective

An exciting and challenging opportunity in the field of multi-core platforms and performance optimization.

Work Experience

Assistant Professor (part-time), Department of Mathematics & Computer Science, Sri Sathya Sai Institute of Higher Learning, July 2011 - May 2013

Education

Ph.D., Computer Science, Sri Sathya Sai Institute of Higher Learning, April 2013
- Advisor: *Prof. Ashok Srinivasan, Florida State University*
- Thesis: *Topology and Routing Aware Mapping on Parallel Processors*

M.Tech., Computer Science, Sri Sathya Sai Institute of Higher Learning, March 2006
- Advisor: *Mr. Shakti Kapoor, STSM, IBM Austin*

B.Tech., Information Technology, RVR&JC College of Engineering, April 2004

Research Projects

Optimizing assignment of threads to SPEs on the Cell BE Processor
- The inter-SPE bandwidth is strongly influenced by the assignment of threads to SPEs in many realistic communication patterns.
- Identified the bottlenecks to optimal performance to determine good afnities for common communication patterns.
- Tools/programming methods used: Cell BE programming involving signals, DMAs and mailboxes, C and MPI.

Programming for Performance on multi-core processors
- To obtain the high level of performance needed in scientific computing, it is necessary for programs to exploit many of the features of modern computer architectures.
- Experimented with the performance-critical features of state-of-the-art architectures such as Intel MIC, Intel SandyBridge and AMD Opetron.

High Performance Computing with Accelerators
- Skills for designing scalable parallel programs targeting high performance on GPUs and multicores.
- Compare and contrast parallel programming style for GPUs and conventional multi-cores.

Topology and routing aware mapping tool for massively parallel processors
- Posed the hop-byte metric as a quadratic assignment problem (QAP) and optimized the metric itself.
- Our heuristics give 75% reduction in hop-bytes over the default allocation, and up to 66% reduction over existing heuristics.
- Tools/programming methods used: C, C++, Cray MPI, Cray Scheduler, Python, OSU MPI benchmarks and large scale code profiler - HPC toolkit.

Processor Architecture and its Applications
- The objective is to understand intricate details of processor system Architecture. The idea is to design and develop an instruction set simulator for a simple in-order single issue RISC processor.
- Involves designing an orthogonal ISA for a hypothetical architecture, simulation routines for pipeline functional units, assembler, physically indexed cache, and then translation.

Operating Systems Design and Implementation
- Understand the interaction between the Operating System and the Architecture. MINIX OS code for the PowerPC architecture is used.

- Various topics covered: context switching (system call interrupt), OS message passing mechanism, keyboard interrupt, Programmable Interrupt Timer interrupt, reset interrupt, Address Translation (TLB interrupt) etc.

Design and implementation of an optimized Proc file system for a message passing operating system

- The aim is to design a process(proc) file system in the Minix OS by first understanding the implementation of it in Linux and then implement it for Minix OS running on PowerPC 405GP board.

Journal Publications

Dynamic Load Balancing for Petascale Quantum Monte Carlo Applications: The Alias Method, **C.D. Sudheer**, S. Krishnan, A. Srinivasan, and P. R. C. Kent. Computer Physics Communciations, Feb 2013, Impact Factor : 3.268, (5-year Impact Factor: 2.812).

Conference Publications

Optimization of the Hop-Byte Metric for Effective Topology Aware Mapping, **C.D. Sudheer**, Ashok Srinivasan, Proceedings of the 19th IEEE International Conference on High Performance Computing (HiPC), 2012, (Acceptance rate: 25%).

Optimizing Assignment of Threads to SPEs of the Cell BE Processor, **C.D. Sudheer**, T. Nagaraju, P.K. Baruah, Ashok Srinivasan, 10th IEEE International Workshop on Parallel and Distributed Scientific and Engineering Computing (PDSEC), Proceedings of the 23rd International Parallel and Distributed Processing Symposium, IEEE, 2009, (Citations: SG - 5).

Investigating Algorithmic Techniques for Enhancing Application Performance on Multicore Processors, **C.D. Sudheer** (Advisor: Ashok Srinivasan), PhD Forum at IEEE International Parallel and Distributed Processing Symposium, 2009.

A Communication Model for Determining Optimal Affinity on the Cell BE processor, **C.D. Sudheer**, Sriram, S.: In: Proc. 16th IEEE International Conference on High Performance Computing (HiPC), Student Research Symposium, Dec 2009.

Invited Presentations

An Overview of the Global Arrays Toolkit, Five-days Technology Workshop on Heterogeneous Computing - Many Core/ Multi GPU - Performance of Algorithms, Application Kernels (HeMPa), 2011.

Programming for Performance on Cell BE processor, Performance Enhancement on Emerging Parallel Processing Platforms Workshop(PEEP), 2008.

Professional Service

Technical Program Committee member for the following conferences HPCC, ISPA, ICA3PP, HiPC SRS. Reviewer for Computing, Springer Journal.

Computer Access Time Grants

XSEDE Research Allocation: Scaling Communication Performance for Massively Parallel Applications, 800,000 SUs, PI: Prof. Ashok Srinivasan, Florida State University.

Technical Expertise

Experience in programming Cell BE, CUDA, OpenCL, Cilk, MPI, OpenMP and Global Arrays. Conversant with architectures ARM, Cell BE, PowerPC 405 Embedded, MIPS and x86. Familiar with the usage of massively parallel machines such as NICS Kraken and TACC Stamepede.

Academic Achievements

TCPP PhD Forum Travel Grant for attending the IPDPS 2009 conference in Italy.
Secured 96.84 percentile in Graduate Aptitude Test in Engineering (GATE-04) in CS stream.
University first rank in C programming theory and laboratory exam in the 1st year of B.Tech.

References

Prof. Ashok Srinivasan, *Florida State University* (asriniva@cs.fsu.edu)
Prof. P. Sadayappan, *Ohio State University* (saday@cse.ohio-state.edu)
Mr. Shakti Kapoor, *STSM, IBM Austin* (skapoor@us.ibm.com)
Prof. Pallav Kumar Baruah, *Sri Sathya Sai Institute of Higher Learning* (pkbaruah@sssihl.edu.in)