CMOS ternary logic circuits

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Indexing *terms*: Logic, Digital arithmetic, Metal-oxide-semiconductor structures

Abstract: We review the main difficulties and advantages in developing CMOS ternary circuits. In addition to employing multiple power sources and multiple thresholds, we describe a new theory of transmission functions for designing CMOS ternary logic circuits. It can explain the main CMOS ternary circuits proposed previously. Computer simulations show that the circuits based on the transmission-function theory have more desirable transfer characteristics than ones with resistors.

1 Introduction

The practical goal of multivalued logic (MVL) research is to direct the design and fabrication of multivalued circuits. In theory, multivalued circuits should enjoy the following advantages over their binary counterparts:

(a) since each wire can transmit more MVL information than binary, the number of connections inside the chip can be reduced

(b) since each MVL element can process more information than a binary element, the complexity of circuits may be decreased

(c) the connections on- and off-chip can be reduced to help alleviate the pin-out difficulties that arise with increasingly larger chips

(d) the speed of serial information transmission will be faster since the transmitted information p.u. time is increased.

However, theory also predicts several disadvantages of MVL circuits

(i) for fixed values of the highest and lowest voltages, the tolerances of circuits with more logic levels will be more critical than with binary circuits

(ii) to realise low-output impedance, additional sources of power are needed to produce the intermediate voltage outputs

(iii) the complexity of fabricating an MVL circuit may be increased since the elements in a circuit must deal with multivalued signals.

Why have we focussed on ternary CMOS circuits? Ternary and quaternary circuits have been studied increasingly in recent years. Quaternary circuits have the practical advantage that a four-valued signal can easily be transformed into a two-valued signal. However, based on the following considerations, we feel that ternary circuits may be of more theoretical significance than quaternary:

(a) since 3 is the smallest radix higher than binary, ternary functions and circuits have the simpler form and construction. They can be studied and discussed easily, yet they still display the characteristics of multivalued elements

(b) As a measure of the cost or complexity of multivalued circuits, the product of the radix and the number of signals has been proposed. Since 3 is the digit nearest to $e = 2.718$, ternary circuits will be more economical according to this measure [1]

(c) if balanced ternary logic $(1, 0, -1)$ is used, the same hardware may be used for addition and for subtraction

(d) since 3 is not an integral power of 2, research on ternary logic may disclose design techniques that are overlooked in the study of binary or quaternary logic.

CMOS integrated-circuit technology is the choice for realising ternary logic for the following reasons:

(i) CMOS multivalued circuits are expected to share three principal advantages of CMOS binary circuits: zero static power dissipation in either stable state, low-output impedance in either state and elimination of passive elements (resistors)

(ii) any multivalued signal can be transmitted through a CMOS transmission gate

(iii) in contrast with the pn-junction threshold of a bipolar transistor, the MOS transistor's threshold may easily be changed during fabrication, simplifying the task of responding to a multilevel input signal

(iv) since the first CMOS ternary circuits were proposed by Mouftah and Jordan in 1974 [2], they have received more attention than other multivalued circuits.

The standards for evaluating proposed circuit designs and the tactics used in the research should be set out in advance. The goal of research in multivalued circuits is to overcome difficulties of binary VLSI with too high density and too many connections. Therefore, we may establish the following criteria for evaluating proposed circuit designs:

(a) is the circuit suitable for VLSI implementation?

(b) are the circuit's electrical parameters competitive with its binary counterpart?

(c) can the circuit be functionally and electrically compatible with a binary circuit in a mixed-radix system?

The research tactics are

(i) to derive experience and understanding from the theory and circuit design of CMOS binary circuits

(ii) to use a suitable algebraic system as a guide for describing the function and realisation of a circuit

(iii) to evaluate a proposed circuit design using the criteria given above, and then to analyse and improve the design.

Paper 6934G (E10), first received 19th April 1988 and in revised form 12th July 1989

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2 Logic levels and traditional algebra

In a ternary system there are three logic levels (2, 1, 0) corresponding, for instance, to high, middle and low voltages (2E, E, Ground). To detect three different signal voltages, there must be two detection threshold voltages, for instance 0.5E and 1.5E, which are associated with logic levels 0.5 and 1.5, respectively.

A ternary function is ddfined by its truth table. Tables 1 and 2 show truth tables of some functions of one or two variables.

Table 1: Truth table of one-variable functions

x	$\bar{x}$	${}^0x^0$	${}^1x^1$	${}^2x^2$	$\overline{{}^2x^2}$
0	2	2	0	0	2
1	1	0	2	0	2
2	0	0	0	2	0

Table 2: Truth table of two-variable functions

x	y	$f(x, y)$	$x \wedge y$	$\overline{x \wedge y}$	$x \vee y$	$\overline{x \vee y}$
0	0	C_0	0	2	0	2
0	1	C_1	0	2	1	1
0	2	C_2	0	2	2	0
1	0	C_3	0	2	1	1
1	1	C_4	1	1	1	1
1	2	C_5	1	1	2	0
2	0	C_6	0	2	2	0
2	1	C_7	1	1	2	0
2	2	C_8	2	0	2	0

In Table 1, ${}^0x^0$, ${}^1x^1$ and ${}^2x^2$ are the binary-valued literals of variable x, $\bar{x}$ is the inverse of x and ${}^0x^0$ and $\overline{{}^2x^2}$ are called the negative and positive inverses of x, respectively. In Table 2, $x \wedge y$ and $\overline{x \wedge y}$ are the ternary AND operation (minimum) and the ternary NAND operation, and $x \vee y$ and $\overline{x \vee y}$ are the ternary OR operation (maximum) and the ternary NOR operation. In Table 2, $f(x, y)$ expresses a general form of a two-variable function, where the function value $C_i \in (0, 1, 2)$.

In a Post algebra, the literal, the AND and the OR form a complete set of operations, and $f(x, y)$ in Table 2 can be expressed in the following algebraic form:

$$\begin{aligned} f(x, y) = {} & (C_0 \wedge {}^0x^0 \wedge {}^0y^0) \vee (C_1 \wedge {}^1x^1 \wedge {}^0y^0) \\ & \vee (C_2 \wedge {}^0x^0 \wedge {}^2y^2) \vee (C_3 \wedge {}^1x^1 \wedge {}^0y^0) \\ & \vee (C_4 \wedge {}^1x^1 \wedge {}^1y^1) \vee (C_5 \wedge {}^1x^1 \wedge {}^2y^2) \\ & \vee (C_6 \wedge {}^2x^2 \wedge {}^0y^0) \vee (C_7 \wedge {}^2x^2 \wedge {}^1y^1) \\ & \vee (C_8 \wedge {}^2x^2 \wedge {}^2y^2) \end{aligned} \quad (1)$$

If the values defining 'x' (from Table 1) are changed from (2, 0) to (1, 0) and the operations A and V are replaced by modulo-3 multiplication ($\otimes$) and modulo-3 addition ($\oplus$), eqn. 1 will be transformed into a form based on a modulus algebra. Substituting other operations in eqn. 1 yields similar expansions. As long as these operations reflect the way elements act in circuits, the corresponding functional form can be fabricated into a circuit and therefore is potentially useful.

By factoring common values of C_i in eqn. 1, $f(x, y)$ can be written in the following form:

$$f(x, y) = (0 \wedge {}^0f^0) \vee (1 \wedge {}^1f^1) \vee (2 \wedge {}^2f^2) \quad (2)$$

In eqn. 2, ${}^0f^0$, ${}^1f^1$ and ${}^2f^2$ are functions with binary output (2, 0) that are mutually complementary and exclusive

$$\begin{aligned} & {}^0f^0 \vee {}^1f^1 \vee {}^2f^2 = 2 \\ & {}^0f^0 \wedge {}^1f^1 = {}^0f^0 \wedge {}^2f^2 = {}^1f^1 \wedge {}^2f^2 = 0 \end{aligned} \quad (3)$$

A detailed discussion of this algebra system can be found in many references [1].

3 CMOS ternary circuits with resistors

At least two elements with different detection thresholds, for instance 1.5 and 0.5, are needed to recognise three logic levels (2, 1, 0) of an input signal. The pair of complementary enhancement-mode MOS transistors in traditional CMOS binary circuits can handle this requirement. If the detection thresholds of the PMOS and NMOS transistors are placed at 1.5 and 0.5, respectively, both transistors will turn on for an input 1. If these detection thresholds are interchanged, both transistors will turn off for an input 1 [3].

Suppose that the threshold voltage V_{TP} of a PMOS transistor is -0.5E or -1.5E. We may represent the threshold voltage as -0.5 or -1.5, which we may call the threshold of the PMOS transistor. The threshold voltage V_{TN} of an NMOS transistor may be 0.5E or 1.5E, represented by threshold 0.5 or 1.5. As shown in Fig. 1, two kinds of ternary CMOS inverter and NAND gate may be designed [2, 4]. In Fig. 1a, all the PMOS and NMOS transistors have thresholds of -0.5 and 0.5, respectively, so that they can respond to an input signal with detection thresholds 1.5 and 0.5. In Fig. 1b, the PMOS and NMOS transistors have thresholds of -1.5 and 1.5, permitting them to respond to an input signal with detection thresholds 0.5 and 1.5. These circuits are

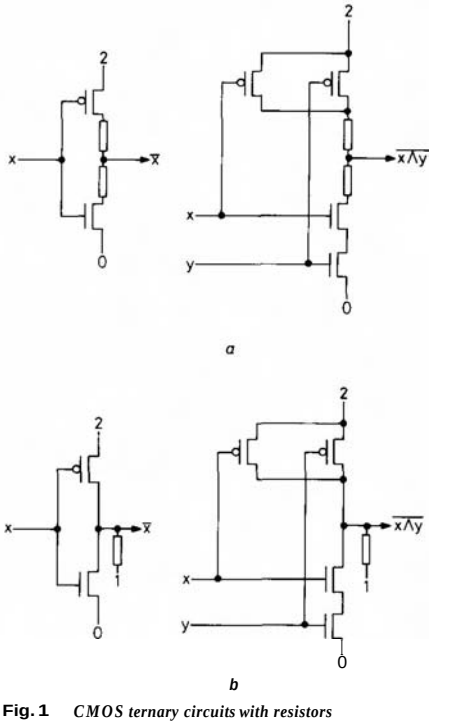

Fig. 1 *CMOS ternary circuits with resistors*
a $T_P = -0.5$, $T_N = 0.5$
b $T_P = -1.5$, $T_N = 1.5$

similar to the traditional CMOS binary inverter and NAND gate. They are ingenious and attractive.

In ternary algebra, the literal and the NAND operation form a complete set. This follows because the AND/OR form of a ternary equation such as eqn. 1 can be expressed in NAND/NAND form by the use of DeMorgan's Law: $\overline{x \vee y} = \bar{x} \wedge \bar{y}$. Consider a circuit realising a simple two-variable function defined by the ternary K-map shown in Fig. 2*a*. We may express the simplified function as

$$f(x, y) = (2 \wedge \overline{{}^2y^2}) \vee (1 \wedge {}^0x^0 \wedge {}^2y^2) \vee (0 \wedge \overline{{}^0x^0} \wedge {}^2y^2)$$

This equation has an AND/OR form, but variables x and y appear only as literals. This means that the input variables may be decoded first into binary literals, and then these binary signals may be processed using ternary gates. We had an idea to use binary circuits, about which we know a great deal, to process these binary signals to get ${}^if^i$ in eqn. 2, and then use the newer and relatively untested ternary circuits to synthesise the ternary output.

Birk and Farmer [5] proposed such a procedure: form $(2 \wedge {}^2f^2)$ and $(1 \wedge {}^1f^1)$ by weighting the power source of the last gates that realise ${}^2f^2$ and ${}^1f^1$, and then obtain the ternary output by using a ternary OR gate. The circuit realisation of function *f* in Fig. 2*a* is shown in Fig. 2*b*. Etiemble and Israel [6] proposed a general circuit construction method, illustrated in Fig. 2*c*. In this construction, a decoder transforms each ternary input into two binary signals that are then processed by a pure binary circuit, and a final encoder transforms the output of the binary circuit into the desired ternary output. For such realisation, we only need a few ternary decoders and encoders. Decoders that correspond to the two choices of threshold in Fig. 1 are shown in Figs. 2d and e, where the decimal numbers by the MOS transistors represent their thresholds. Figs. 2*f* and *g* show two forms of encoder.

The CMOS ternary circuits in Figs. 1 and 2 contain passive devices (resistors), which take up too much chip area and increase the power dissipation, output impedance and delay of the circuit. Furthermore, resistors are difficult to fabricate in a CMOS VLSI circuit, and ternary circuits containing resistors will probably fare poorly when compared with their binary equivalent.

4 CMOS ternary encoder and decoder

We can use a pair of binary signals, A and B, to convey ternary information to the inputs of a ternary encoder. From A and B we can construct ${}^0f^0$, ${}^1f^1$ and ${}^2f^2$ in three ways, as shown in the K-maps in Fig. 3*a*. In each of these three encoding schemes the 'don't care' term x is placed diagonal to a different ${}^if^i$, and we have the three sets of relationships $A = {}^1f^1$, $B = 0f^0$; $A = \overline{{}^2f^2}$, $B = \overline{{}^1f^1}$; $A = \overline{{}^2f^2}$, $B = {}^0f^0$. The required outputs may also be expressed with K-maps, as shown in Fig. 3*b*. The encoders in Figs. 2*f* and *g* conform to the third encoding scheme. However, the existence of resistors in these encoders will increase the output impedance and delay, and will decrease the load-driving capability of the output.

To eliminate the resistors and obtain better performance characteristics for these ternary circuits, three power sources (2, 1, 0) are needed instead of only two (2, 0). This leads to a consideration of multiple-powered circuits [7, 8]. McCluskey proposed all three forms of the ternary encoder, without resistors, by using an additional intermediate power source [9]. Fig. 3*c* shows these circuits.

Now let us eliminate resistors in the ternary decoders. Mouftah and Garba pointed out that altering the length-to-width ratio of the PMOS and NMOS channels can change the resistance of the channels [10]. Their circuits are shown in Fig. 4*a*. When an intermediate input signal is presented, the asymmetric resistances of the two MOS transistors will make the output either high or low, depending on the choice of circuit. This form of decoder

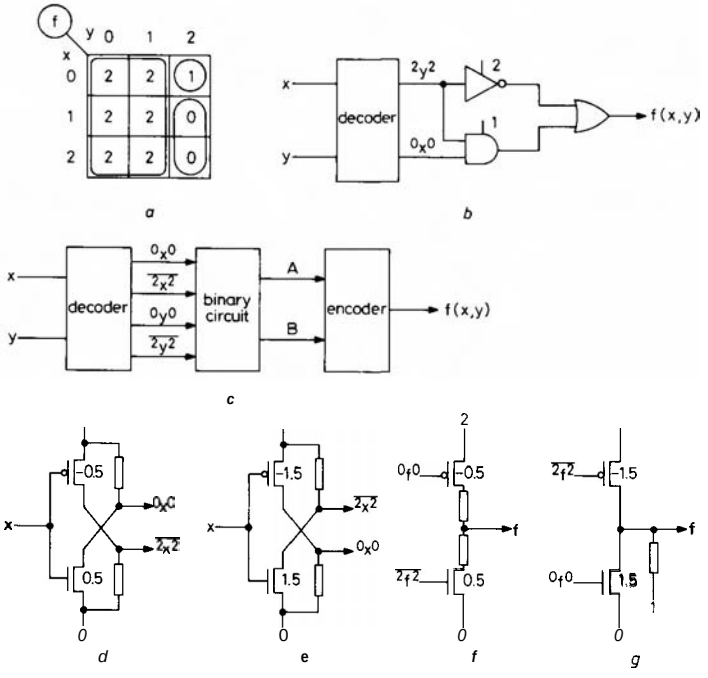

Fig. 2 *Traditional construction of ternary circuits*

a K-map expression of a two-variable ternary function
b Circuit realisation by decoding input signals and weighting power sources
c General wnstruction of ternary circuits with decoder and encoder
d Decoder with resistors
$T_P = -0.5$
$T_N = 0.5$
e Decoder with resistors
$T_P = -1.5$
$T_N = 1.5$
f Encoder with resistors
$T_P = -0.5$
$T_N = 0.5$
g Encoder with resistors
$T_P = -1.5$
$T_N = 1.5$

merges the resistors into the transistor channels. Under an intermediate input signal this decoder functions as a voltage divider rather than relying on the natural switching states of the transistors.

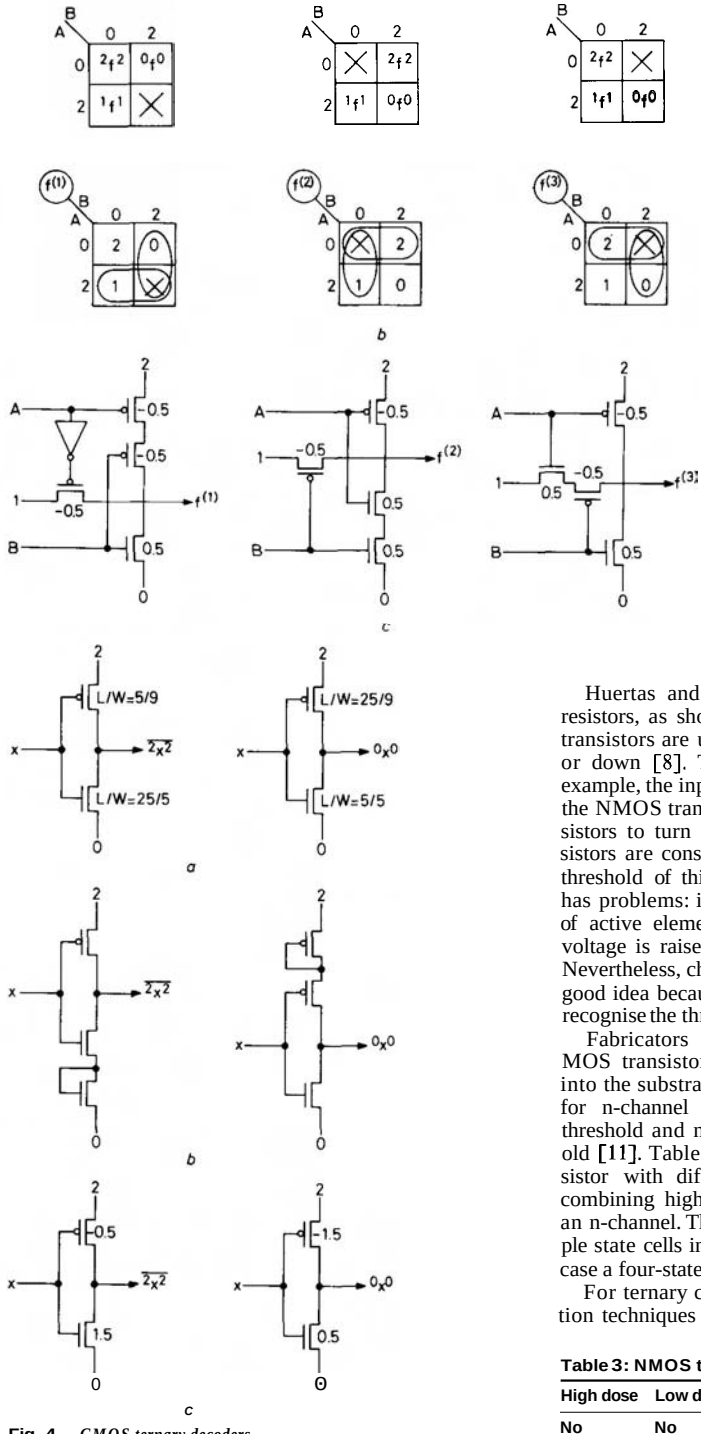

Fig. 4 *CMOS ternary decoders*
a Decoder with MOS transistors altering length-to-width ratio
b Decoder with pad MOS transistors
c Decoder with multithreshold MOS transistors

Fig. 3 *CMOS ternary encoders*
a Three encoding schemes
b K-maps of required output
c Circuit realisations of a w d e r

Huertas and Carmona proposed a decoder without resistors, as shown in Fig. ***4b,*** in which two-pad MOS transistors are used to shift their detection thresholds up or down [8]. Taking the left circuit in Fig. ***4b*** as an example, the input signal **x** must be twice the threshold of the NMOS transistor in order for these two NMOS transistors to turn on. Therefore, if these two NMOS transistors are considered to be one input element, then the threshold of this element is raised. This decoder circuit has problems: in addition to the increase in the number of active elements in the circuit, the low-level output voltage is raised, placing it near the NMOS threshold. Nevertheless, changing the threshold of a transistor is a good idea because it does provide a way for the circuit to recognise the three different input levels.

Fabricators may change the threshold voltage of a MOS transistor by implanting ions of a dopant atom into the substrate of the transistor channel. For example, for n-channel devices, p-type ions (boron) raise the threshold and n-type ions (phosphorus) lower the threshold [11]. Table 3 shows how four kinds of NMOS transistor with different thresholds can be fabricated by combining high-dose and low-dose boron implants into an n-channel. These four transistors can be used as multiple state cells in the storage matrix of a ROM, in which case a four-state ROM is formed [12].

For ternary circuits we can use multiple ion implantation techniques to make NMOS transistors with thresh-

Table 3: NMOS transistors with different thresholds

High dose	Low dose	Threshold voltage
No	No	0.7 V
No	Yes	2.2 V
Yes	No	3.2 V
Yes	Yes	4.1 V

olds 1.5 and *0.5,* and to make PMOS transistors with thresholds -1.5 and -0.5. Then a new decoder is possible, as shown in Fig. 4*c*. This decoder has ideal operational characteristics, at the expense of additional masks and implantation steps during fabrication.

Ternary encoders and decoders designed according to the above techniques meet the requirements for useful ternary circuits, at the expense of additional power sources and additional fabrication steps. However, the sandwich-like structure of the ternary circuits of Fig. 2*c* is not satisfying, since we have only surrounded the original binary circuit by new ternary crusts. Moreover, the centre binary circuit is inefficient, since its two outputs are wholly devoted to representing one ternary signal. Furthermore, the ternary crusts surrounding the binary circuit increase the number of stages in the circuit and increase the circuit's transmission delay. Such a circuit is unlikely to be viewed as superior to a pure binary circuit that realises the same function.

These undesirable properties are a result of the sandwich-like construction of the ternary circuits, but the sandwich mode seems inherent in the fabrication of the reported multivalued circuits [13] and it is difficult to avoid its effects even in the design of storage devices [14]. If we trace the cause of the sandwich-like implementations, we find that the functional form of eqn. *1* is responsible. In this form the ternary function has been expressed in terms of literals with binary outputs, which then are used in subsequent steps in the processing. The sandwich form of the resulting circuits cannot be changed as long as eqn. *1* forms the basis of expressing functions defined by truth tables.

5 Transmission functions and CMOS transmission networks

As an alternative to eqn. *1,* the function $f(x, y)$ of Table *2* may be expressed as follows, by making use of the transmission-threshold properties of MOS switching transistors [15]:

$$\begin{aligned} f(x,y) = {} & C_0 * (x^{0.5} \blacksquare y^{0.5}) \# C_1 * (x^{0.5} \blacksquare {}^{0.5}y \bullet y^{1.5}) \\ & \# C_2 * (x^{0.5} \blacksquare {}^{1.5}y) \# C_3 * ({}^{0.5}x \bullet x^{1.5} \blacksquare y^{0.5}) \\ & \# C_4 * ({}^{0.5}x \bullet x^{1.5} \blacksquare {}^{0.5}y \bullet y^{1.5}) \\ & \# C_5 * ({}^{0.5}x \bullet x^{1.5} \blacksquare {}^{1.5}y) \\ & \# C_6 * ({}^{1.5}x \bullet y^{0.5}) \# C_7 * ({}^{1.5}x \bullet {}^{0.5}y \bullet y^{1.5}) \\ & \# C_8 * ({}^{1.5}x \bullet {}^{1.5}y) \end{aligned} \tag{4}$$

Three new types of operations appear in eqn. *4*. These are defined below.

5.1 Threshold-comparison operations

$$x^t \triangleq \begin{cases} \mathrm{T} & \text{if } x < t \\ \mathrm{F} & \text{if } x > t \end{cases} \quad \text{and} \quad {}^t x \triangleq \begin{cases} \mathrm{T} & \text{if } x > t \\ \mathrm{F} & \text{if } x < t \end{cases}$$

In these definitions, the input variable $x \in (0, 1, 2)$ and the detection threshold $t \in (0.5, 1.5)$. The result x^t or ${}^t x$ is a Boolean switching value T or F rather than a ternary signal value 2 or 0 as arose in ${}^i x^i$ in eqn. *1.* The AND operator $\bullet$ and the OR operator $+$ (which does not appear in eqn. *4)* are the conventional Boolean algebraic operators. They represent switches connected in series and in parallel, respectively.

5.2 Transmission operation

$$C_i * B \triangleq \begin{cases} C_i & \text{if } B = T \\ \emptyset & \text{if } B = F \end{cases}$$

Here $C_i \in (0, 1, 2)$ is called the transmission source. When the switching variable B is true, the source C_i will be transmitted to the output. When B is false, the output is empty ($\emptyset$).

5.3 Union operation

$$C_i * B_i \# C_j * B_j \triangleq \begin{cases} C_i * B_j & \text{if } B_j = F \\ C_j * B_j & \text{if } B_i = F \end{cases}$$

If $C_i \neq C_j$ and $B_i = B_j = T$, then a voltage conflict arises between sources C_i and C_j; this condition is disallowed.

In MOS circuits, the threshold-comparison operation and the transmission operation describe physical actions of MOS transistors. The union operation represents the wiring together of the outputs of corresponding transmission branches in CMOS circuits.

Since $C_i \in (0, 1, 2)$, eqn. *4* can be factored into the form

$$f(x, y) = 0 * B_0 \# 1 * B_1 \# 2 * B_2 \tag{5}$$

where the three switching functions B_i are mutually complementary and exclusive, as in eqn. 2

$$\begin{aligned} & B_0 + B_1 + B_2 = T \\ & B_0 \bullet B_1 = B_0 \bullet B_2 = B_1 \bullet B_2 = F \end{aligned} \tag{6}$$

With these definitions, let us consider how to use MOS transistors to realise the transmission functions $C * x^t$ and $C * {}^t x$, where $C, x \in (0, 1, 2)$ and $t \in (0.5, 1.5)$. NMOS transistors conduct where the difference between the gate voltage V_G and the source voltage V_S is greater than the threshold voltage V_{T_N}: $(V_G - V_S) - V_{T_N} > 0$. PMOS transistors conduct when the difference between the gate and source voltages is less than the threshold voltage V_{T_P}: $(V_G - V_S) - V_{T_P} < 0$. Accordingly, Fig. *5* shows circuit realisations of various transmission functions. In Fig. 5*a* the inverter symbols labeled t represent the threshold t inverter, which detects a ternary input x with

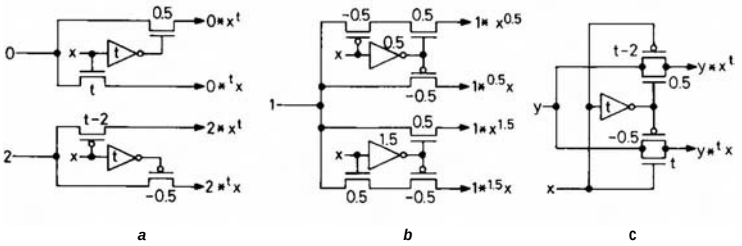

Fig. 5 ***CMOS*** **circuit realisations of transmission functions**
a Transmission functions with sources 0 and 2 b Transmission functions with source 1 c Transmission functions with variable source

detection threshold t and produces a binary output $\overline{x(t)}$. Of particular interest are the cases for thresholds 0.5 and 1.5: $\overline{x(0.5)} = {}^{0}x^{0}$ and $\overline{x(1.5)} = \overline{{}^{2}x^{2}}$. Fig. 5*b* shows two schemes to realise transmission functions $1 * x^{0.5}$ and $1 * {}^{1.5}x$. Fig. 5*c* shows how to propagate a variable source $y \in (0, 1, 2)$ using complementary MOS transmission.

Using the transmission-function algebra, we can express several functions introduced earlier in this paper; $\bar{x}$, ${}^{0}x^{0}$, and $\overline{{}^{2}x^{2}}$ from Table 1, the three encoder functions $f^{(i)}$ from Fig. 3b, function f defined in Fig. 2a and $\overline{x \wedge y}$ from Table 2

$$x = 2 * x^{0.5} \# 1 * ({}^{0.5}x \bullet x^{1.5}) \# 0 * {}^{1.5}x$$
$${}^{0}x^{0} = \overline{x(0.5)} = 2 * x^{0.5} \# 0 * {}^{0.5}x$$
$$\overline{{}^{2}x^{2}} = \overline{x(1.5)} = 2 * x^{1.5} \# 0 * {}^{1.5}x$$
$$f^{(1)} = 2 * (A^{1.5} \bullet B^{1.5}) \# 1 * {}^{0.5}A \# 0 * {}^{0.5}B$$
$$f^{(2)} = 2 * A^{1.5} \# 1 * B^{0.5} \# 0 * ({}^{0.5}A \bullet {}^{0.5}B)$$
$$f^{(3)} = 2 * A^{1.5} \# 1 * ({}^{1.5}A \bullet B^{0.5}) \# 0 * {}^{0.5}B$$
$$f = 2 * y^{1.5} \# 1 * (x^{0.5} \bullet {}^{1.5}y) \# 0 * ({}^{0.5}x \bullet {}^{1.5}y)$$
$$\overline{x \wedge y} = 2 * (x^{0.5} + y^{0.5}) \# 1 * [{}^{0.5}x \bullet {}^{0.5}y \bullet (x^{1.5} + y^{1.5})] \# 0 * ({}^{1.5}x \bullet {}^{1.5}y)$$

In the expressions for $f^{(i)}$, the detection thresholds may be selected arbitrarily as 1.5 or 0.5, since A and B are binary signals with values (2, 0).

Using the circuits in Fig. 5 to realise the transmission functions, we can establish that the circuits for $\overline{x(t)}$ and $f^{(i)}$ are the same as in Figs. 4*c* and 3*c*, respectively. Fig. 6 shows circuits that realise $\bar{x}$, f and $\overline{x \wedge y}$. Fig. 6*b* is a fully ternary circuit, containing no binary signals since the threshold-comparison operation represents a binary switching state rather than a binary signal transfer. Examples of the design of other basic CMOS ternary circuits and storage devices can be found in Reference 16; further work is in progress.

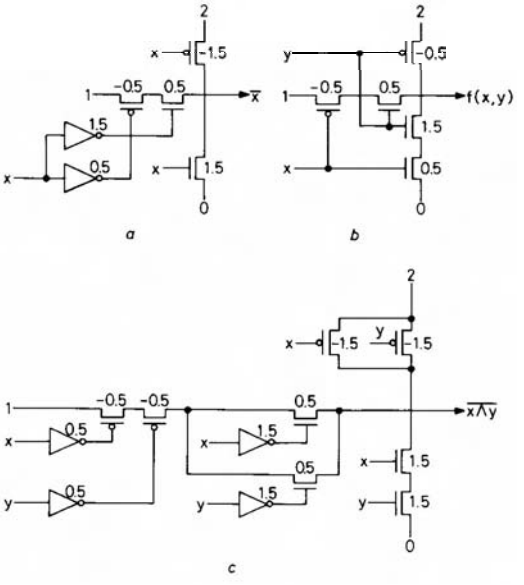

Fig. 6 *CMOS circuit realisations*

a $\bar{x}$
b $f(x, y)$ in Fig. 2*a*
c $x \wedge y$

Transmission-function theory can also explain CMOS ternary circuits that contain resistors. In eqn. 5, one of the three transmission functions B^i may be realised by a resistor R, giving a circuit with two low-impedance paths and one high-impedance path. Since the three transmission functions are mutually complementary and exclusive, the MOS transmission network will work in the following way: when one of the two nonresistive sources is transmitted to the output (with a low impedance), the source passing through the high-impedance R has no effect on the output, but when neither low-impedance source is transmitted, the source passing through R will be transmitted to the output.

If a resistor R takes the place of the more complicated branch to which source 1 is attached in Figs. 6a and c, these circuits will be the same as that in Fig. 1b. Similarly, we can derive Fig. 2*g* from the third circuit in Fig. 3*c*. These three transmission functions can be rewritten as follows:

$$\bar{x} = 2 * x^{0.5} \# 0 * {}^{1.5}x \# 1_R$$
$$\overline{x \wedge y} = 2 * (x^{0.5} + y^{0.5}) \# 0 * ({}^{1.5}x \bullet {}^{1.5}y) \# 1_R$$
$$f^{(3)} = 2 * A^t \# 0 * {}^tB \# 1_R \quad t \in \{0.5, 1.5\}$$

The technique of replacing a branch of a circuit with a resistor can also be applied to a two-source MOS transmission network. If R substitutes for an NMOS transistor, a PMOS circuit family is formed, and if R substitutes for a PMOS transistor, an NMOS circuit family is formed. For example, the circuits in Figs. 2d and e can be derived from the circuits in Fig. 4*c*.

In the above discussion, if the circuits are not in a state that is transmitting source 2 or source 0, then the circuits are transmitting source 1. There is another approach which eliminates voltage source 1: to create an output at the medial voltage of source 1, we may simultaneously transmit both source 2 and source 0 instead of source 1 to the output through two balanced voltage-division resistors. Again using the functions $\bar{x}$, $\overline{x \wedge y}$ and $f^{(3)}$ as examples, we may write transmission-function expressions that do not require source 1

$$\bar{x} = 2_R * x^{1.5} \# 0_R * {}^{0.5}x$$
$$\overline{x \wedge y} = 2_R * (x^{1.5} + y^{1.5}) \# 0_R * ({}^{0.5}x \bullet {}^{0.5}y)$$
$$f^{(3)} = 2_R * B^t \# 0_R * {}^tA \quad t \in \{0.5, 1.5\}$$

The circuits corresponding to these expressions are the same ones shown in Figs. 1a and 2*f*. The preceding discussion shows that the proposed transmission-function theory can explain previous CMOS ternary circuits that contain resistors. Although the circuits with resistors look simpler, their electrical parameters and characteristics are not desirable. SPICE2G5 has been used to simulate CMOS ternary circuits. Taking 5 V and 2.5 V as the high- and middle-voltage sources in the ternary circuits, a part of model parameters of NMOS and PMOS transistors used in SPICE simulations are listed in Table 4, where T_N and T_P represent thresholds of NMOS and PMOS transistors, respectively [15].

DC transfer characteristics of two kinds of ternary inverter with resistors and the inverter in Fig. 6a are shown in Fig. 7. Obviously, Fig. 7a and b are not desirable because of the existence of resistors. In Fig. 7*c*, the voltages corresponding to detection thresholds 0.5 and 1.5 are 1.25 V and 3.75 V, respectively. In comparison

Table 4: SPICE2G5 parameters

	NMOS				PMOS		
T	VTO, V	μ_o, cm²/V/s	W, μm	T_p	VTO, V	μ_o, cm²/V/s	W, μm
0.5	0.8	560	25	−0.5	−3.3	200	55
1.5	3.3	330	35	−1.5	−0.8	130	85

Channel length $L = 10\ \mu m$
Oxide thickness $TOX = 0.07\ \mu m$

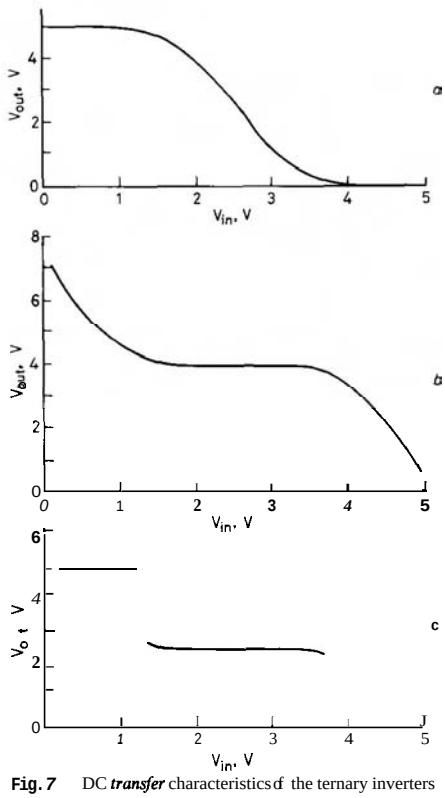

Fig. 7 DC *transfer* characteristics of the ternary inverters
Temperature = 27°C
a Inverter in Fig. 1*a* With two resistors
b Inverter in Fig. 1*b* With one resistor
c Inverter in Fig. 6*a*

with the conventional binary inverter, the DC transfer curve has two different outputs and shows only a single detection threshold. It means that ternary gates have greater capability for processing signals than binary ones.

6 Conclusions

Based on briefly reviewing the research progress of CMOS ternary circuits, the transmission-function theory is introduced in this paper. After proposing three operations (threshold-comparison operation, transmission operation and union operation), the expression of transmission function and the corresponding CMOS circuit realisation are discussed. The result of the threshold-comparison operation is Boolean switching value T or F rather than the highest and lowest ternary signal value 2 or 0, as in other references that conform to the switching function of MOS transistors, and it avoids a sandwich-like structure of the ternary circuits. This paper shows that the new circuit design can explain the main CMOS ternary circuits proposed previously. We think that the transmission-function theory proposed in this paper, used in an environment with multiple power sources and multiple threshold, provides another step toward making practical CMOS multivalued circuits. The major advantage of using multiple ion implant technique is that the size of a ternary MOS transistor is same as a binary one [12]. Therefore, the silicon areas necessary for ternary MOS devices are not larger than conventional binary ones using the same fabrication geometries. This means that a reduction in silicon area is possible for ternary circuits when processing given information.

The procedure for designing CMOS ternary combinational circuits can be used to construct CMOS ternary sequential circuit [16]. Besides, the discussion in this paper can be extended to a higher radix, and can be used to design the traditional CMOS binary circuits as well.

7 Acknowledgment

This work is part of a project supported by NSFC.

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