TOPIC 6

MEMORY AND I/O INTERFACING

MEMORY INTERFACING

i. External ROM (program memory) Interfacing

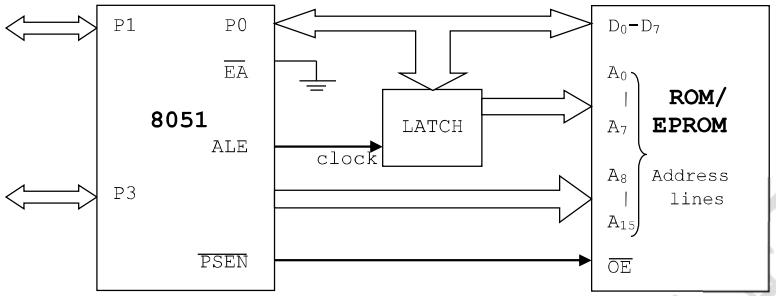

FIGURE 1 INTERFACING OF ROM/EPROM TO µC 8051.

above figure shows how to access or interface ROM to 8051.
port 0 is used as multiplexed data & address lines.
it gives lower order (A_7-A_0) 8 bit address in initial T cycle & higher order (A_8-A_{15}) used as data bus.
8 bit address is latched using external latch & ALE signal from 8051.
port 2 provides higher order (A_{15}-A_8) 8 bit address.
PSEN is used to activate the output enable signal of external ROM/EPROM.

ii. External RAM (data memory) Interfacing

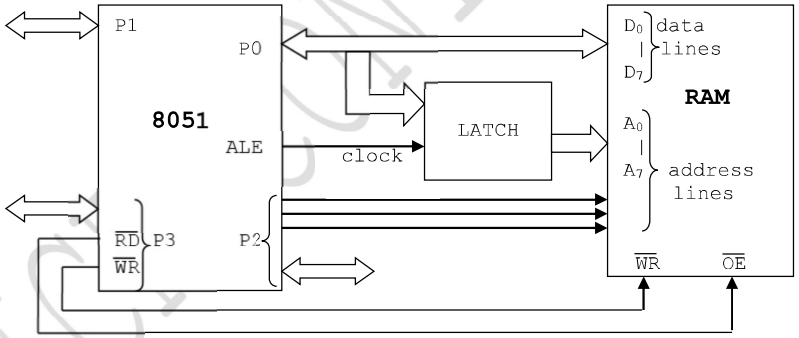

FIGURE 2 INTERFACING OF RAM(DATA MEMORY) TO µC 8051.

above figure shows how to connect or interface external RAM(data memory) to 8051.
port 0 is used as multiplexed data & address lines.
address lines are decoded using external latch & ALE signal from 8051 to provide lower order (A7-A0) address lines.
port 2 gives higher order address lines.
RD & WR signals from 8051 selects the memory read & memory write operations respectively.

RD & WR signals: generally P3.6 & P3.7 pins of port 3 are used to generate meamory read and memory write signals.
remaining pins of port 3 i.e. P3.0-P3.5 can be used for other functions.

LINEAR AND ABSOLUTE DECODING

i. Absolute Decoding

all higher address lines : decoded to select memory chip for specific logic levels.

for other logic levels memory chip is disabled.

generally used in large memory systems.

figure below shows memory interfacing using absolute decoding.

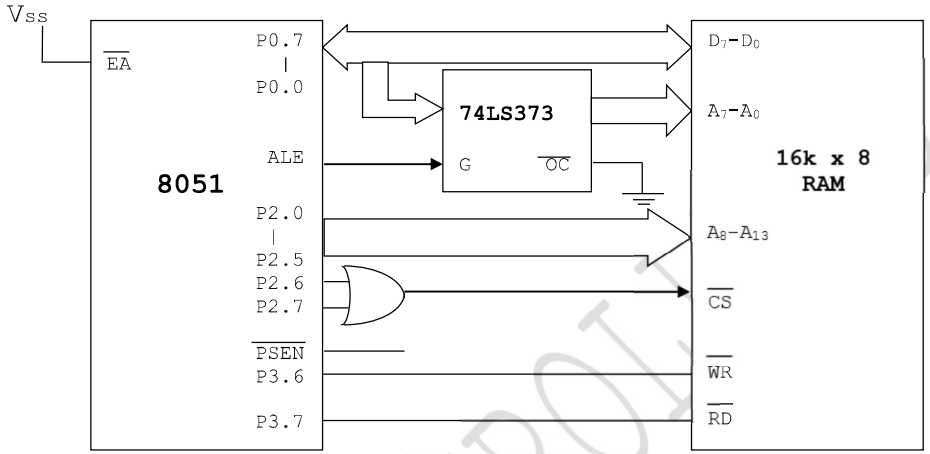

FIGURE 3 MEMORY (RAM) INTERFACING USING ABSOLUTE DECODING.

ii. Linear Decoding (Partial Decoding)

for small systems : individual higher order address lines used to select memory chip.

replacing the hardware by decoding logic.

reducing the cost of decoding, drawback is- multiple addresses.

as shown in figure below, A_{14} line is directly connected to chip select line, A_{15} line not connected anywhere, kept open.

so, status of A_{15}- not considered for generation of chip select signal.

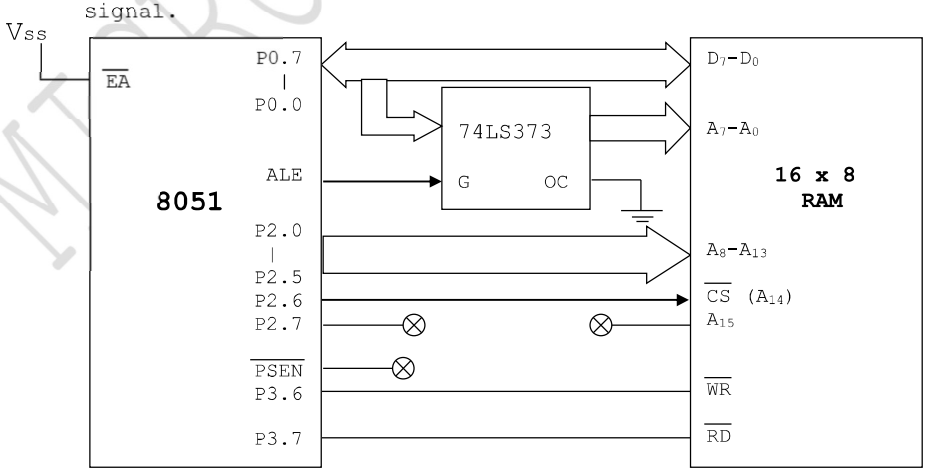

FIGURE 4 MEMORY (RAM) INTERFACING USING LINEAR DECODING.

Address Mapping(Memory Map)

i. Absolute Decoding

Address	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	HEX adrs.
starting	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
end	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	3FFFH

ii. Linear Decoding

Address	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	HEX adrs.
starting	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
end	x	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	3FFFH

Comparison between Full address(Absolute) & Partial address (Linear) Decoding.

Full Adress(Absolute) Decoding	Partial Address(Linear Decoding
i. all higher address lines are decoded to select memory or I/O device.	i. few or individual address lines are decoded to select memory or I/O device.
ii. more hardware : decoding logic.	ii. less hardware : decoding logic. (sometimes none.)
iii. decoding circuit : higher cost.	iii. decoding circuit : less cost.
iv. No multiple addresses.	iv. multiple addresses possible.
v. used in large systems.	v. used in small systems.

Solved Examples:

Example 1: Design a µController system using 8051.Interface the external RAM of size 16k x 8.

Solution: Given, Memory size: 16k

that means we require 2^n=16k :: n address lines

here n=14 :: A_0 to A_{13} address lines are required.

A_{14} and A_{15} are connected through OR gate to CS pin of external RAM.

when A_{14} and A_{15} both are low (logic '0'), external data memory(RAM) is selected.

Address Decoding(Memory Map)for 16k x 8 RAM.

Address	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	HEX adrs.
starting	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
end	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	3FFFH

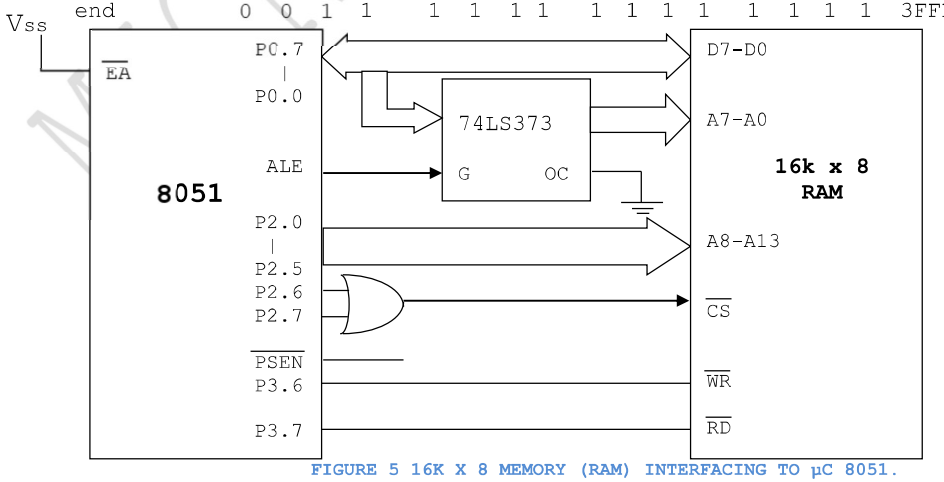

FIGURE 5 16K X 8 MEMORY (RAM) INTERFACING TO µC 8051.

Example 2: Design a µController system using 8051.Interface the external ROM of size 4k x 8.

Solution: Given, Memory size: 4k

that means we require 2^n=4k :: n address lines

here n=12 :: A_0 to A_{11} address lines are required.

remaining lines A_0, A_0, A_0, A_0 & PSEN are connected though OR gate to CS & RD of external ROM.

when A_0 to A_0 are low (logic '0'), only then external ROM is selected.

Address Decoding(Memory Map)for 4k x 8 RAM.

Address	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	HEX adrs.
starting	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
end	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0FFFH

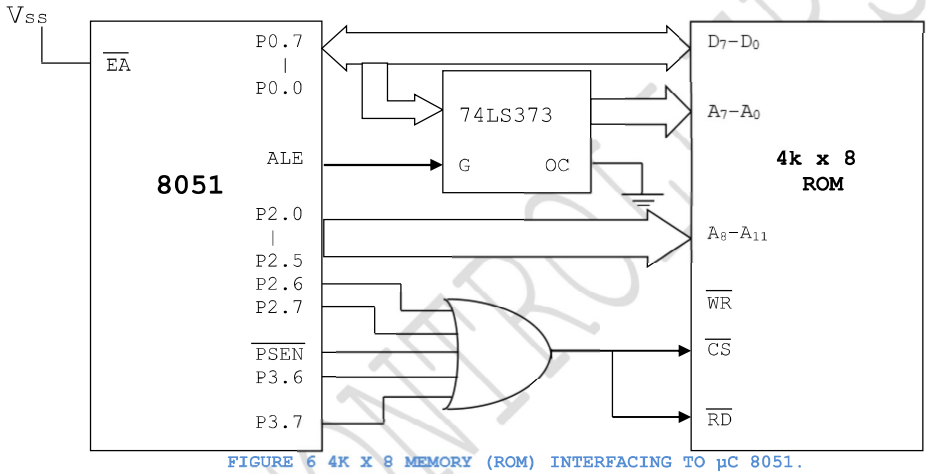

FIGURE 6 4K X 8 MEMORY (ROM) INTERFACING TO µC 8051.

Example 3: Design a µController system using 8051, 16k bytes of ROM & 32k bytes of RAM. Interface the memory such that starting address for ROM is 0000H & RAM is 8000H.

Solution: Given, Memory size- ROM : 16k

that means we require 2^n=16k :: n address lines

here n=14 :: A_0 to A_{13} address lines are required.

A14,A15,PSEN ⟶ ORed ⟶ $\overline{CS}$

when low - ROM is selected.

Memory size- RAM :32k

that means we require 2^n=32k :: n address lines

here n=15 :: A_0 to A_{15} address lines are required.

A15 ⟶ inverted(NOT Gate) ⟶ $\overline{CS}$

when high- RAM is selected.

$\overline{PSEN}$ is used as chip select pin ROM.

$\overline{RD}$ is used as read control signal pin.

$\overline{WR}$ is used as write control signal pin.

for RAM selection.

Address Decoding(Memory Map)for 16k x 8 ROM.

Address	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	HEX adrs.
starting	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
end	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	3FFFH

Address Decoding(Memory Map)for 32k x 8 RAM.

Address	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	HEX adrs.
starting	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8000H
end	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFFH

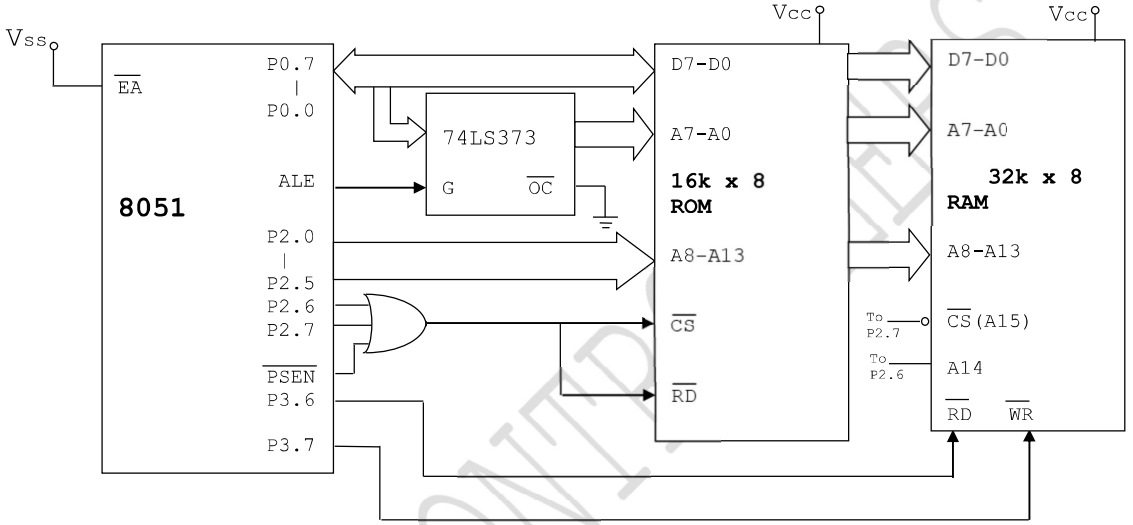

FIGURE 7 16K X 8 ROM AND 32K X 8 RAM INTERFACING TO µC 8051.

Example 4: Design a µController system using 8051, 8k bytes of program ROM & 8k bytes of data RAM. Interface the memory such that starting address for ROM is 0000H & RAM is E000H.

Solution: Given, Memory size- ROM : 8k

that means we require 2^n=8k :: n address lines

here n=13 :: A_0 to A_{12} address lines are required.

A13,A14,A15,PSEN → ORed → $\overline{CS}$

when low - program ROM is selected.

Memory size- RAM :8k

that means we require 2^n=8k :: n address lines

here n=13 :: A_0 to A_{12} address lines are required.

A13,A14,A15 → NANDed → $\overline{CS}$

when high- data RAM is selected.

$\overline{PSEN}$ is used as chip select pin ROM.
$\overline{RD}$ is used as read control signal pin.
$\overline{WR}$ is used as write control signal pin.

for RAM selection.

Address Decoding(Memory Map)for 8k x 8 ROM.

Address	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	HEX adrs.
starting	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
end	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1FFFH

Address Decoding(Memory Map)for 8k x 8 RAM.

Address	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	HEX adrs.
starting	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	E000H
end	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFFH

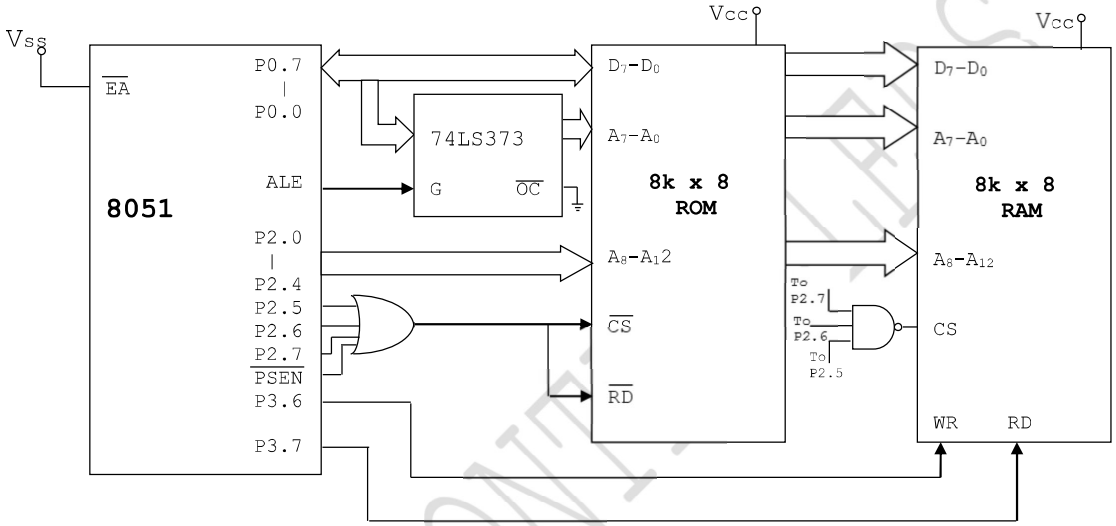

FIGURE 8 8K X 8 ROM AND 8K X 8 RAM INTERFACING TO µC 8051.