Microcontroller 8051
Memory Interfacing

Program and Data Memory

- The program and data memories of 8051 family are logically separated.
- Logical separation means they can be accessed separately with the same addresses
- 8051 can address up to 128K of memory which includes 64K of program memory & 64K of data memory.
- data memory is controlled by the special function register called data pointer (DPTR).
- Input ports P0 & P2 are used as address and data bus for external memory interfacing.
- The control signals used for external memory interfacing are PSEN', EA', ALE, RD'& WR'

Program and Data Memory

- The total memory is 64K with address range 0000H to FFFFH.
- Low on EA' indicates external memory for the whole address range.
- When external memory is used, PSEN' (Program Store Enable) signal is used to read the data.
- High value of EA' signal indicates 4K on chip i.e. internal memory is used. If required external memory can also be connected with it
- data memory is read & write memory
- 8051 has 256 byte of internal RAM from 00 to FFH.
- External RAM can be connected with address range of 64K from 0000H to FFFFH.
- when external RAM is used, RD' & WR' signals are used for reading and writing from external RAM.

External memory interfacing

Signals and ports are used for External memory interfacing:

- Port P0 is used as multiplexed address data bus AD0 -AD7,
- Port P2 is used as higher order address bus A8-A15.
- Control signal ALE (address latch Enable) is used to De-multiplex address data bus of Port P0
- EA’ indicates external access, it is made low when External ROM is used
- PSEN’ (Program Store Enable) is used for reading External ROM
- RD’ & WR’ are used with external RAM for reading & writing

Port P0 & P2

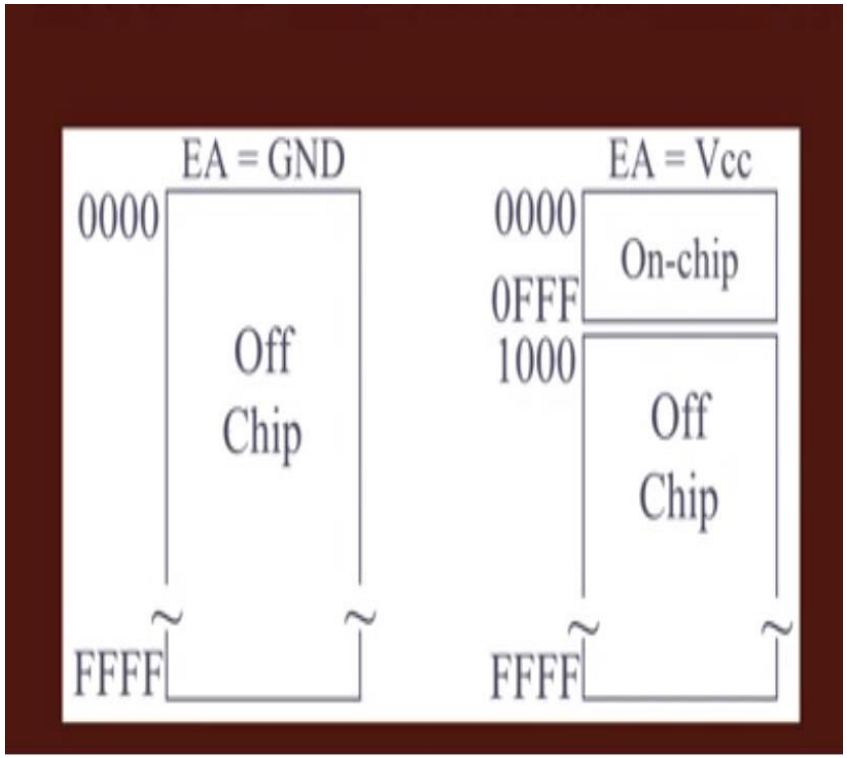
- In 8051, port P0 and port P2 provide the 16-bit address to access external memory A0-A15
- P0 provides the lower 8 bit address A0-A7 and P2 provides the upper 8 bit address A8-A15.
- Total 16 bit address results in 2^16 =64K memory space
- 64K Data Memory & 64 K Code Memory as both uses different control signals
- Port P0 has multiplexed address data line, it gives 8 bit address & 8 Bit data bus
- ALE pin De-multiplexes address /data bus.

ALE(Address Latch Enable)

- ALE stands for Address Latch Enable
- It is output pin and is active high.
- When connecting 8051 to external memory, ALE is used in conjunction with port P0
- The ALE pin is used for de-multiplexing the address and data lines
- Lets see how we demultiplex address/data bus
- When ALE is '0', we have data on port P0
- and when ALE is '1', we have address on the port P0

EA (External Access)

- EA', stands for "External Access”
- EA' is an input pin and must be connected to either VCC or GND. In other words, it cannot be left unconnected
- When it is connected to GND, it is to indicate that external ROM is connected to 8051. Thus whole address range 0000H to FFFFH is given to external ROM.
- When this pin is connected to VCC, internal ROM is used from 0000H to 0FFFH, it is used either alone or in conjunction with external ROM.

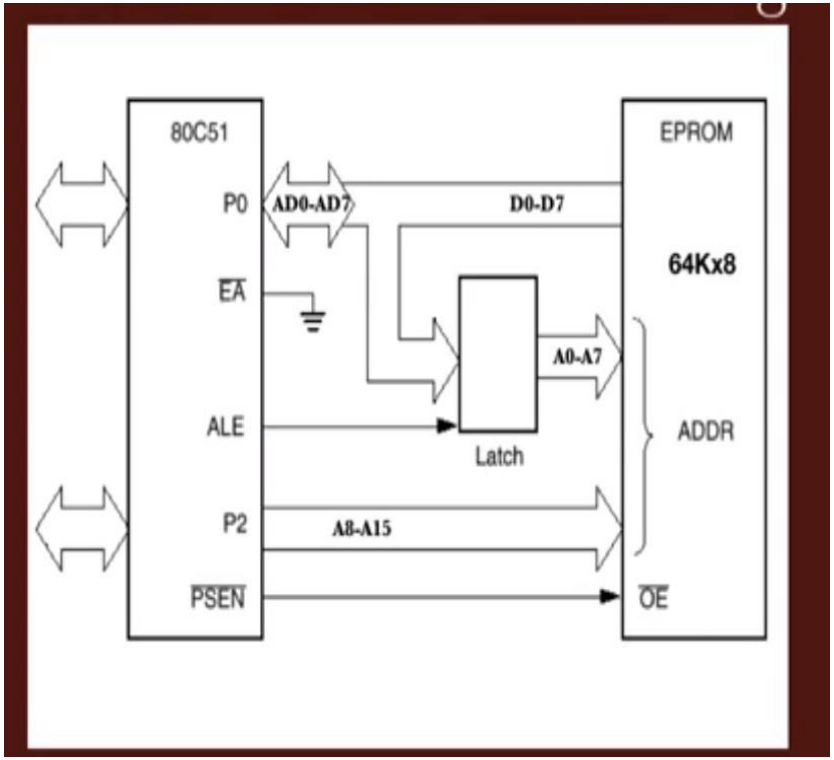


PSEN (Program Store Enable)

- PSEN' is a output pin and stands for "Program Store Enable
- When external ROM holds the program code, it is used with EA' Pin
- This pin is connected to the OE' (output Enable) pin of the ROM for reading purpose.

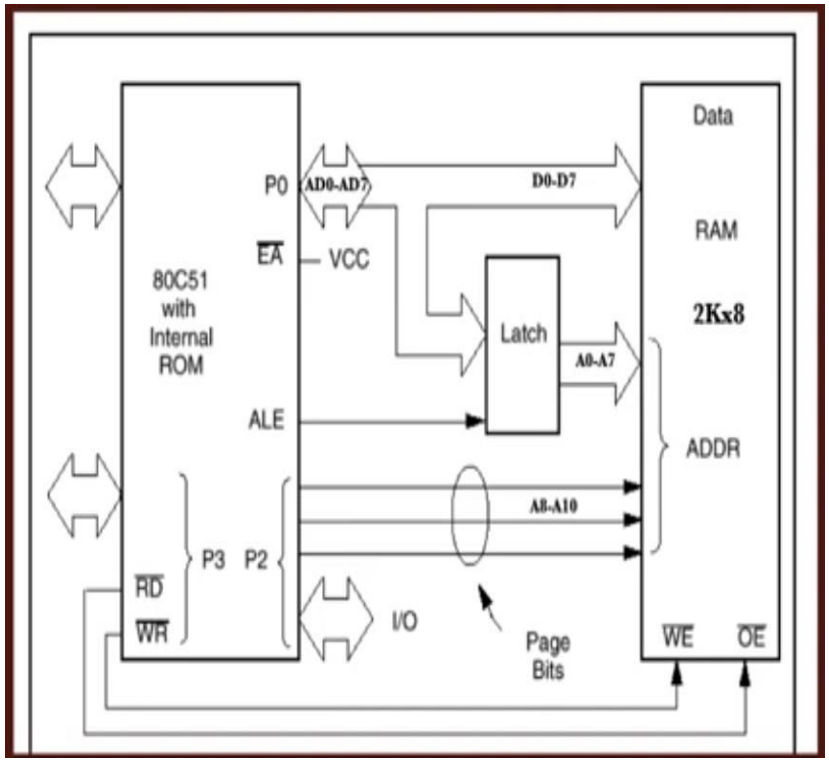
How External ROM is connected to 8051?

- This is a 64K ROM to be connected to 8051
- EA' is tied low as shown in the diagram
- Port P0 is used as multiplexed address data bus AD0-AD7 to access external ROM
- AD0-AD7 is connected to a Latch with latch enable signal as ALE
- When ALE goes high, these lines have address on it so address is latched and connected to ROM
- D0-D7 are directly connected to EPROM
- Port P2 as higher order address bus A8-A15
- PSEN' is used for reading of external ROM so it is connected to OE' of the memory IC



How External RAM is connected to 8051?

- Port P0 is used as multiplexed address & data bus,
- P2 are used as higher order address
- DPTR register saves the address of the RAM i.e. it acts as memory pointer.
- RAM size is 2K, it requires 11 address lines 2^11=2K i.e. A0-A10
- A0-A7 are connected as before using port P0, High ALE will latch the address
- Only three lines of port2 A8-A10 used with this RAM .
- Remaining line of P2 can be used as I/O Lines.
- Port P3 are used for reading & writing from RAM.
- Two pins of P3, RD' & WR' are used for reading and writing of RAM



The difference between ROM & RAM

- For accessing DATA from ROM, MOV instruction is used and MOVX is used with RAM
- In ROM, PSEN’ is used and EA’ is low whereas in RAM, EA’ is high and RD’ & WR’ are used

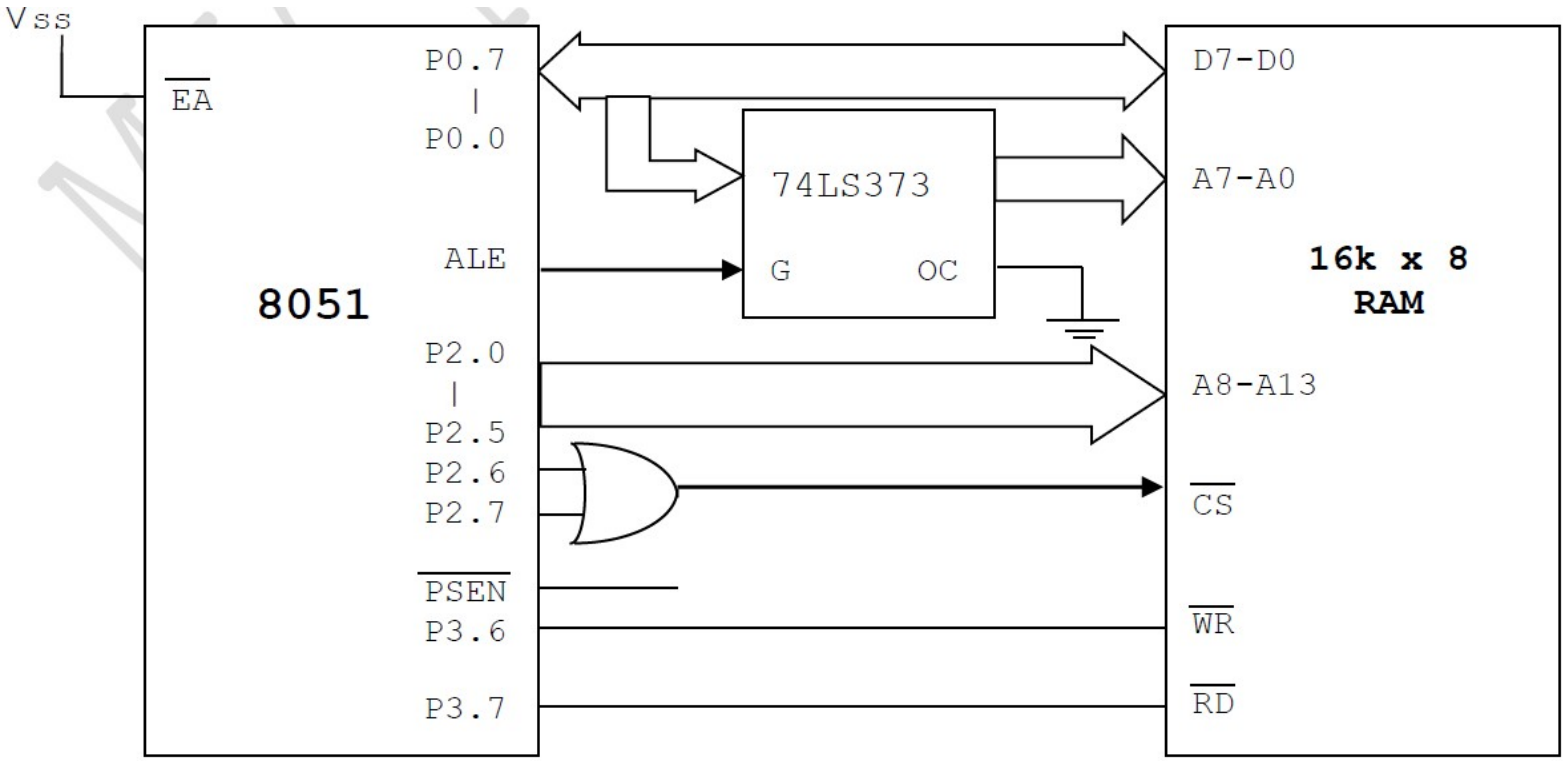
Exercise-1

Design a µController system using 8051.Interface the external RAM of size 16k x 8.

Solution:

- Given, Memory size: 16k that means we require 2n=16k :: n address lines, here n=14 :: A0 to A13 address lines are required.
- A14 and A15 are connected through OR gate to CS pin of external RAM.
- when A14 and A15 both are low (logic '0'), external data memory(RAM) is selected.
- Address Decoding(Memory Map)for 16k x 8 RAM.

	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
Starting Address	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0000 H**
Ending Address	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	**3FFF H**

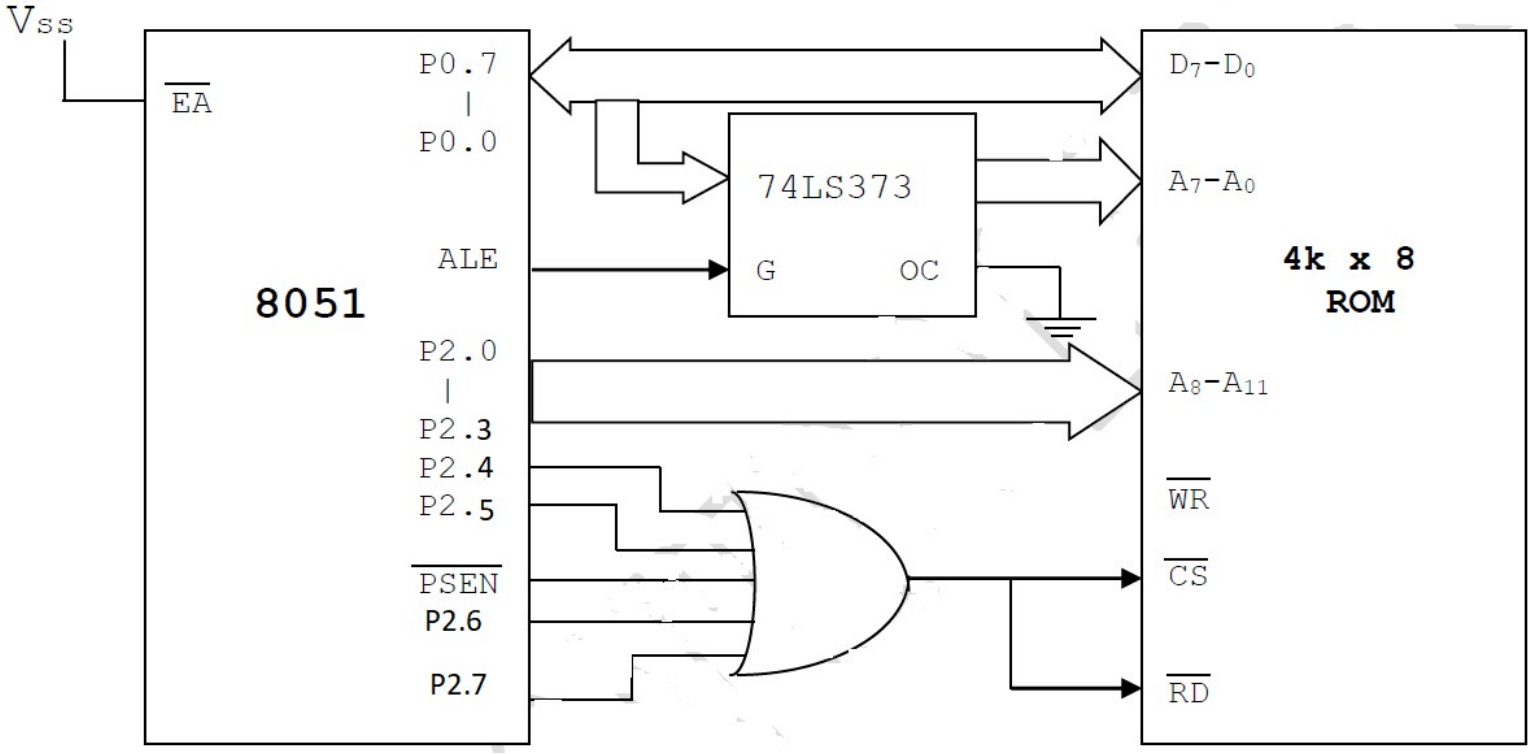

Vss
EA
P0.7
P0.0
ALE
8051
P2.0
P2.5
P2.6
P2.7
PSEN
P3.6
P3.7
74LS373
G
OC
D7-D0
A7-A0
16k x 8
RAM
A8-A13
CS
WR
RD

Design a µController system using 8051.Interface the external ROM of size 4k x 8.

Solution: Given, Memory size: 4k

- that means we require 2n=4k :: n address lines
- here n=12 :: A0 to A11 address lines are required.
- remaining lines A12, A13, A14, A15 & PSEN are connected though OR gate to CS & RD of external ROM.
- when A12 to A15 are low (logic '0'), only then external ROM is selected.
- Address Decoding(Memory Map)for 4k x 8 RAM.

	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
Starting Address	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0000 H**
Ending Address	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	**0FFF H**


Vss
EA
P0.7
|
P0.0
ALE
8051
P2.0
|
P2.3
P2.4
P2.5
PSEN
P2.6
P2.7
74LS373
G
OC
D7-D0
A7-A0
4k x 8
ROM
A8-A11
WR
CS
RD

Design a µController system using 8051, 16k bytes of ROM & 32k bytes of RAM. Interface the memory such that starting address for ROM is 0000H & RAM is 8000H.

Solution: Given, Memory size- ROM : 16k
that means we require 2^n=16k :: n address lines
here n=14 : A_0 to A_{13} address lines are required.

A14, A15, PSEN ⟶ ORed ⟶ $\overline{CS}$

when low – ROM is selected.

Memory size- RAM :32k
that means we require 2^n=32k :: n address lines
here n=15 :: A_0 to A_{14} address lines are required.

A15 ⟶ inverted (NOT Gate) ⟶ $\overline{CS}$

when high- RAM is selected.

$\overline{PSEN}$ is used as chip select pin ROM.
$\overline{RD}$ is used as read control signal pin.
$\overline{WR}$ is used as write control signal pin.

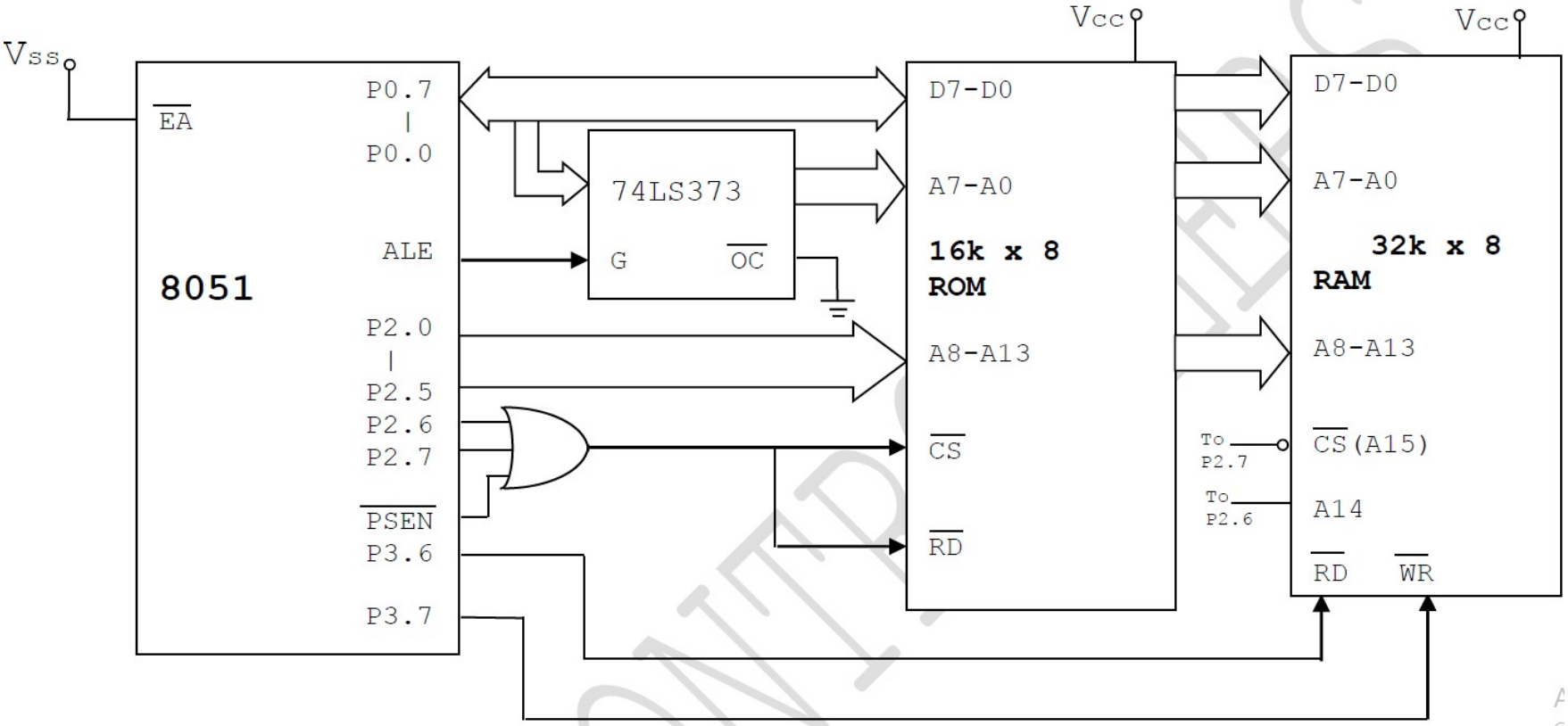
for RAM selection.

Address Decoding(Memory Map)for 16k x 8 ROM.

Address	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	HEX adrs.
starting	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
end	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	3FFFH

Address Decoding(Memory Map)for 32k x 8 RAM.

Address	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	HEX adrs.
starting	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8000H
end	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFFH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G
OC
Vcc
D7-D0
A7-A0
16k x 8
ROM
A8-A13
CS
RD
Vcc
D7-D0
A7-A0
32k x 8
RAM
A8-A13
CS (A15)
To P2.7
To P2.6
A14
RD
WR

Design a µController system using 8051, 8k bytes of program ROM & 8k bytes of data RAM. Interface the memory such that starting address for ROM is 0000H & RAM is E000H.

Solution: Given, Memory size- ROM : 8k
that means we require 2^n=8k :: n address lines
here n=13 :: A_0 to A_{12} address lines are required.

A13,A14,A15,PSEN → ORed → $\overline{CS}$

when low - program ROM is selected.

Memory size- RAM :8k
that means we require 2^n=8k :: n address lines
here n=13 :: A_0 to A_{12} address lines are required.

A13,A14,A15 → NANDed → $\overline{CS}$

when high- data RAM is selected.

$\overline{PSEN}$ is used as chip select pin ROM.
$\overline{RD}$ is used as read control signal pin.
$\overline{WR}$ is used as write control signal pin.

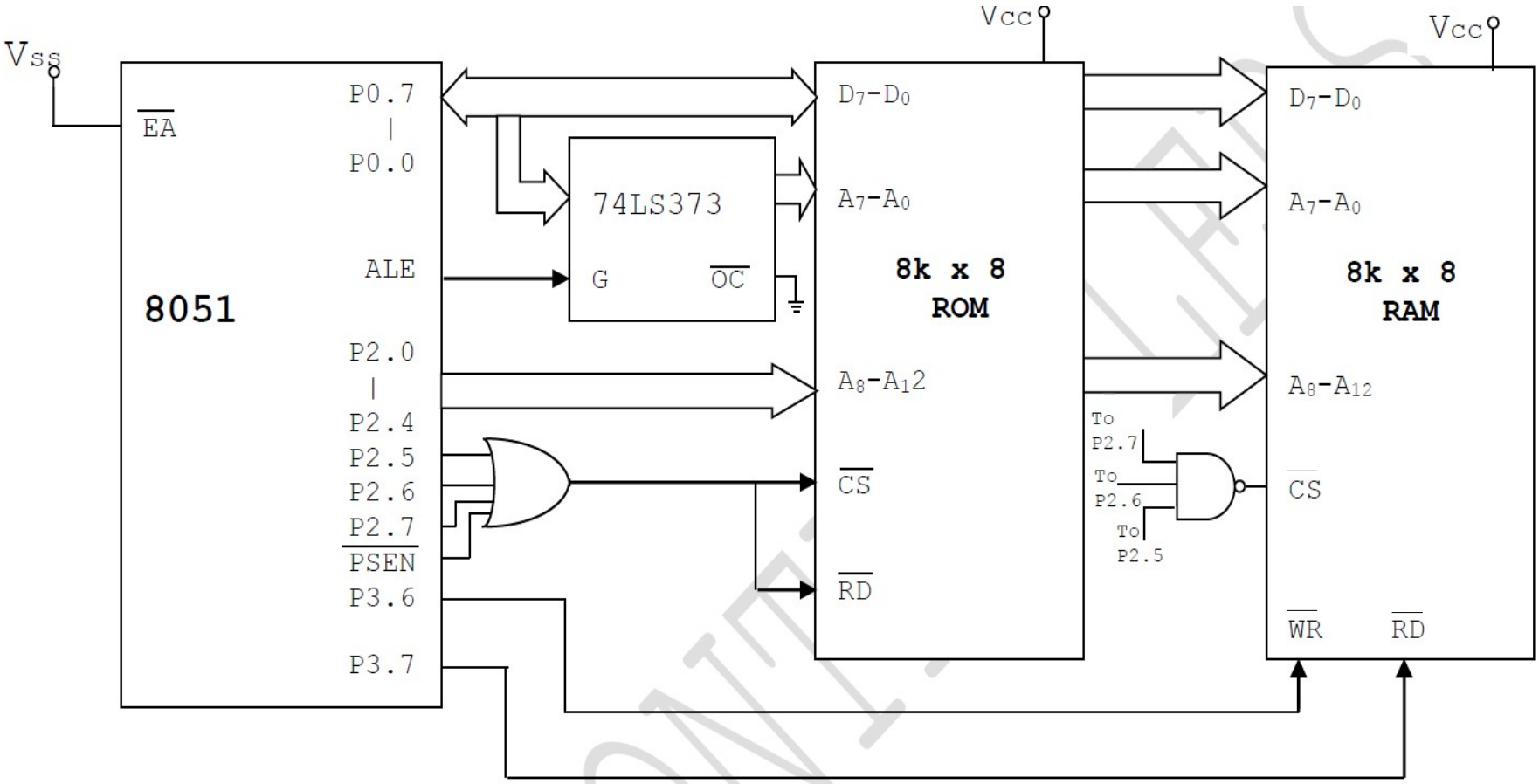
for RAM selection.

Address Decoding(Memory Map)for 8k x 8 ROM.

Address	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	HEX adrs.
starting	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
end	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1FFFH

Address Decoding(Memory Map)for 8k x 8 RAM.

Address	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	HEX adrs.
starting	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	E000H
end	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFFH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Vcc
D7-D0
A7-A0
8k x 8
ROM
A8-A12
CS
RD
To
P2.7
To
P2.6
To
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Vcc
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