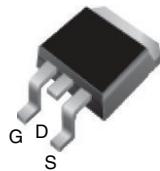
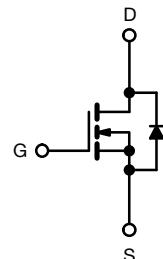


## Power MOSFET

D<sup>2</sup>PAK (TO-263)


N-Channel MOSFET



### FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dV/dt rating
- Logic-level gate drive
- R<sub>DS(on)</sub> specified at V<sub>GS</sub> = 4 V and 5 V
- 175 °C operating temperature
- Fast switching
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS\***  
Available

**HALOGEN  
FREE**

Available

### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D<sup>2</sup>PAK (TO-263) is a surface-mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D<sup>2</sup>PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

### PRODUCT SUMMARY

V <sub>DS</sub> (V)	60	
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 5.0 V	0.028
Q <sub>g</sub> (Max.) (nC)	66	
Q <sub>gs</sub> (nC)	12	
Q <sub>gd</sub> (nC)	43	
Configuration	Single	

### ORDERING INFORMATION

Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHLZ44S-GE3	SiHLZ44STRR-GE3 <sup>a</sup>
Lead (Pb)-free	IRLZ44SPbF	IRLZ44STRRPbFa

#### Note

a. See device orientation

### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	60	V
Gate-Source Voltage	V <sub>GS</sub>	± 10	
Continuous Drain Current <sup>f</sup>	I <sub>D</sub>	50	A
Continuous Drain Current		36	
Pulsed Drain Current <sup>a</sup>	I <sub>DM</sub>	200	W/°C
Linear Derating Factor		1.0	
Linear Derating Factor (PCB Mount) <sup>e</sup>		0.025	
Single Pulse Avalanche Energy <sup>b</sup>	E <sub>AS</sub>	400	mJ
Maximum Power Dissipation	P <sub>D</sub>	150	W
Maximum Power Dissipation (PCB Mount) <sup>e</sup>		3.7	
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature) <sup>d</sup>	For 10 s	300 <sup>d</sup>	

#### Notes

b. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

c. V<sub>DD</sub> = 25 V, starting T<sub>J</sub> = 25 °C, L = 179 μH, R<sub>G</sub> = 25 Ω, I<sub>AS</sub> = 51 A (see fig. 12)

d. I<sub>SD</sub> ≤ 51 A, dI/dt ≤ 250 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 175 °C

e. 1.6 mm from case

f. When mounted on 1" square PCB (FR-4 or G-10 material)

g. Current limited by the package, (die current = 51 A)

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	40	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.0	

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material)

**SPECIFICATIONS ( $T_J = 25 \text{ }^{\circ}\text{C}$ , unless otherwise noted)**

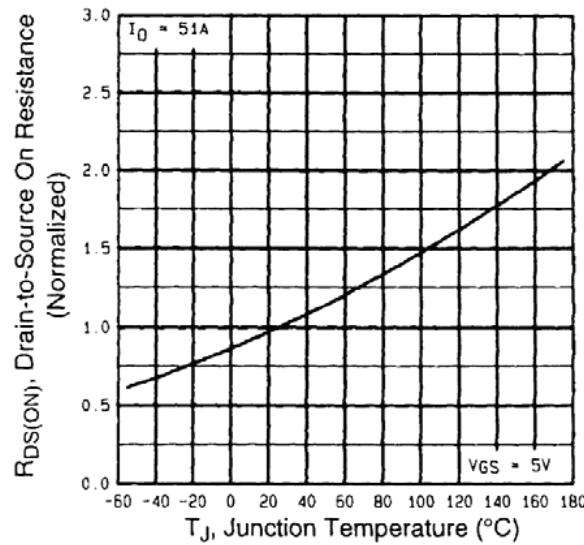
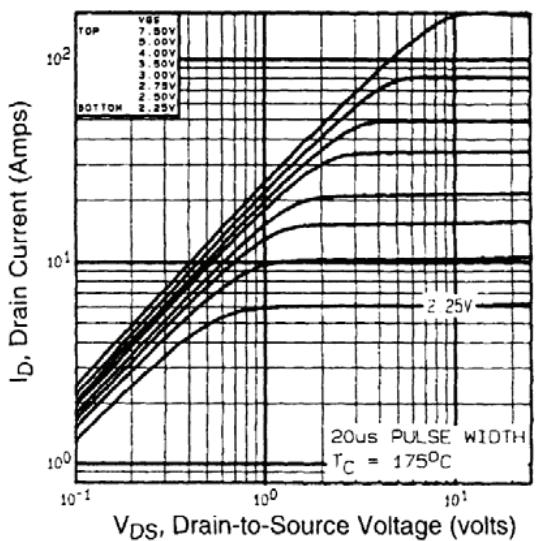
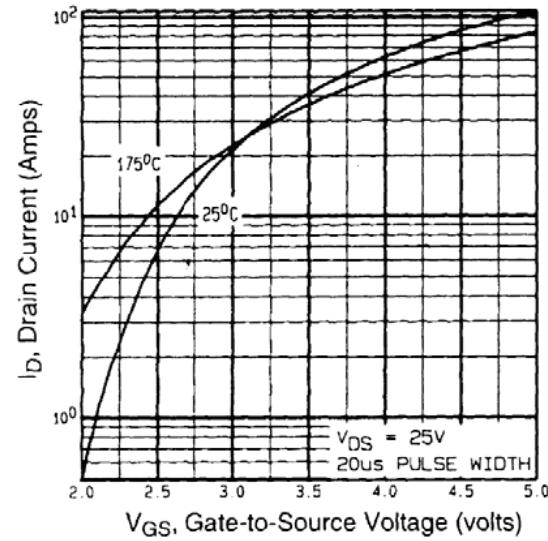
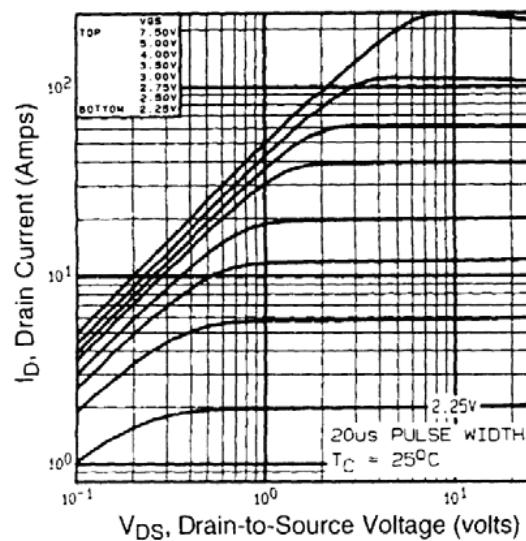
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
<b>Static</b>								
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0$ , $I_D = 250 \mu\text{A}$		60	-	-	V	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25 \text{ }^{\circ}\text{C}$ , $I_D = 1 \text{ mA}$		-	0.070	-	$\text{V}/^{\circ}\text{C}$	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$		1.0	-	2.0	V	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 10 \text{ V}$		-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60 \text{ V}$ , $V_{GS} = 0 \text{ V}$		-	-	25	$\mu\text{A}$	
		$V_{DS} = 48 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 150 \text{ }^{\circ}\text{C}$		-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 5.0 \text{ V}$	$I_D = 31 \text{ A}^b$	-	-	0.028	$\Omega$	
		$V_{GS} = 4.0 \text{ V}$	$I_D = 25 \text{ A}^b$	-	-	0.039		
Forward Transconductance	$g_{fs}$	$V_{DS} = 25 \text{ V}$ , $I_D = 31 \text{ A}^b$		23	-	-	S	
<b>Dynamic</b>								
Input Capacitance	$C_{iss}$	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 25 \text{ V}$ , $f = 1.0 \text{ MHz}$ , see fig. 5		-	3300	-	pF	
Output Capacitance	$C_{oss}$			-	1200	-		
Reverse Transfer Capacitance	$C_{rss}$			-	200	-		
Total Gate Charge	$Q_g$	$V_{GS} = 5.0 \text{ V}$	$I_D = 51 \text{ A}$ , $V_{DS} = 48 \text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	66	nC	
Gate-Source Charge	$Q_{gs}$			-	-	12		
Gate-Drain Charge	$Q_{gd}$			-	-	43		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30 \text{ V}$ , $I_D = 51 \text{ A}$ , $R_g = 4.6 \Omega$ , $R_D = 0.56 \Omega$ , see fig. 10 <sup>b</sup>		-	17	-	ns	
Rise Time	$t_r$			-	230	-		
Turn-Off Delay Time	$t_{d(off)}$			-	42	-		
Fall Time	$t_f$			-	110	-		
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH	
Internal Source Inductance	$L_S$			-	7.5	-		
<b>Drain-Source Body Diode Characteristics</b>								
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	50 <sup>c</sup>	A	
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	200		
Body Diode Voltage	$V_{SD}$	$T_J = 25 \text{ }^{\circ}\text{C}$ , $I_S = 51 \text{ A}$ , $V_{GS} = 0 \text{ V}^b$		-	-	2.5	V	
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25 \text{ }^{\circ}\text{C}$ , $I_F = 51 \text{ A}$ , $dI/dt = 100 \text{ A}/\mu\text{s}^b$		-	130	180	ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.84	1.3	$\mu\text{C}$	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )						

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width  $\leq 300 \mu\text{s}$ ; duty cycle  $\leq 2 \%$ 

c. Current limited by the package, (Die Current = 51 A)

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)


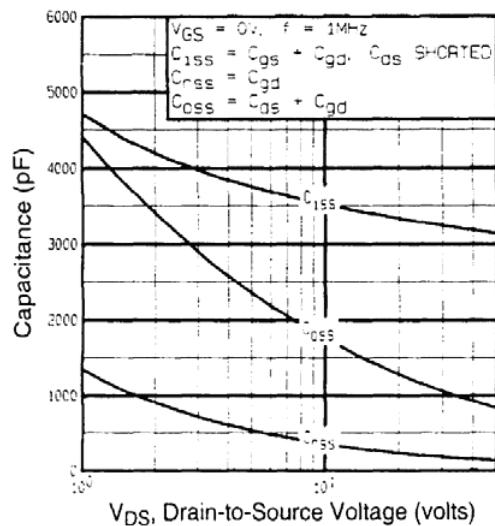


Fig. 4 - Typical Capacitance vs. Drain-to-Source Voltage

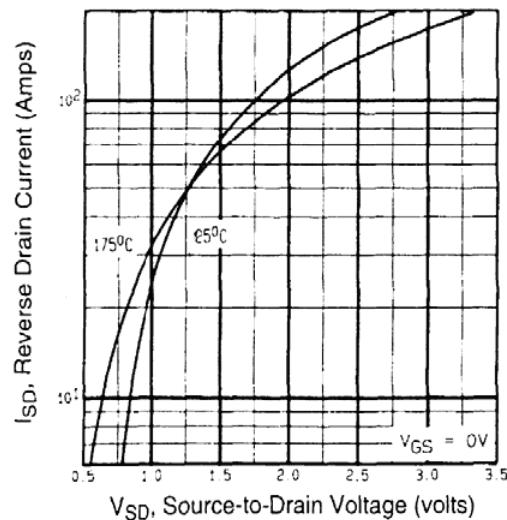


Fig. 6 - Typical Source-Drain Diode Forward Voltage

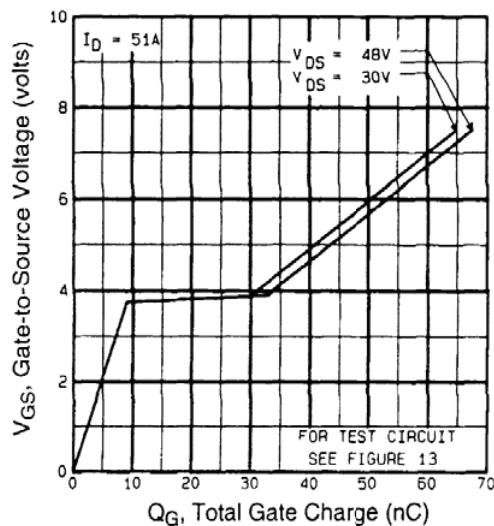


Fig. 5 - Typical Gate Charge vs. Gate-to-Source Voltage

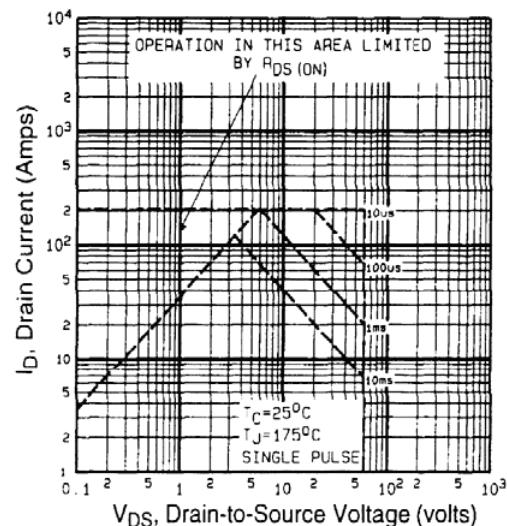


Fig. 7 - Maximum Safe Operating Area

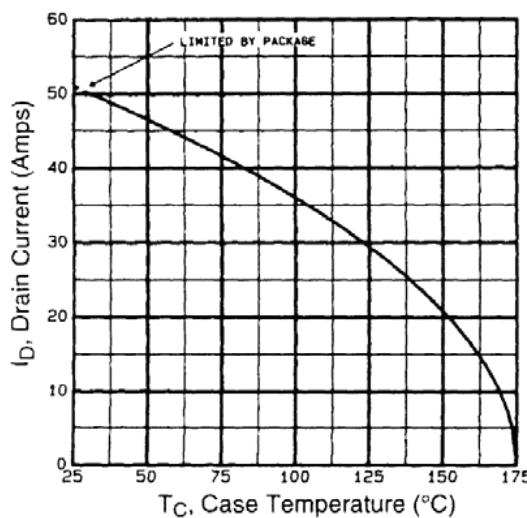


Fig. 8 - Maximum Drain Current vs. Case Temperature

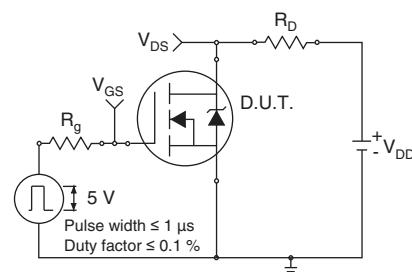


Fig. 10a - Switching Time Test Circuit

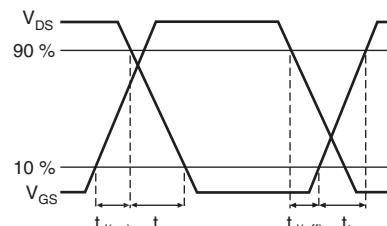


Fig. 10b - Switching Time Waveforms

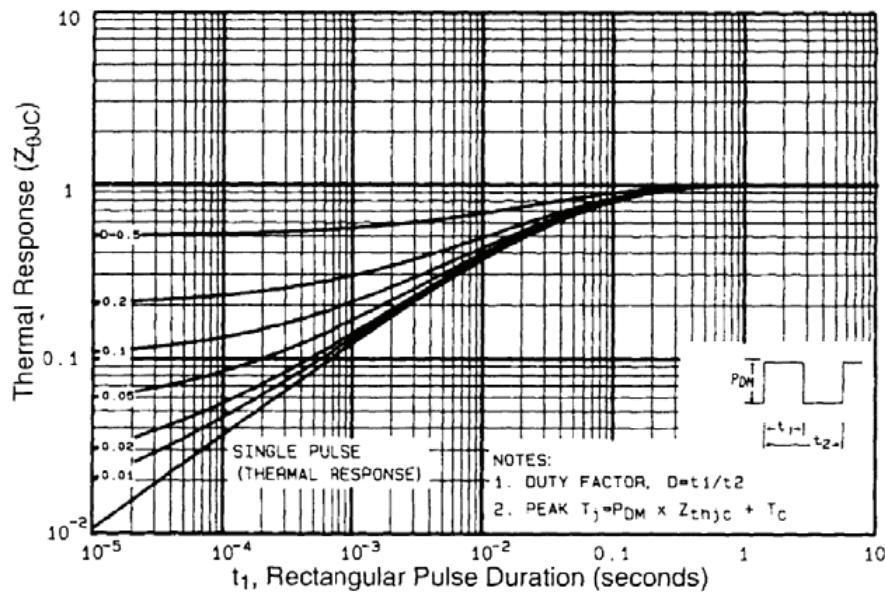
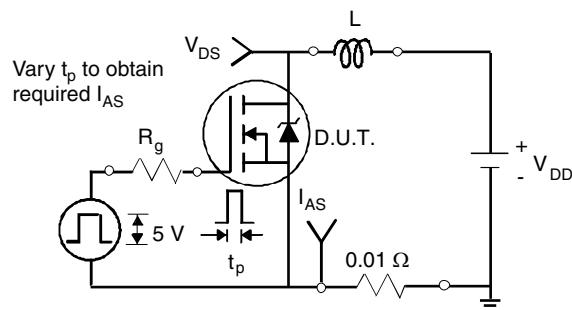
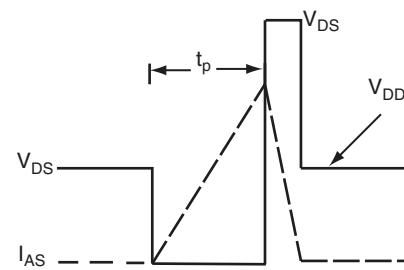


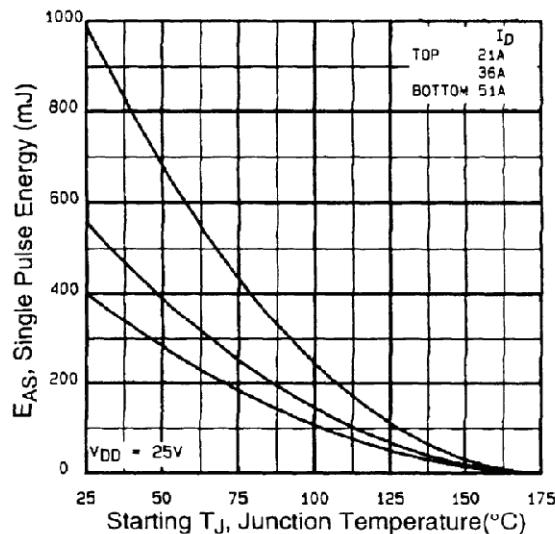
Fig. 9 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



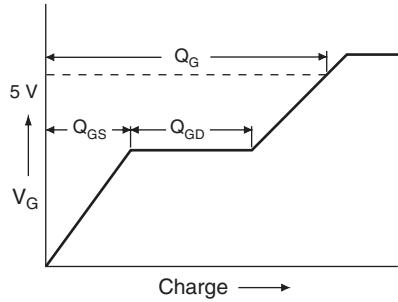
**Fig. 12a - Unclamped Inductive Test Circuit**



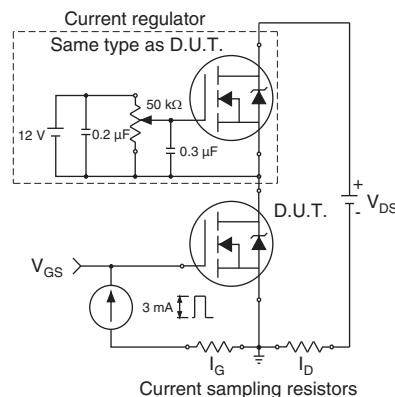
**Fig. 12b - Unclamped Inductive Waveforms**



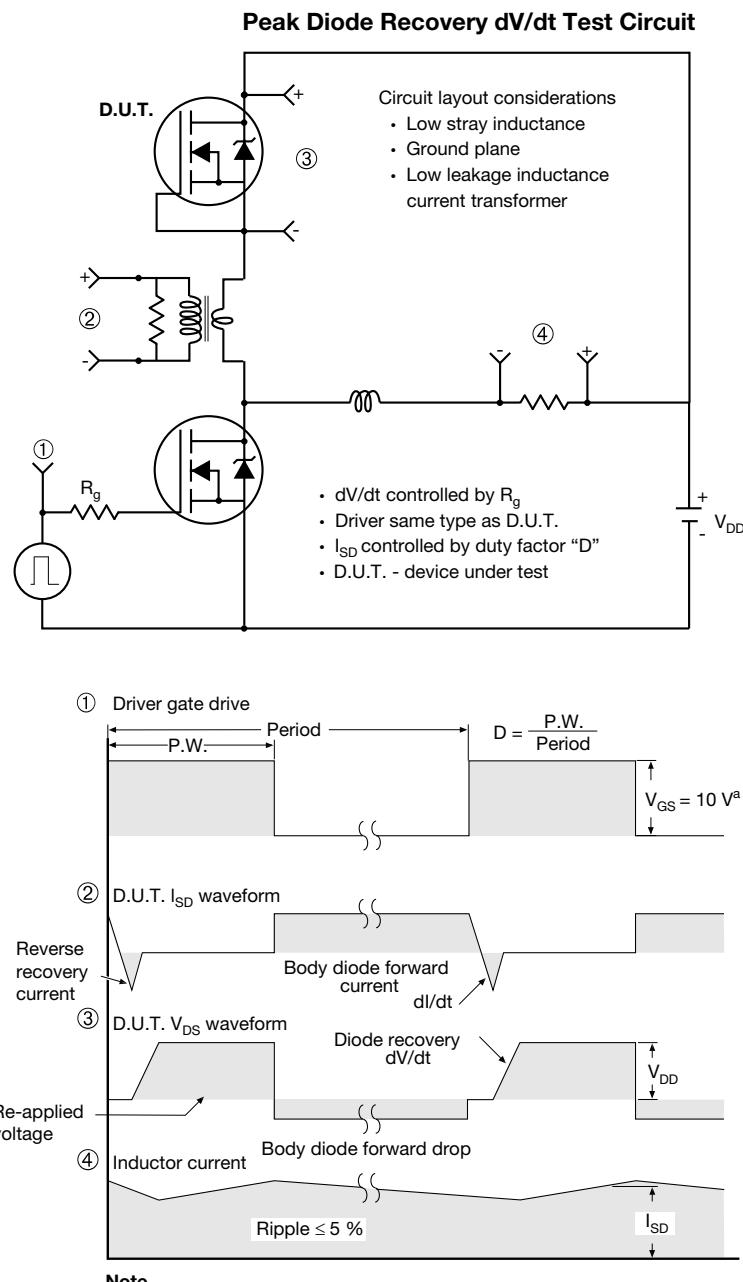
**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**



**Fig. 13a - Basic Gate Charge Waveform**

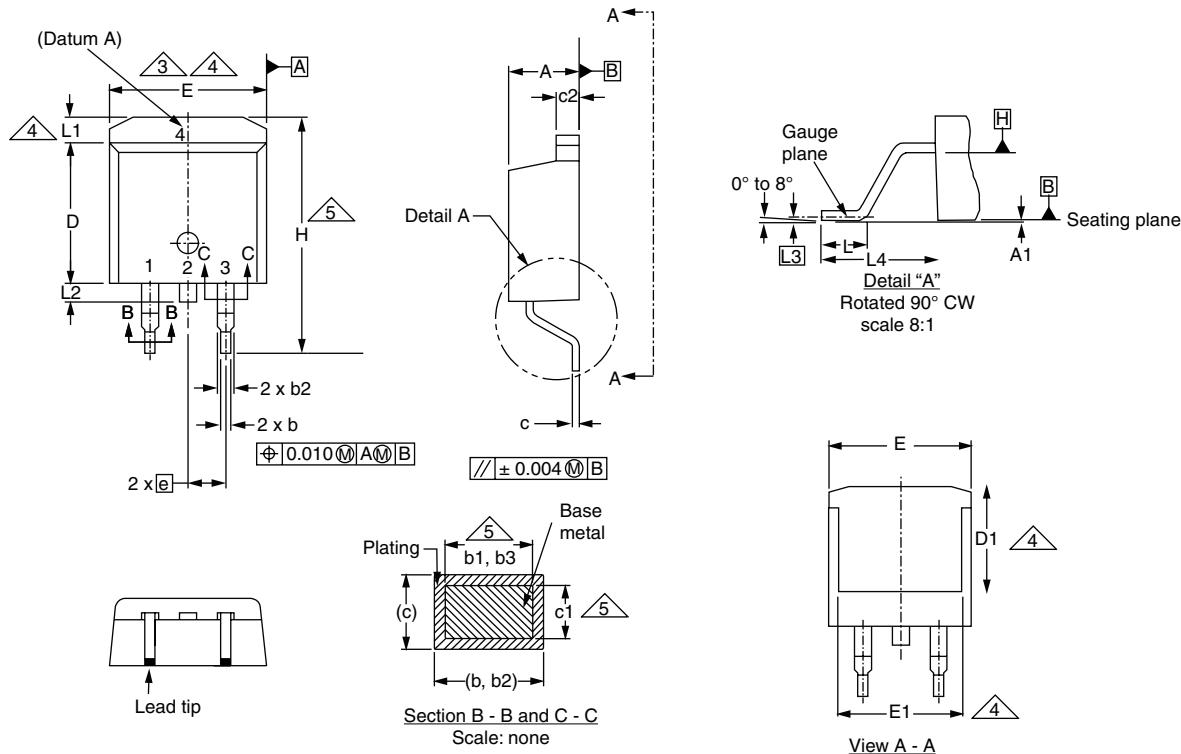


**Fig. 13b - Gate Charge Test Circuit**


**Fig. 10 - For N-Channel**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?91329](http://www.vishay.com/ppg?91329).

### TO-263AB (HIGH VOLTAGE)

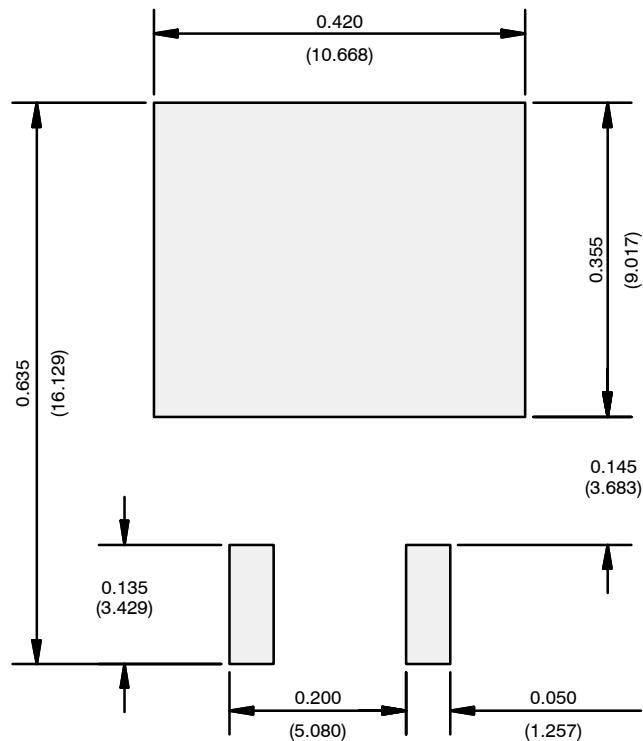


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

ECN: S-82110-Rev. A, 15-Sep-08  
DWG: 5970

#### Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994.
- Dimensions are shown in millimeters (inches).
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
- Thermal PAD contour optional within dimension E, L1, D1 and E1.
- Dimension b1 and c1 apply to base metal only.
- Datum A and B to be determined at datum plane H.
- Outline conforms to JEDEC outline to TO-263AB.

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**

Recommended Minimum Pads  
Dimensions in Inches/(mm)

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