

ALL PROGRAMMABLE



5G Wireless • Embedded Vision • Industrial IoT • Cloud Computing



KCU105 Software Install and Board Setup

June 2017

XTP352

Revision History

Date	Version	Description
06/20/17	11.0	Updated for 2017.2.
04/19/17	10.0	Updated for 2017.1.
12/19/16	9.0	Updated for 2016.4.
10/13/16	8.0	Updated for 2016.3.
06/08/16	7.0	Updated for 2016.2.
04/13/16	6.0	Updated for 2016.1
11/24/15	5.0	Updated for 2015.4.
10/06/15	4.0	Updated for 2015.3.
06/30/15	3.0	Updated for 2015.2.
04/30/15	2.0	Updated for 2015.1.
03/06/15	1.0	Initial version. Added AR63771.

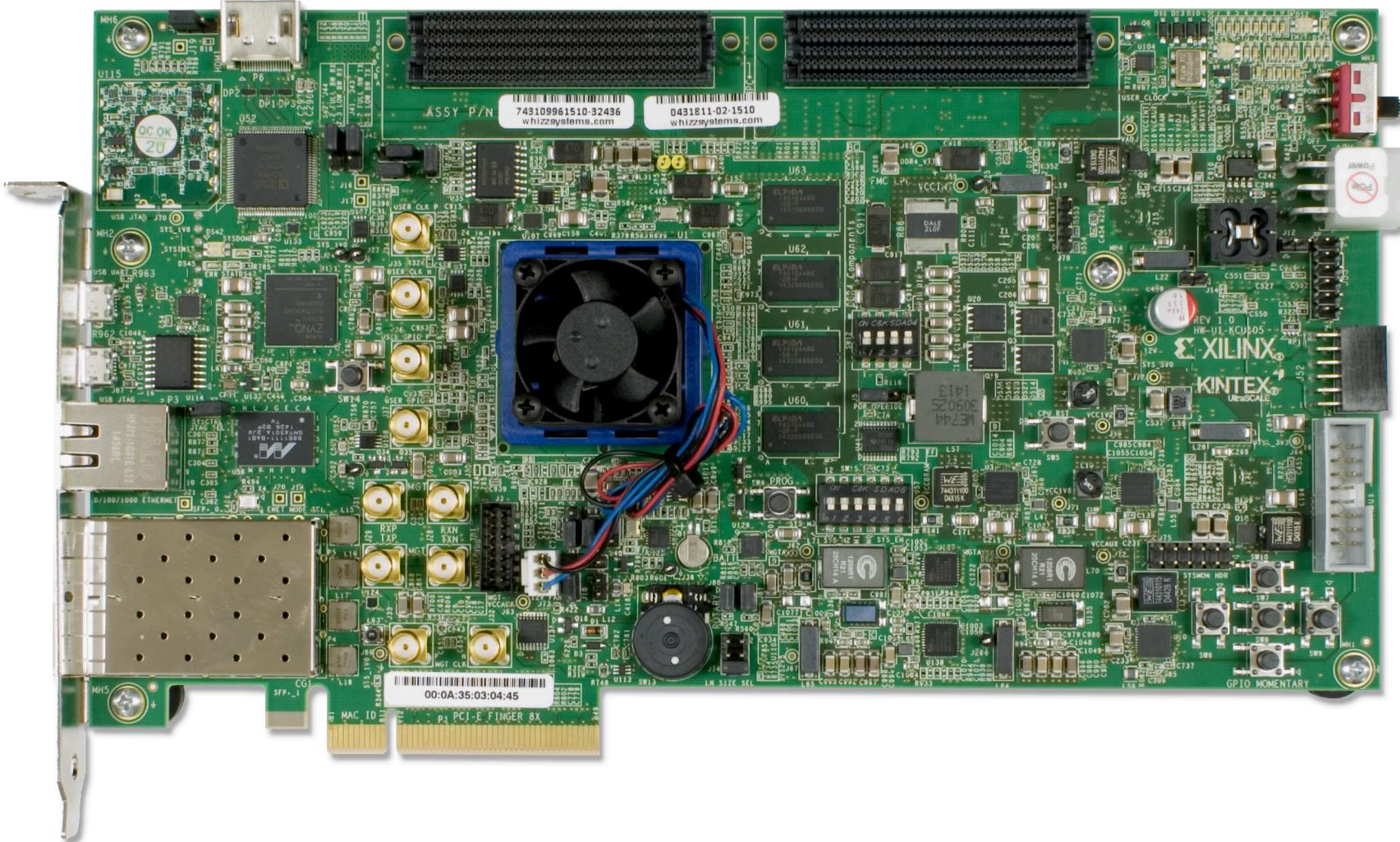
© Copyright 2017 Xilinx, Inc. Xilinx, the Xilinx logo, Artix, ISE, Kintex, Spartan, Virtex, Vivado, Zynq, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. All other trademarks are the property of their respective owners.

NOTICE OF DISCLAIMER: The information disclosed to you hereunder (the "Information") is provided "AS-IS" with no warranty of any kind, express or implied. Xilinx does not assume any liability arising from your use of the Information. You are responsible for obtaining any rights you may require for your use of this Information. Xilinx reserves the right to make changes, at any time, to the Information without notice and at its sole discretion. Xilinx assumes no obligation to correct any errors contained in the Information or to advise you of any corrections or updates. Xilinx expressly disclaims any liability in connection with technical support or assistance that may be provided to you in connection with the Information. XILINX MAKES NO OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED, OR STATUTORY, REGARDING THE INFORMATION, INCLUDING ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NONINFRINGEMENT OF THIRD-PARTY RIGHTS.

KCU105 Software Install and Board Setup

- Xilinx KCU105 Board
- Software Requirements
- KCU105 Hardware Setup
- UART Driver Install
- Terminal Setup
- Clock Setup
- Ethernet Setup
- Optional Hardware Setup
- References

Xilinx KCU105 Board



Note: Presentation applies to the KCU105

 XILINX ➤ ALL PROGRAMMABLE™

Software Requirements

- Xilinx Vivado Design Suite 2017.2, Design Edition with SDK



KCU105 Hardware Setup

► Kit Hardware contents

- KCU105 Board
- Two SFP Modules and fiber optic Patch cable
- XM107 FMC Loopback board
- PCIe Loopback board
- Micro USB cables
- Power supply



KCU105 Hardware Setup

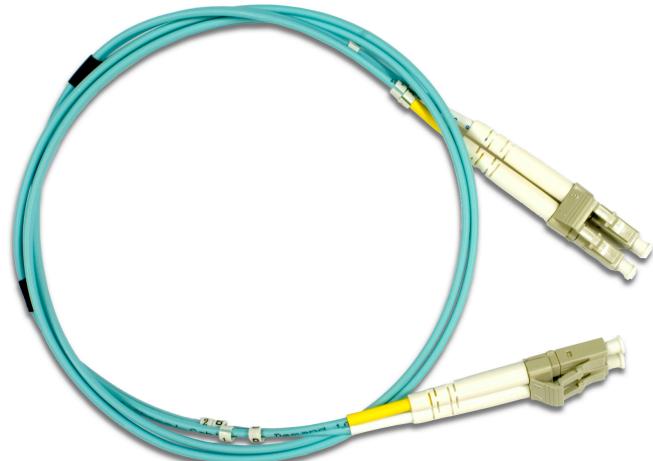
➤ Two Avago SFP+ Optical Transceivers

- <http://www.avagotech.com>
- Part number: [AFBR-709SMZ](#)
- 10Gb Ethernet, 850 nm,
10GBASE-SR/SW, SFP+
Transceiver



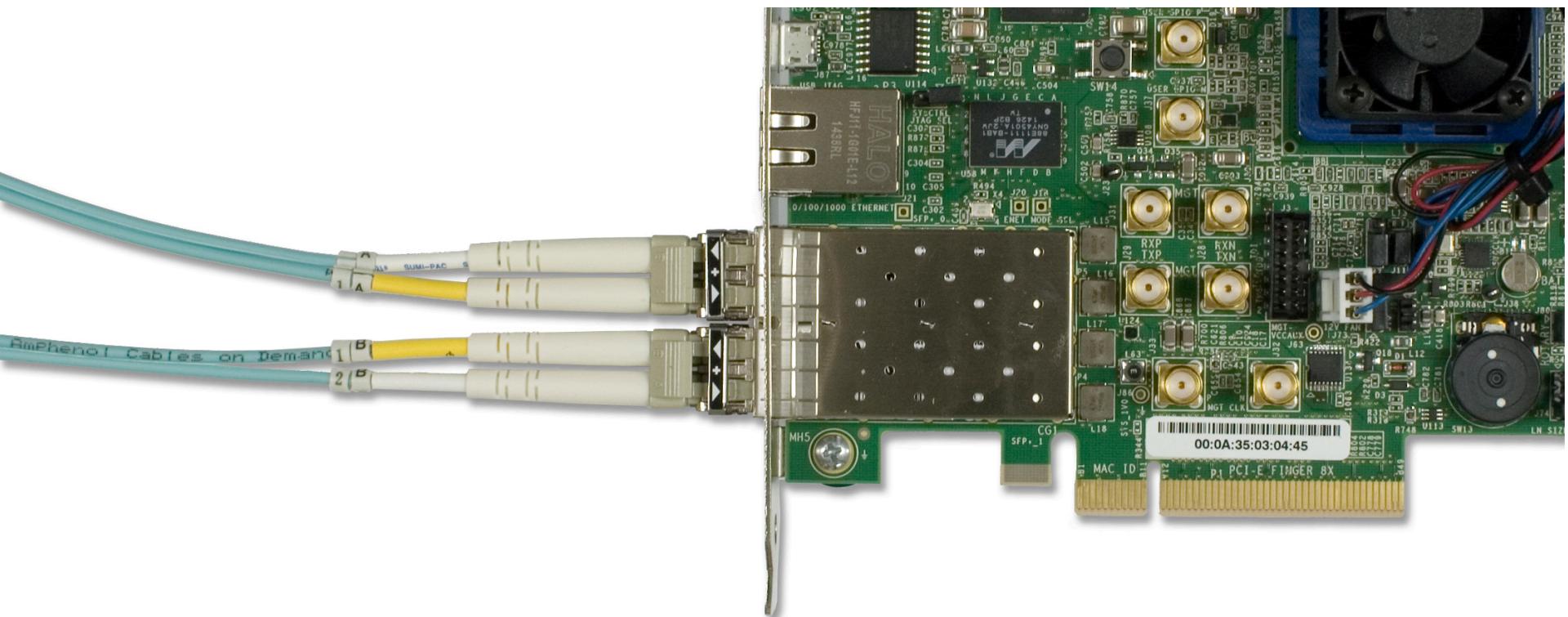
➤ Optical Patch cable

- Amphenol [Cables on Demand](#)



KCU105 Hardware Setup

- Insert these transceivers into the SFP cages (P4 & P5)
- Connect the two transceivers with the included Optical Patch cable
 - Remove the protective plastic caps before inserting



Note: Presentation applies to the KCU105

KCU105 Hardware Setup

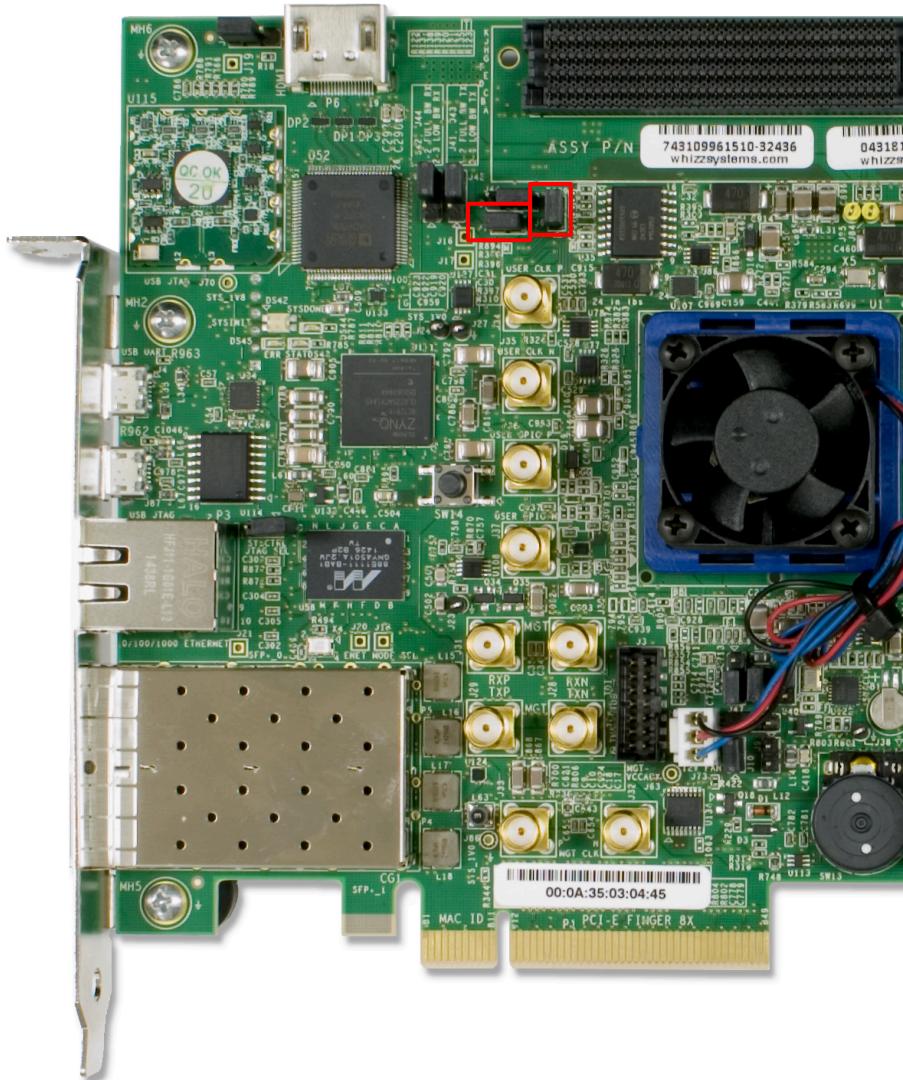


- Warning: These Optical transceivers contain lasers!
- As per the manufacturer's [datasheet](#):
 - Class 1 Eye safe per requirements of IEC 60825-1 / CDRH
- Wikipedia [notes](#):
 - “A Class 1 laser is safe under all conditions of normal use....It is important to realize that certain lasers classified as Class 1 may still pose a hazard when viewed with a telescope or microscope of sufficiently large aperture.”
- Therefore, when working with lasers, please observe the following caution:



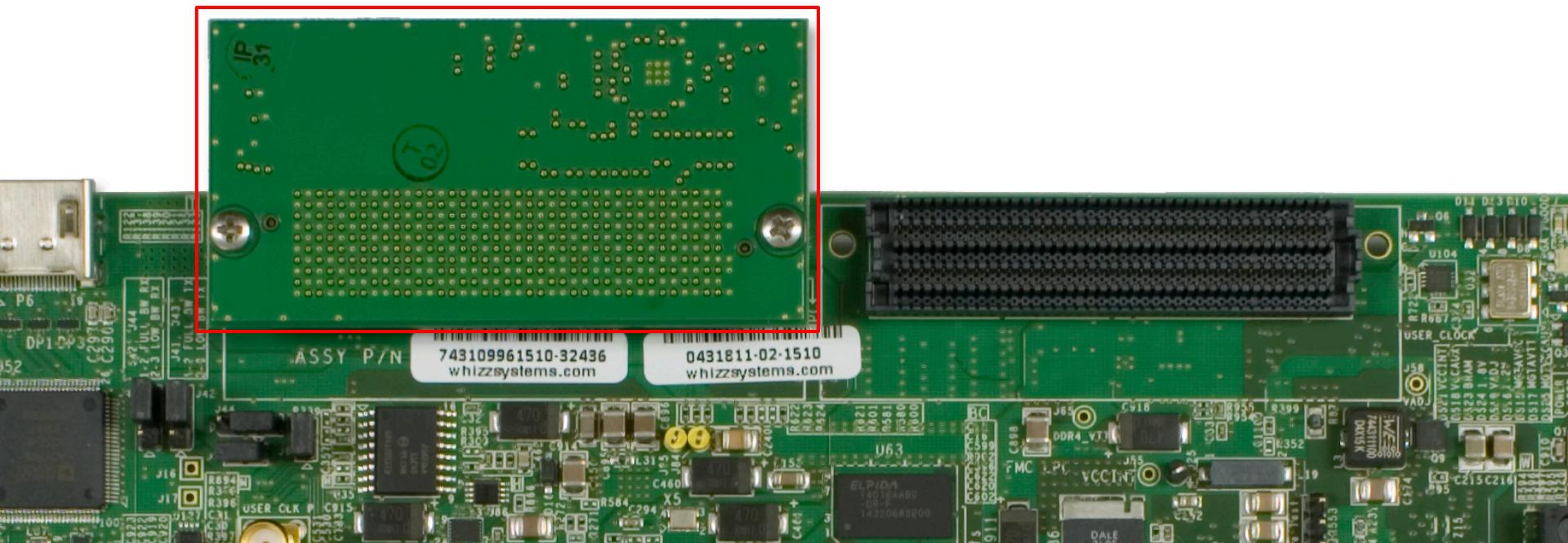
KCU105 Hardware Setup

- Ensure that jumpers are installed on J6 and J7
 - Required for the IBERT SFP test



KCU105 Hardware Setup

- ▶ Attach the FMC XM107 board to the FMC HPC connector (J22)



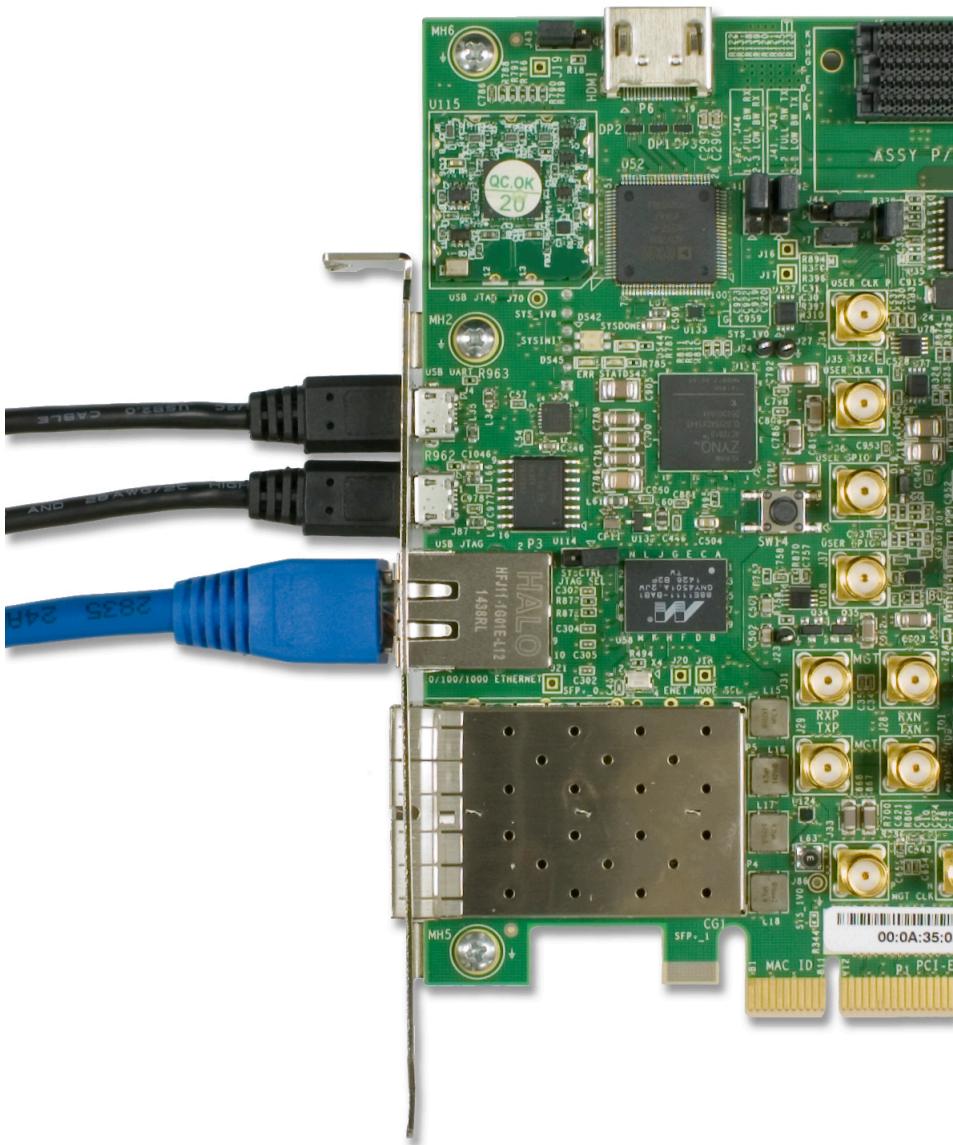
KCU105 Hardware Setup

- Connect a micro USB cable to the PCIe Loopback card for power
 - Connect this cable to your PC
- Attach to the PCIe connector (P1) on the KCU105



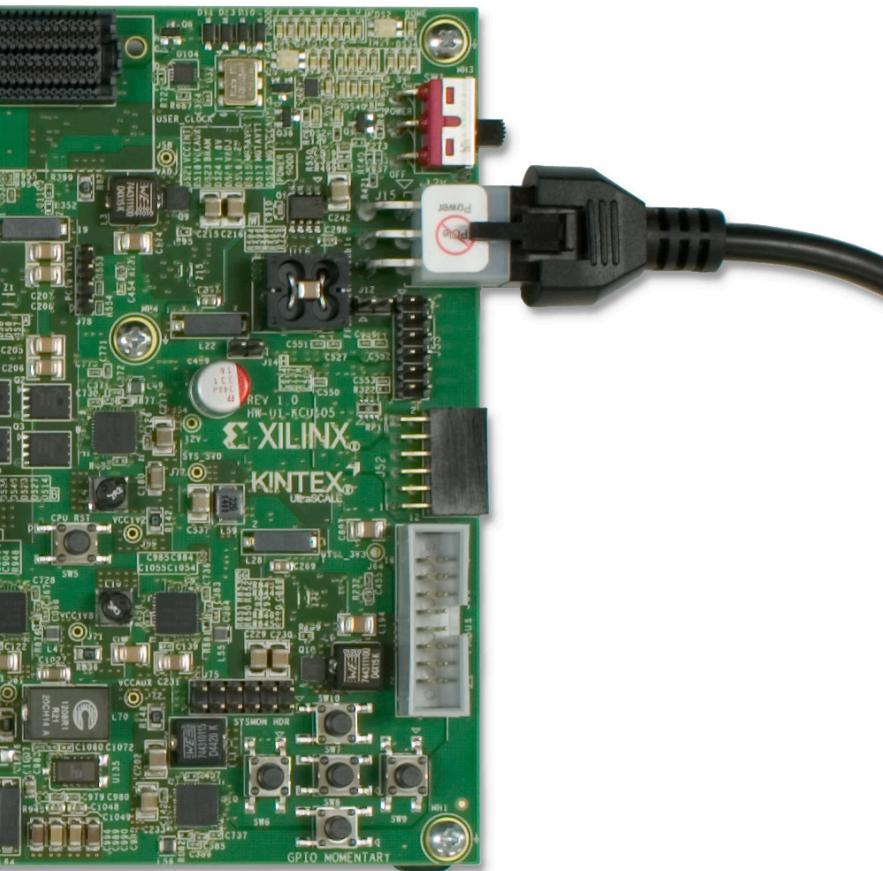
KCU105 Hardware Setup

- Connect a USB Type-A to Micro-B cable to the USB UART connector (J4) on the KCU105 board
- Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) (J87) connector on the KCU105 board
- Connect the Ethernet cable to P3
- Connect these cables to your PC



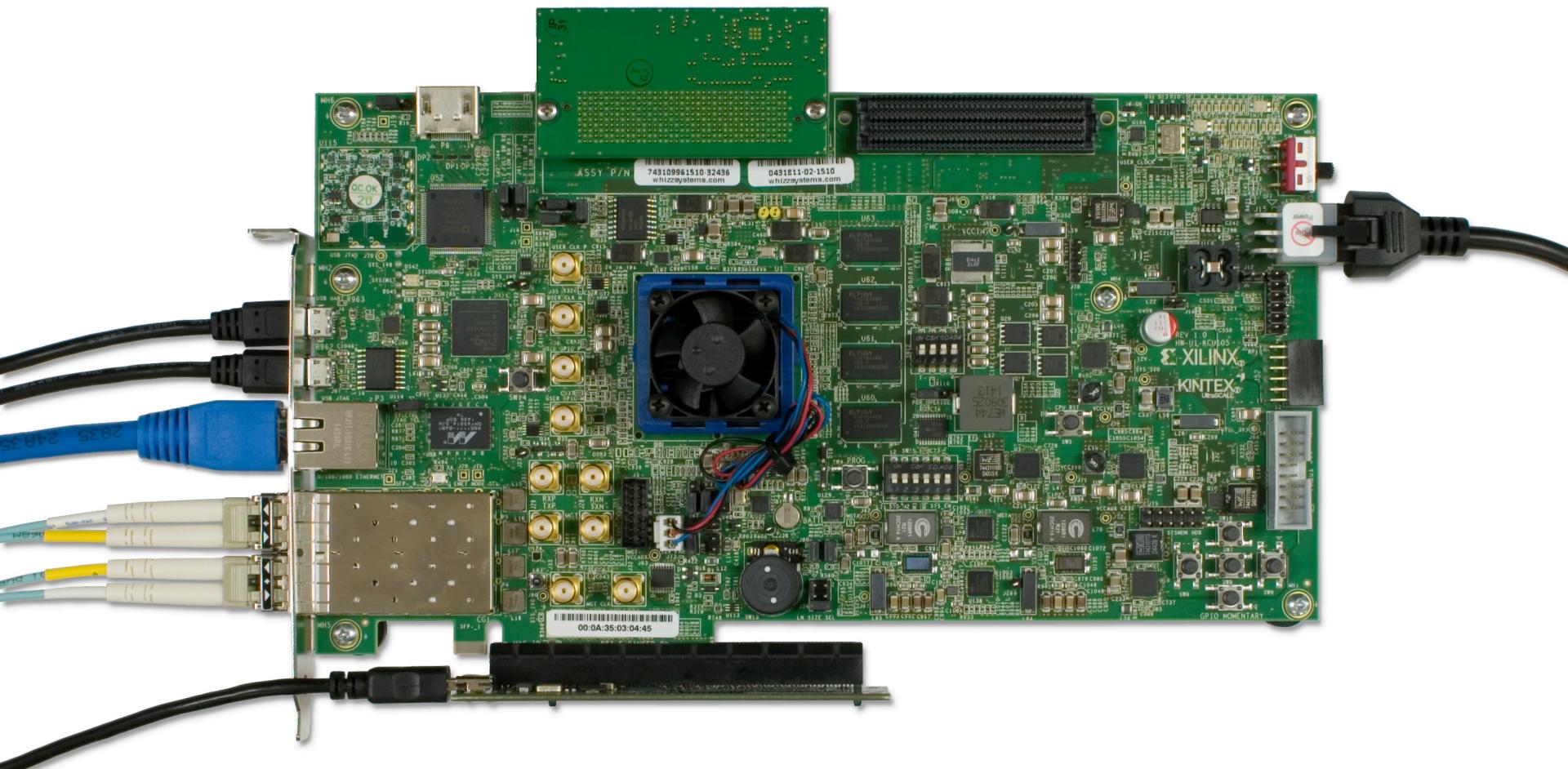
KCU105 Hardware Setup

- Connect the power supply to the KCU105 (J15)
 - Connect this cable a power outlet



KCU105 Hardware Setup

- Board connected with all Kit items installed
- Power on the KCU105 board for the UART driver installation



UART Driver Install

► Install Si Labs CP210x USB UART Drivers

- Refer to [UG1033](#) for details on installing the USB to UART Drivers



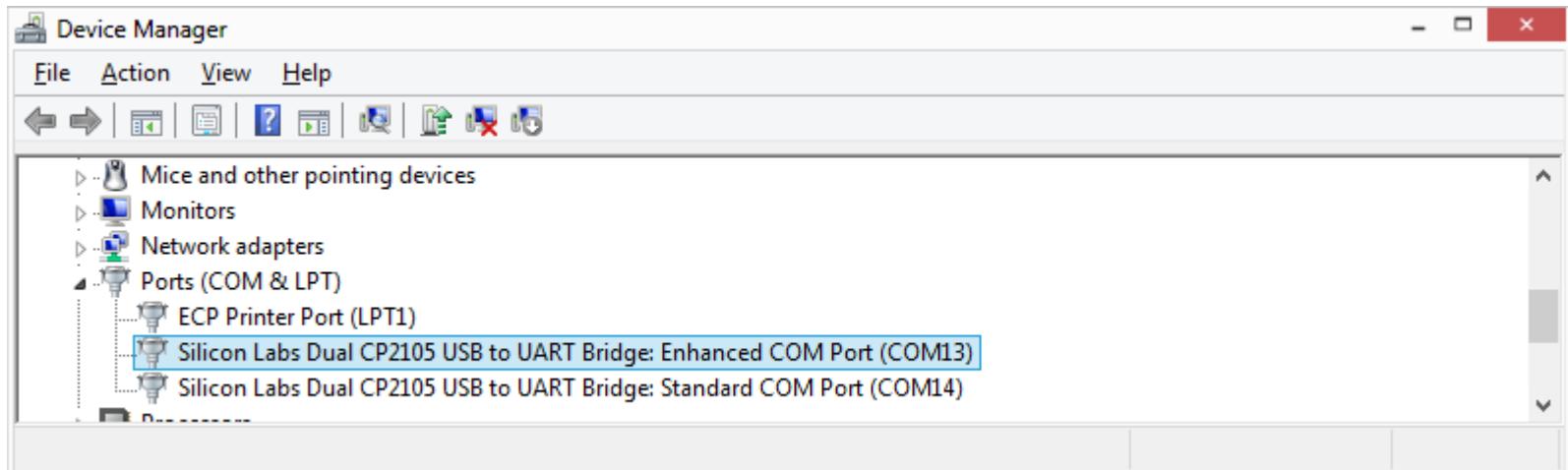
UART Driver Install

- Determine the COM Port numbers for your system
- Open the Device manager

Control Panel → System → Device Manager

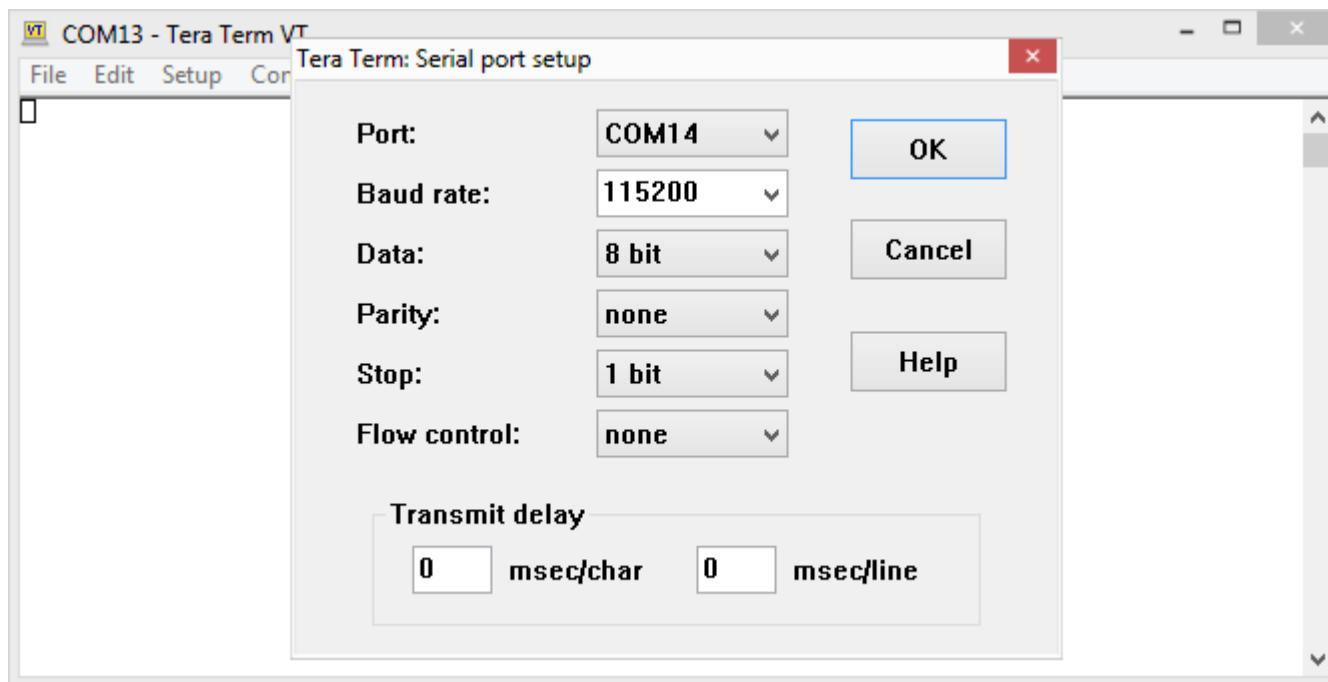
- There will be two “Silicon Labs Dual CP210x” COM ports, **Standard** and **Enhanced**
- The Standard COM Port is the FPGA UART COM Port
- The Enhanced COM Port is the System Controller COM Port
- The COM Port numbers **will vary** from system to system

- These COM Port Numbers will be used in several of the tutorials



Terminal Setup

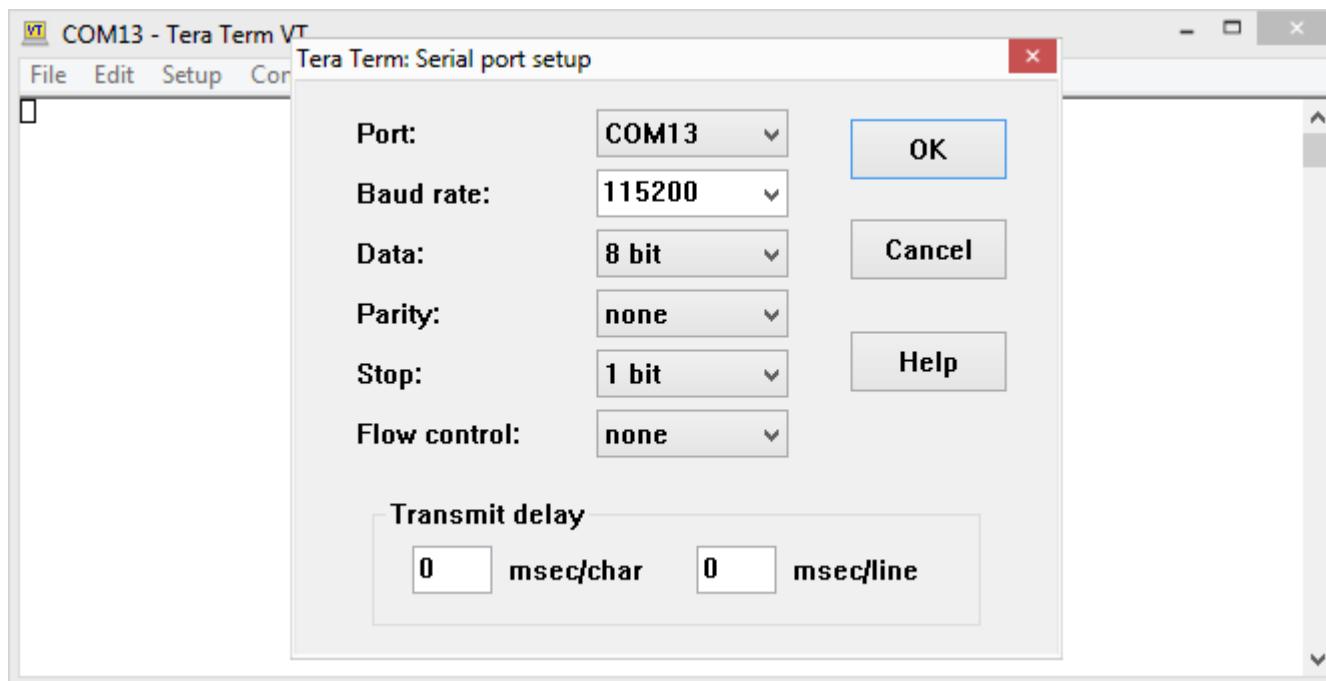
- Refer to [UG1036](#) regarding Tera Term installation
- Board Power must be on before starting Tera Term
- Start the Terminal Program
 - Select your Standard COM Port
 - Set the baud to **115200**



Terminal Setup

► Start a second Terminal Program for the System Controller

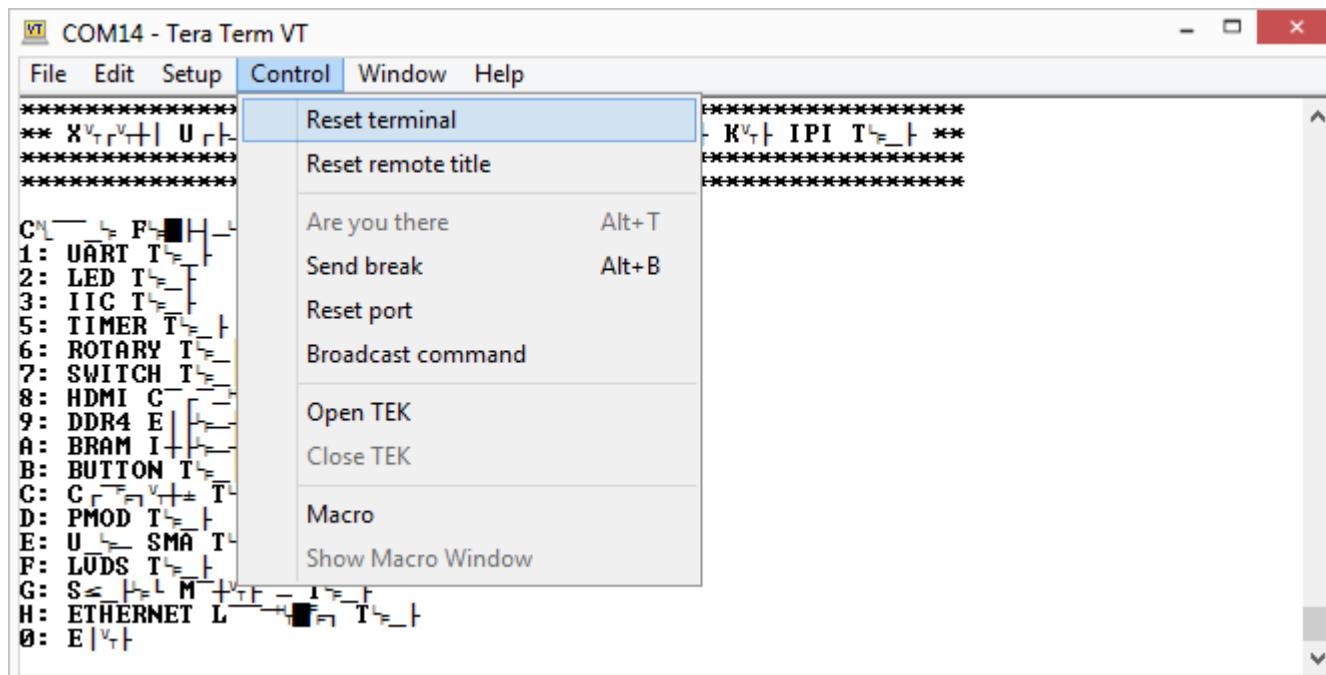
- Select your Enhanced COM Port
- Set the baud to **115200**



Terminal Setup

► If 115200 UART output occurs while set to 9600, you may need to reset Tera Term. From the menu select:

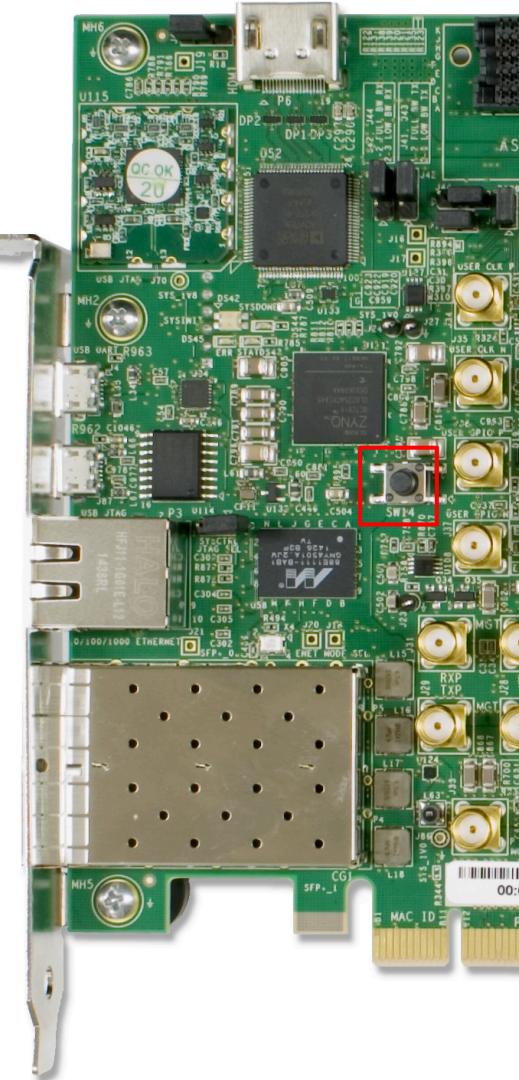
Control -> Reset Terminal



Terminal Setup

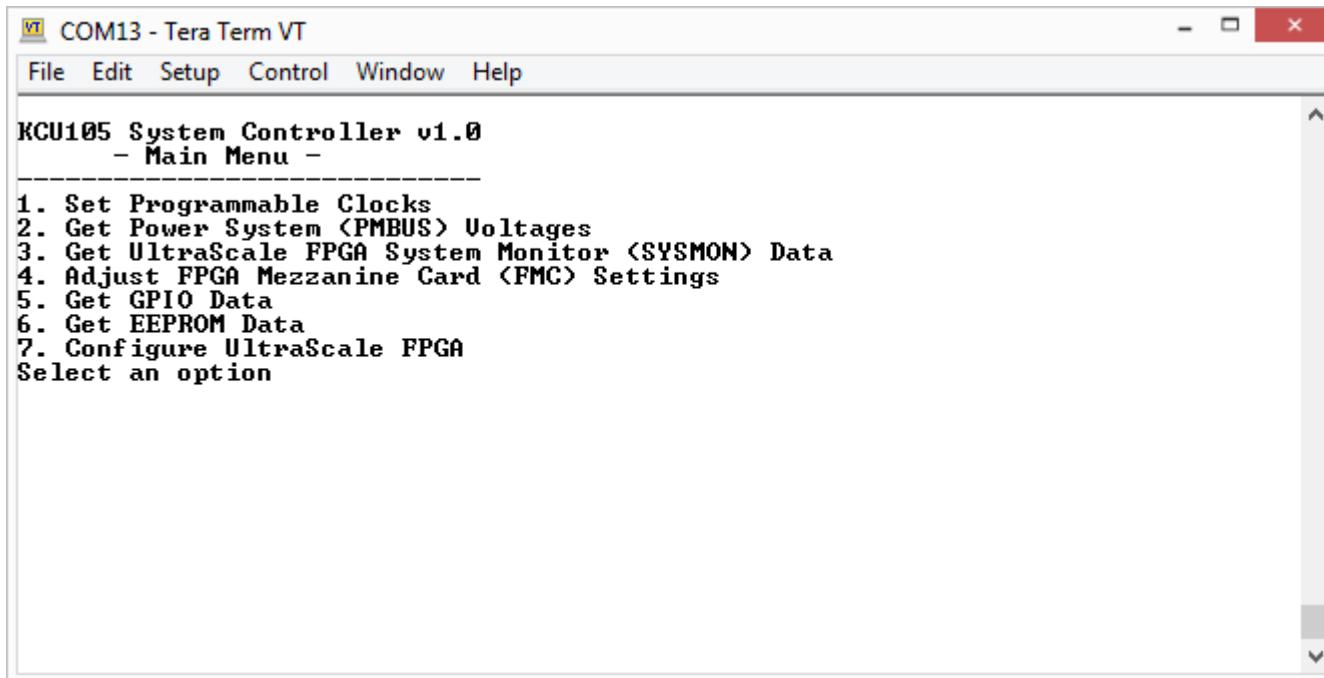
► Press CPU Reset (SW5) or SW14 (System Controller) to clear the terminal output

```
VT COM14 - Tera Term VT
File Edit Setup Control Window Help
*****
** Xilinx UltraScale FPGA KCU105 Evaluation Kit IPI Test **
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: IIC Test
5: TIMER Test
6: ROTARY Test
7: SWITCH Test
8: HDMI Colorbar Test
9: DDR4 External Memory Test
A: BRAM Internal Memory Test
B: BUTTON Test
C: Clocking Test
D: PMOD Test
E: User SMA Test
F: LVDS Test
G: System Monitor Test
H: ETHERNET Loopback Test
0: Exit
```



Clock Setup

- Cycle Board Power and view the System Controller Menu
- Note: When running the Board Interface Test (XTP345), both UART terminals must be disconnected



Clock Setup

- Set the Si570 Frequency to 163 MHz for Hardware Testing
- Press “1”, Enter, “1”, Enter, then enter “163”; press “Enter”
 - Note: The HPC IBERT test derives its Ref clocks from this on-board Si570

COM13 - Tera Term VT

File Edit Setup Control Window Help

```
2. Get Power System (PMBUS) Voltages
3. Get UltraScale FPGA System Monitor (SYSMON) Data
4. Adjust FPGA Mezzanine Card (FMC) Settings
5. Get GPIO Data
6. Get EEPROM Data
7. Configure UltraScale FPGA
Select an option
1

KCU105 System Controller v1.0
- Clock Menu -

1. Set KCU105 Si570 User Clock Frequency
2. Set KCU105 Si5328 MGT Clock Frequency
3. Save KCU105 Clock Frequency to EEPROM
4. Restore KCU105 Clock Frequency from EEPROM
5. View KCU105 Saved Clocks in EEPROM
6. Set KCU105 Clock Restore Options
7. Read KCU105 Si570 User Clock Frequency
8. Read KCU105 Si5328 MGT Clock Frequency
0. Return to Main Menu
Select an option
1

Enter the Si570 frequency (10-810MHz):
163

RFreq_Cal[0]=0x02, RFreq_Cal[1]=0xBC, RFreq_Cal[2]=0x00, RFreq_Cal[3]=0xE4, RFreq_Cal[4]=0xED

Freq:163.0000000000 HS_DIV=5 N1=6 DCO=4890.0 RFREQ=0x02AC9A797D
```

Clock Setup

- The Si5328 Frequency must be set to 156.25 MHz
- Press “2”, Enter, then enter “156.25”; press “Enter”
 - Note: The LPC, SFP, and SMA IBERT tests derive their Ref clocks from this Si5328

COM13 - Tera Term VT

```
File Edit Setup Control Window Help
3. Save KCU105 Clock Frequency to EEPROM
4. Restore KCU105 Clock Frequency from EEPROM
5. View KCU105 Saved Clocks in EEPROM
6. Set KCU105 Clock Restore Options
7. Read KCU105 Si570 User Clock Frequency
8. Read KCU105 Si5328 MGT Clock Frequency
0. Return to Main Menu
Select an option
2

Enter the Si5328 frequency <0.008-808MHz>:
156.25

Freq:156.2500000000 fosc=5000.000MHz f3= 5.000KHz LBW=0.200KHz N1=32 N1_HS=8 NC1
_LS=4 N2=1000000 N2_HS=4 N2_LS=250000 N31=31250 N32=22857

KCU105 System Controller v1.0
- Clock Menu -
1. Set KCU105 Si570 User Clock Frequency
2. Set KCU105 Si5328 MGT Clock Frequency
3. Save KCU105 Clock Frequency to EEPROM
4. Restore KCU105 Clock Frequency from EEPROM
5. View KCU105 Saved Clocks in EEPROM
6. Set KCU105 Clock Restore Options
7. Read KCU105 Si570 User Clock Frequency
8. Read KCU105 Si5328 MGT Clock Frequency
0. Return to Main Menu
Select an option
```

Note: The Si5328 must be reprogrammed after cycling power

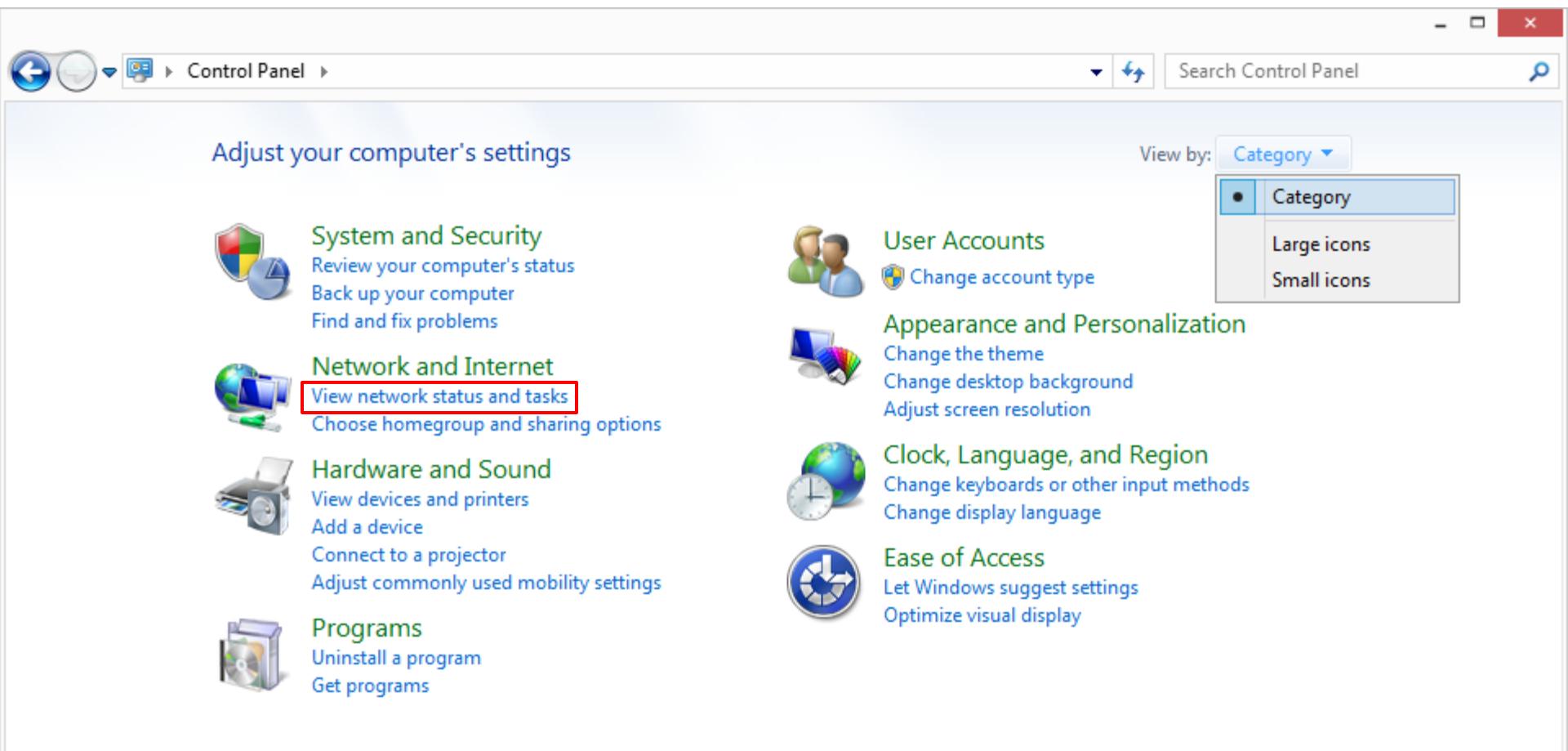
XILINX ➤ ALL PROGRAMMABLE™

Ethernet Setup

► Open the Windows Control Panel

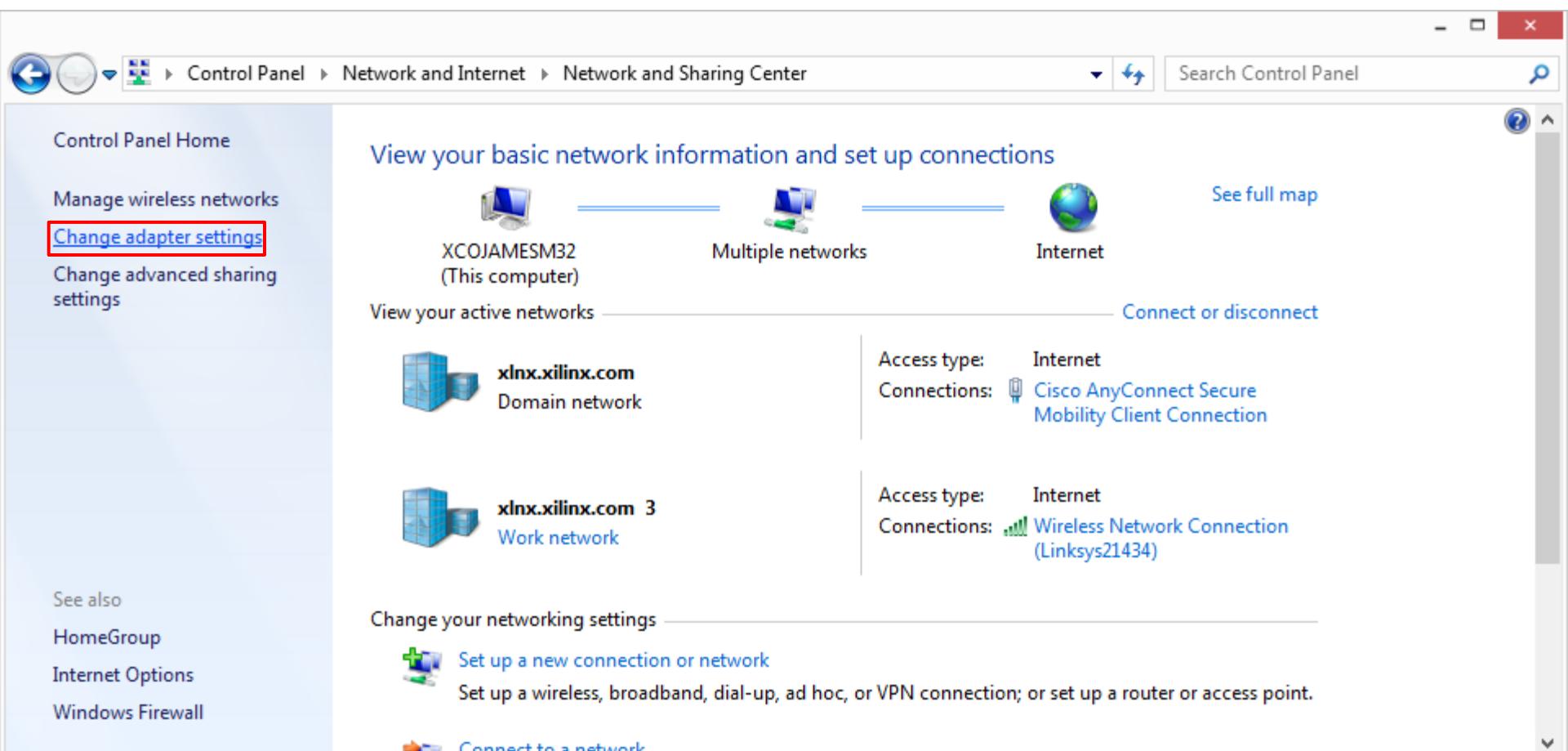
- Set to View by Category

► Click on “View network status and tasks”



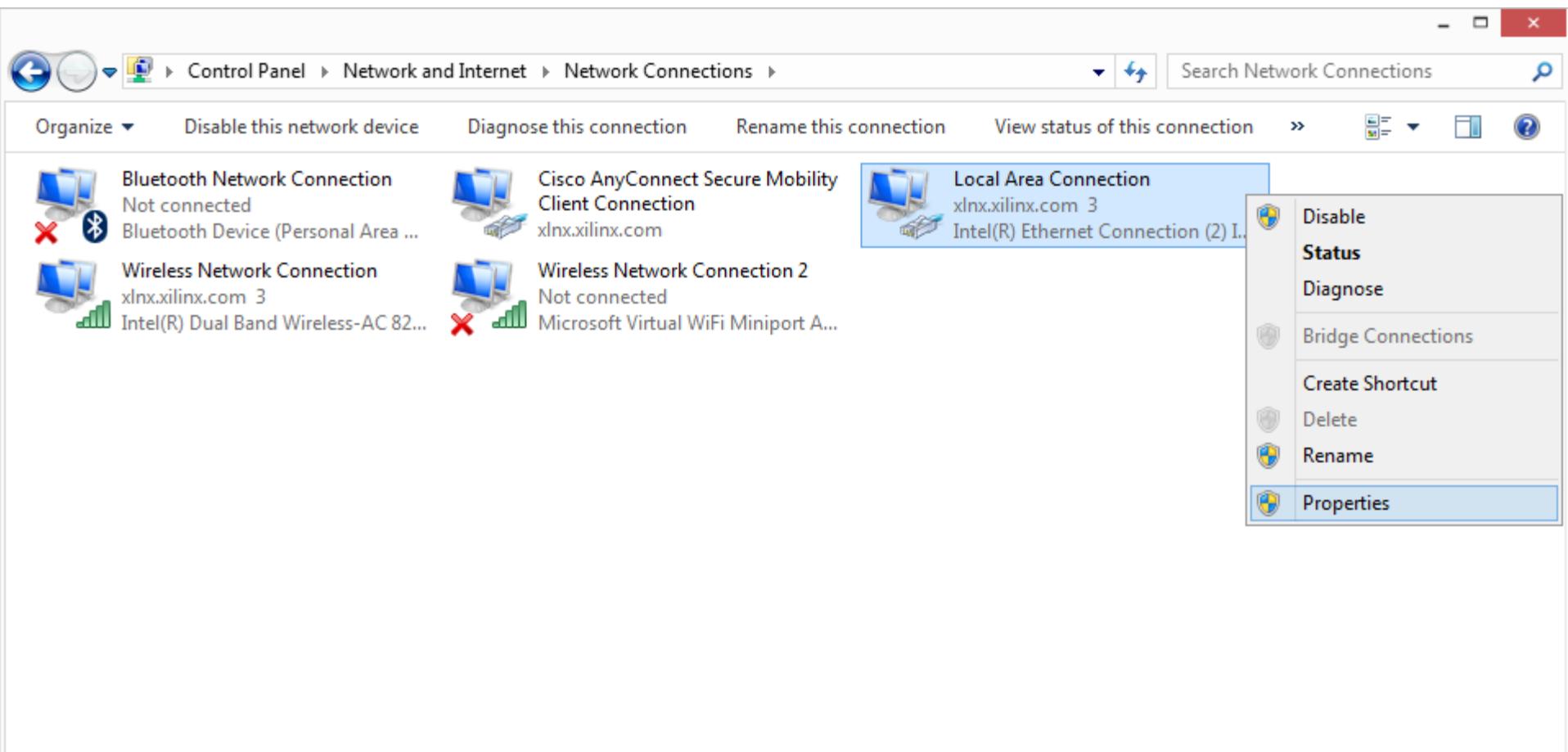
Ethernet Setup

► Click on “Change adapter settings”



Ethernet Setup

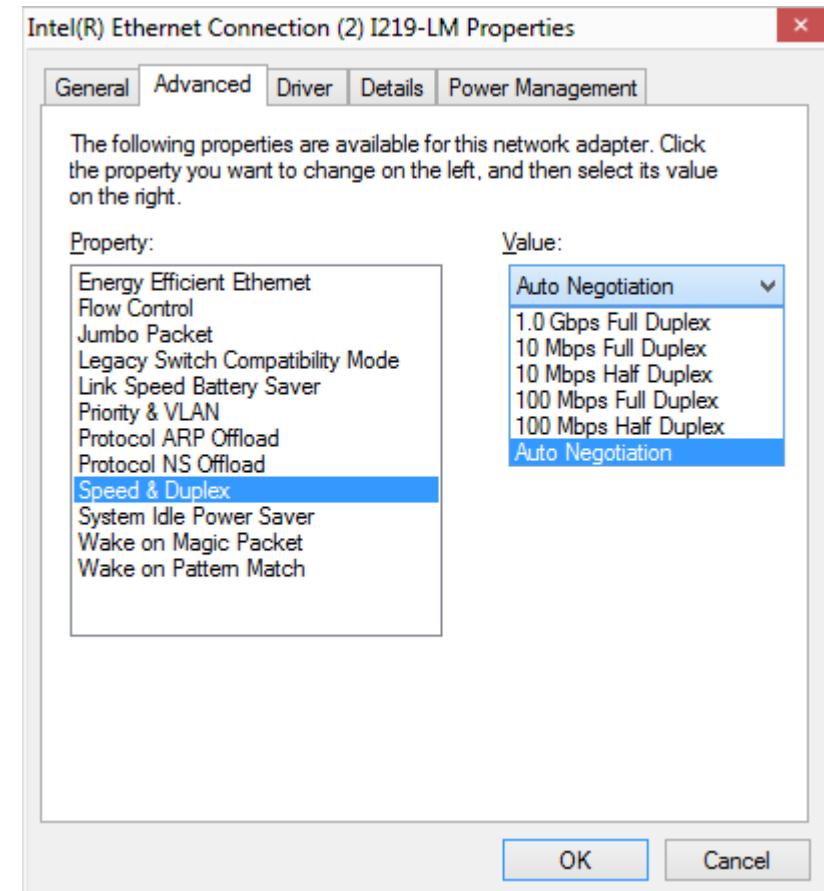
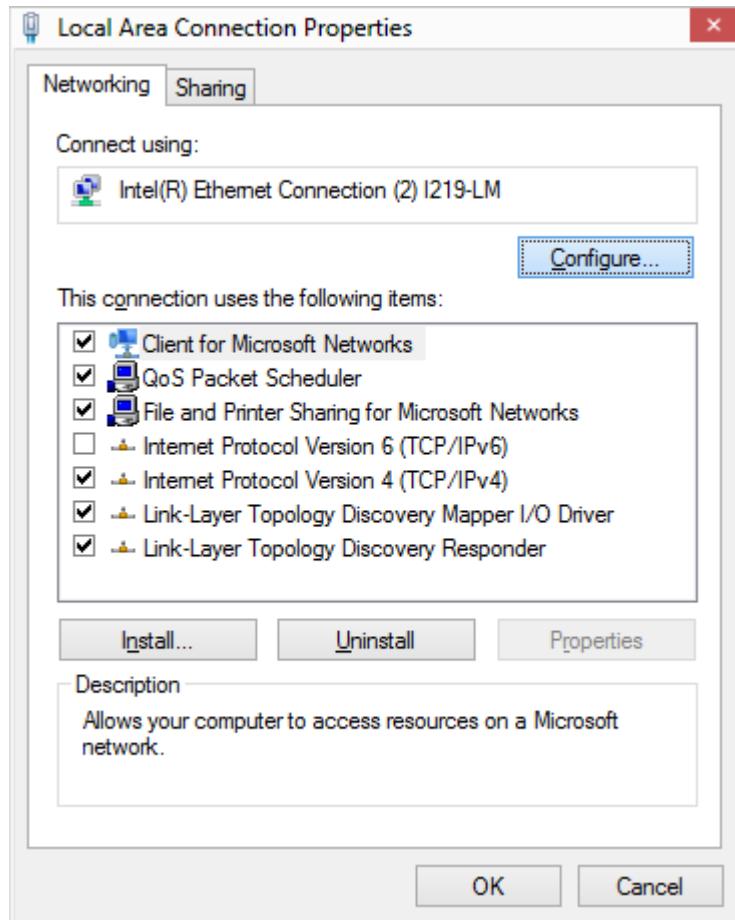
► Right-click on the Gigabit Ethernet Adapter that you will be using for this test and select Properties



Ethernet Setup

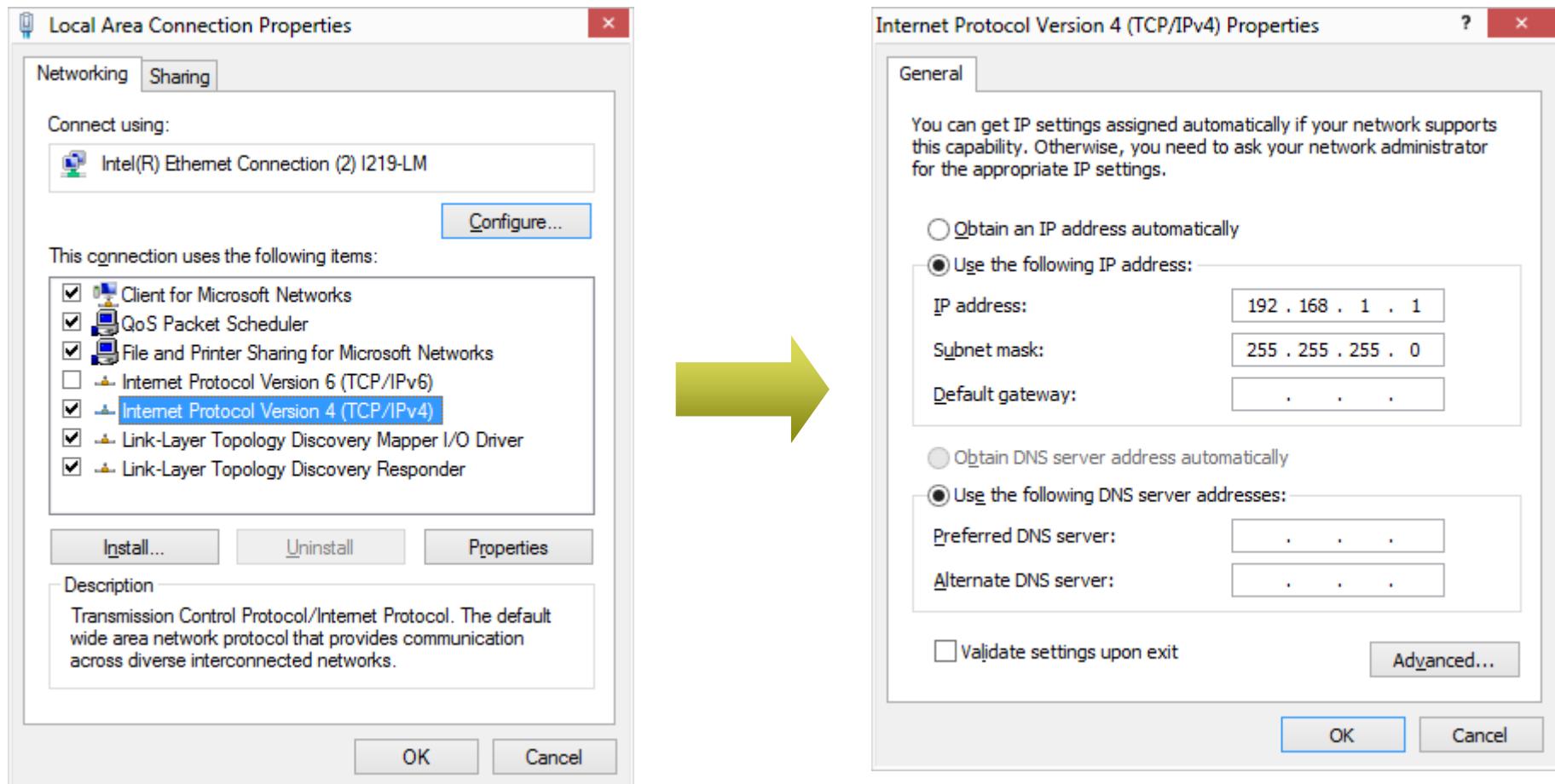
► Click Configure

- Set the Link Speed & Duplex to Auto Negotiation then click OK



Ethernet Setup

- Reopen the properties after the last step
- Double-click the Internet Protocol Version 4
- Set your host (PC) to this IP Address:

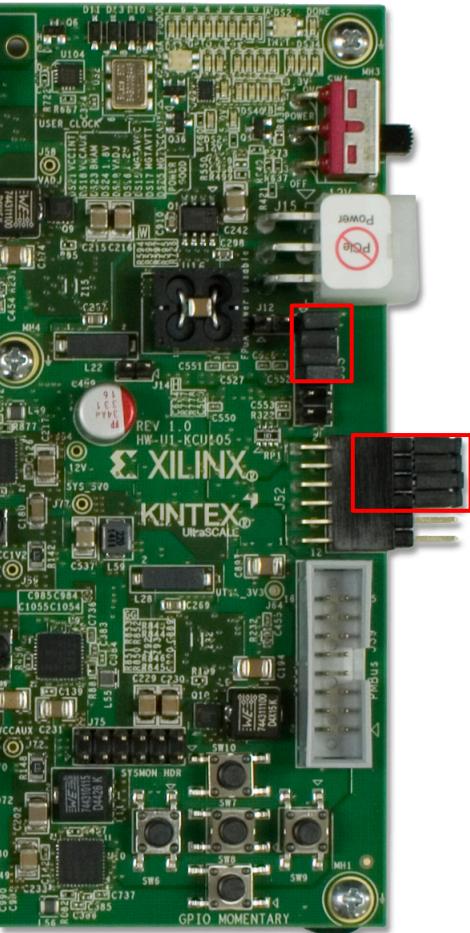


Note: Remember to restore your IP settings when finished

Optional Hardware Setup

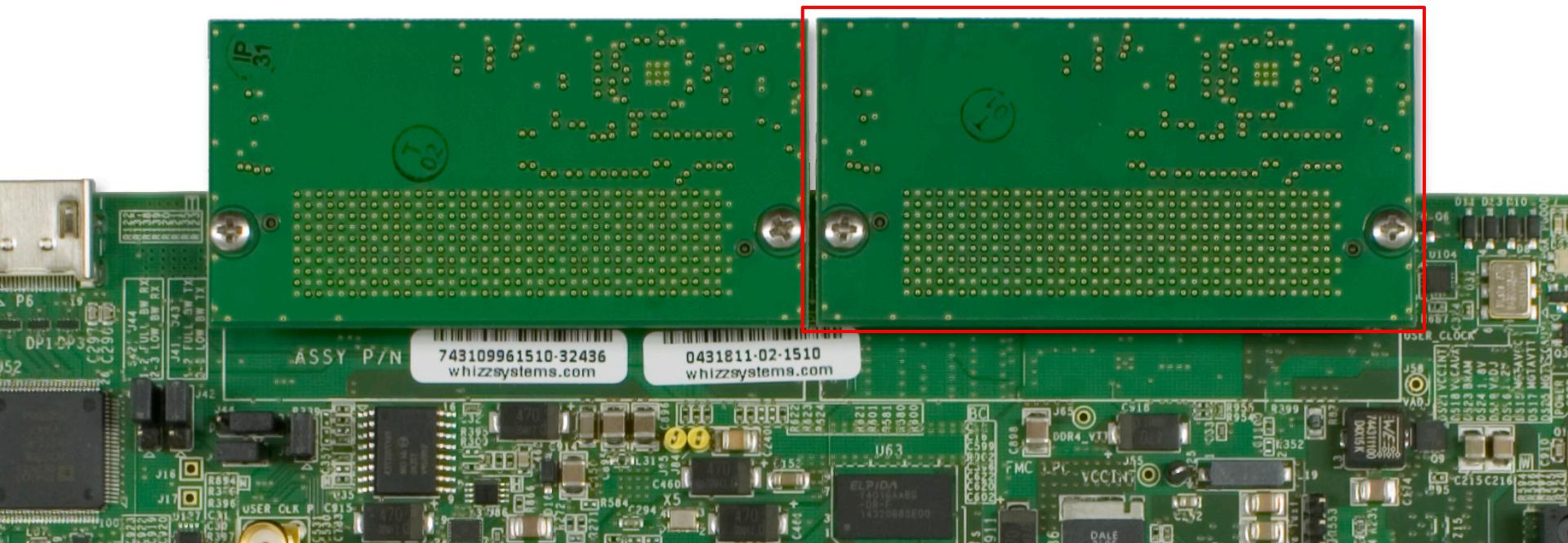
- Connect PMOD headers
- Both J52 and J53:

- 1 to 2
- 3 to 4
- 5 to 6
- 7 to 8



Optional Hardware Setup

- Attach a second FMC XM107 board to the FMC LPC connector (J2)
- Available through [Whizz Systems](#)



Optional Hardware Setup

➤ Two SMA Cables

- www.rosenbergerna.com
- Part number:
72D-32S1-32S1-00610A



➤ Optional: SMA Quick connects

- RADIALL
- Part number: R125791501
- Available [here](#) or [here](#)



Optional Hardware Setup

➤ Hook up the SMA cables as shown

➤ IBERT Test:

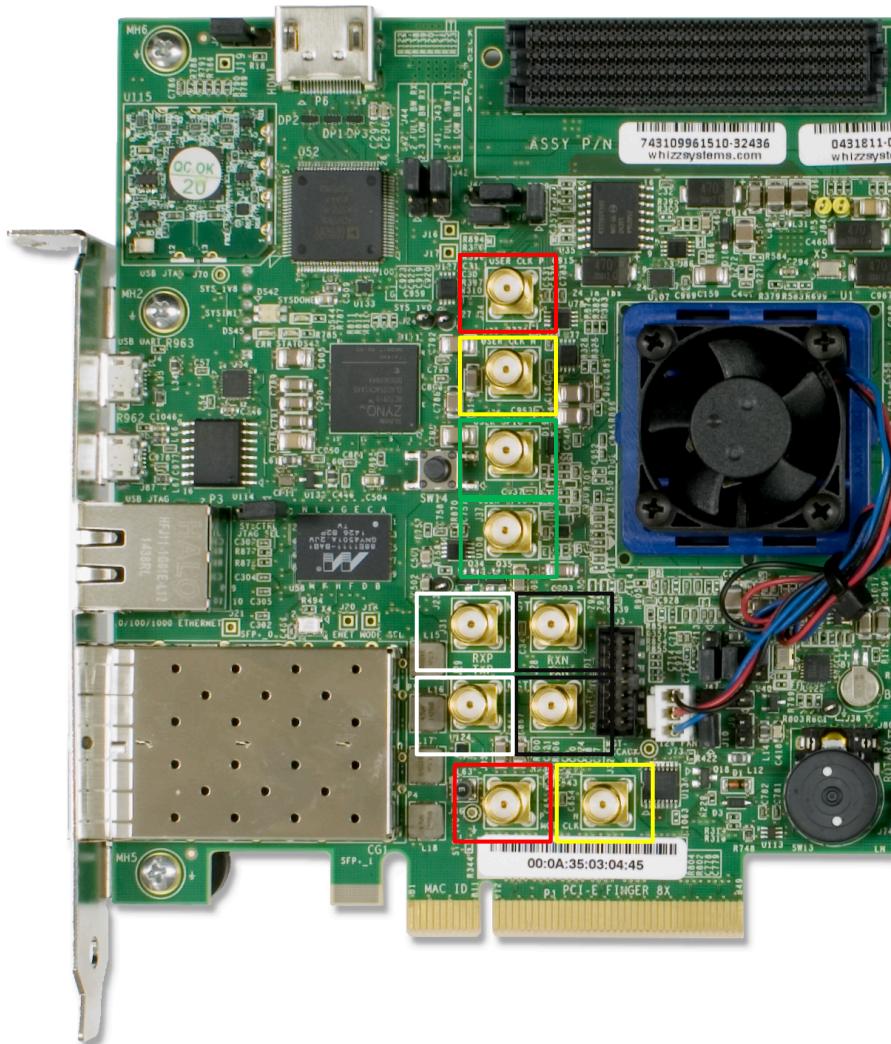
- J29 to J31 (White)
- J28 to J30 (Black)

➤ Clocking Test

- J33 to J34 (Red)
- J32 to J35 (Yellow)

➤ User SMA Loopback

- J36 to J37 (Green)



Optional Hardware Setup

- Using a common HDMI cable, connect an HDMI Monitor to the HDMI port (P6)



References

References

➤ Vivado Release Notes

- Vivado Design Suite User Guide - Release Notes – UG973
 - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2017_2/ug973-vivado-release-notes-install-license.pdf
- Vivado Design Suite 2017 - Vivado Known Issues
 - <https://www.xilinx.com/support/answers/68923.html>

➤ Vivado Programming and Debugging

- Vivado Design Suite Programming and Debugging User Guide – UG908
 - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2017_2/ug908-vivado-programming-debugging.pdf

Documentation

Documentation

► Kintex UltraScale

- Kintex UltraScale FPGA Family
 - <https://www.xilinx.com/products/silicon-devices/fpga/kintex-ultrascale.html>

► KCU105 Documentation

- Kintex UltraScale FPGA KCU105 Evaluation Kit
 - <https://www.xilinx.com/products/boards-and-kits/kcu105.html>
- KCU105 Board User Guide – UG917
 - https://www.xilinx.com/support/documentation/boards_and_kits/kcu105/ug917-kcu105-eval-bd.pdf
- KCU105 Evaluation Kit Quick Start Guide User Guide – XTP391
 - https://www.xilinx.com/support/documentation/boards_and_kits/kcu105/xtp391-kcu105-quickstart.pdf
- KCU105 - Known Issues Master Answer Record
 - <https://www.xilinx.com/support/answers/63175.html>