Higher Voltage Level and Lower Total Harmonic Distortion in a New Setting up Multilevel Inverter

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Abstract- **In this paper some new multilevel inverter topologies, their characteristics and also block diagram are presented. They are essentially based on cascade multilevel inverter with the same number of switches and separated dc sources. The paper is illustrated that increasing the number of output waveform levels in the topologies reduces the low order harmonics and also the total harmonic distortion which are so harmful and trouble maker in power electronic devices. It's shown that one of the presented multilevel inverter topologies uses a method which reduces the number of in use switches. The effect of higher DC link voltage on multilevel inverters is also explained. A new topology of multilevel inverter is presented too which has the highest number of output voltage levels due to the number of the cells which is made it so operational. The topologies MATLAB simulation comparison results are presented as well.**

Keywords: Cascade Multilevel Inverter, Total Harmonic Distortion, Output waveform levels.

I. INTRODUCTION

Inverters are very popular power electronic devices which are widely used in adjustable speed motor drivers, power supplies and photovoltaic cells. These devices are used to create single or poly phase AC voltage from a dc source [1, 2]. The inverter sinusoidal output waveform causes the output harmonics to be optimized [3].

The presented inverters in this paper are:

A) Cascade H-bridge
B) Incremental cascade H-bridge
C) Incremental cascade I–bridge
D) Incremental – reduction cascade H-bridge
E) Combined cell cascade

More details on these multilevel topologies are highlighted later.

In this paper, after presenting the 5 multilevel inverters block diagram, their features, and also output waveforms, their MATLAB simulation comparison results are declared.

A new structure of multilevel inverter is presented which significantly increases the number of output voltage levels for the same number of stages which is reduced the low order harmonics and also the total harmonic distortion (THD). Elimination of low order harmonics and reduction of THD in the output voltage are generally desired because their filtering is so hard.

It's also explained that how using a technique in a topology, helps decreasing of the switches number. As well, it's declared that how the cell with higher DC link voltage has lower switching frequency which causes reduction in switching losses.

I. CASCADE STRUCTURE MULTILEVEL INVERTER

The basic features of various cascade multilevel topologies are summarized in this section.

The output voltage waveform and the harmonic chart of each topology are also presented [4].

A. Cascade H-bridge multilevel inverter

Fig. 1 shows the block diagram of a single phase leg of the cascade H-bridge multilevel inverter. The output waveform levels consist of $S \times V_{DC}$ where S is the number of the separated dc sources or the number of the cells. The number of levels in the output waveform is equal to 2S+1.

Fig. 2 illustrates the output waveform and the harmonic chart of a cascade H-bridge multilevel inverter using S=2. The 5 levels of the output are $\pm 1V_{DC}$, $\pm 2V_{DC}$ and 0. Note that the dc source has the voltage value of 10v.

B. Incremental cascade H-bridge

This section introduces a topology based on the cascade H-bridge named incremental cascade H-bridge (Fig. 3). It increases the number of output waveform levels thereby considerably reduces the low order harmonics and also THD.

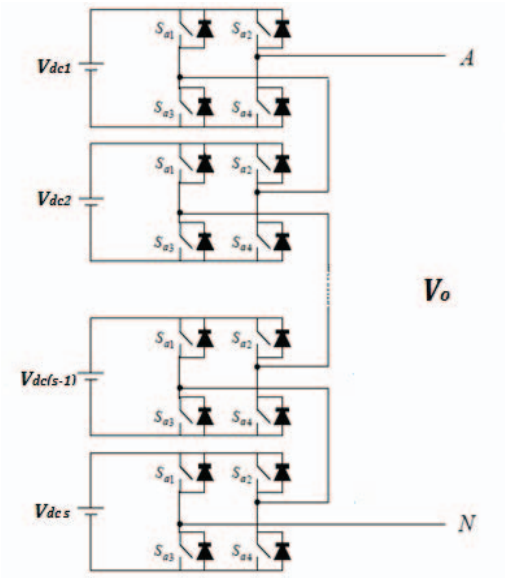

Figure 1. Cascade H-bridge multilevel inverter.

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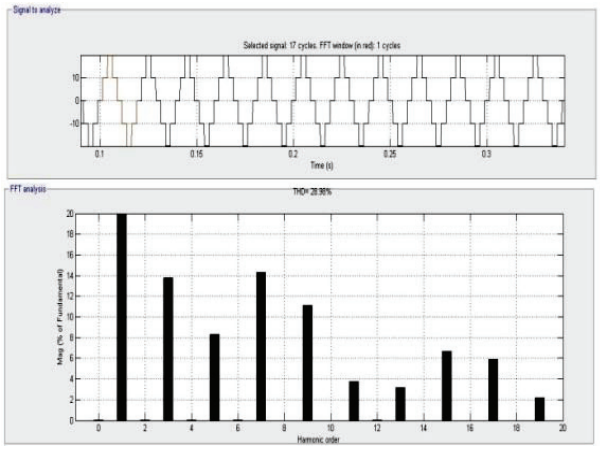

Figure 2. Output waveform and the harmonic chart of a cascade H-bridge with S=2.

One of the advantages of the structure is that the stage with higher DC-link voltage has lower number of commutations which reduces the associated switching losses on one hand and by using special technique reduces the number of the switching devices on the other hand.

The number of output levels is 2^{S+1} where S is the number of the separated dc sources or the number of the cells. In Fig. 4 the incremental cascade H-bridge multilevel inverter output and its harmonic chart, for S=2 are shown. The output waveform has 7 levels: $\pm 3V_{DC}$, $\pm 2V_{DC}$, $\pm 1V_{DC}$ and 0.

C. Incremental cascade I-bridge

Fig. 5 shows the block diagram of a single phase leg for the incremental cascade I-bridge. In this topology one leg of H-bridge is canceled by using special method.

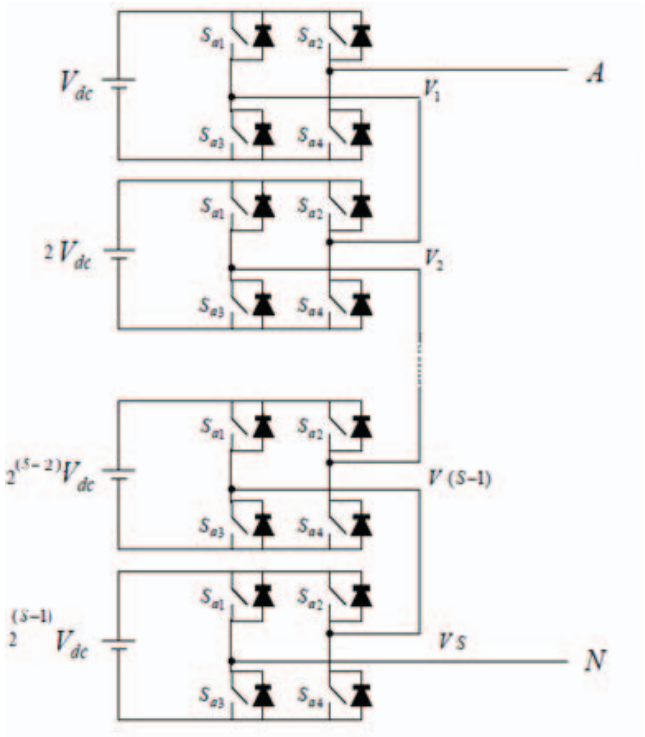

Figure 3. Incremental cascade H-bridge.

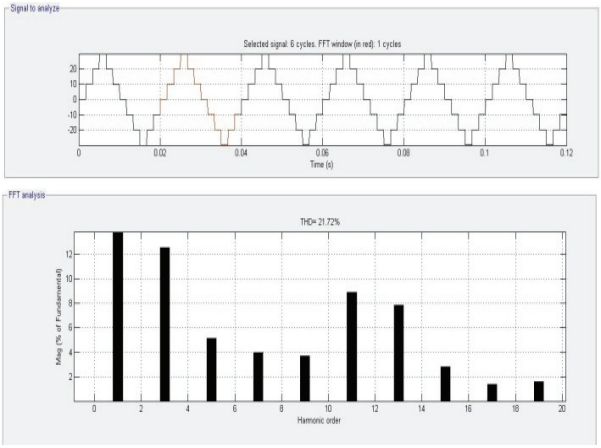

Figure 4. Output waveform and the harmonic chart of an incremental cascade H-bridge with S=2.

A switch can be removed from the circuit, without any difference in the situation during a period. In this case we can use usual state instead of switch.

We can create the half period (positive or negative) of original output waveform and use H-bridge cell to produce another half period (positive or negative) in different time. So the main cell cycle becomes shorter. Special switching method can be selected to put switches in permanent status which causes some of them be removed. The number of switches in this topology is less than H-bridge topology:

$$b = (S \times 4) \quad \text{For H-bridge topology} \tag{1}$$

$$b = (S \times 2) + 4 \quad \text{For I-bridge topology} \tag{2}$$

Fig. 6 presents the output waveform and the harmonic chart of the incremental cascade I-bridge multilevel inverter for S=2.

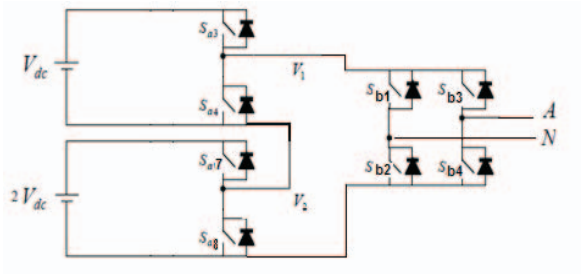

Figure 5. Incremental cascade I-bridge.

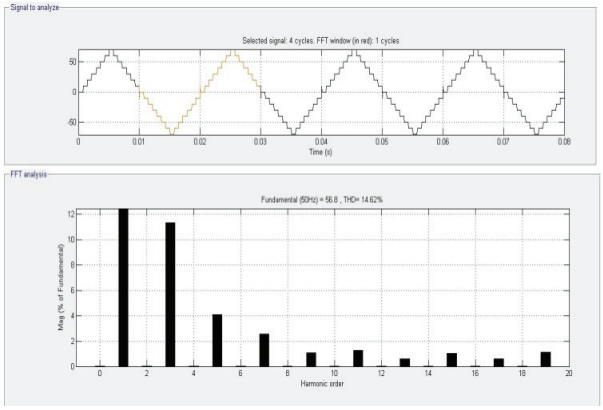

Figure 6. Output waveform and the harmonic chart of an incremental cascade I-bridge with S=2.

As it's shown the output waveform has 15 levels :$\pm 7V_{DC}$, $\pm 6V_{DC}$, $\pm 5V_{DC}$, $\pm 4V_{DC}$, $\pm 3V_{DC}$, $\pm 2V_{DC}$, $\pm 1V_{DC}$ and 0. But it only uses 8 switches instead of 12 switches in incremental cascade H-bridge. Note that the original cells have the module properties.

D. Incremental - reduction cascade H-bridge

The block diagram of a single phase leg for the incremental-reduction cascade H-bridge is shown in Fig. 7. The inverter consists of H-bridge while the DC-link voltage among the cells is 1V, 3V, 9V,… .

In this topology the original output is the summation of all cells output. Each cell can produce positive or negative polarities. In Fig. 8, the output waveform for S=2 is illustrated. The output waveform has 9 levels (3^S): $\pm 4V_{DC}$, $\pm 3V_{DC}$, $\pm 2V_{DC}$, $\pm 1V_{DC}$ and 0.

E. Combined Cell Cascade Multilevel Inverter

In this section a different structure of cascade topology is introduced. The structure called combined cascade topology has the highest number of levels due to the number of cells in cascade

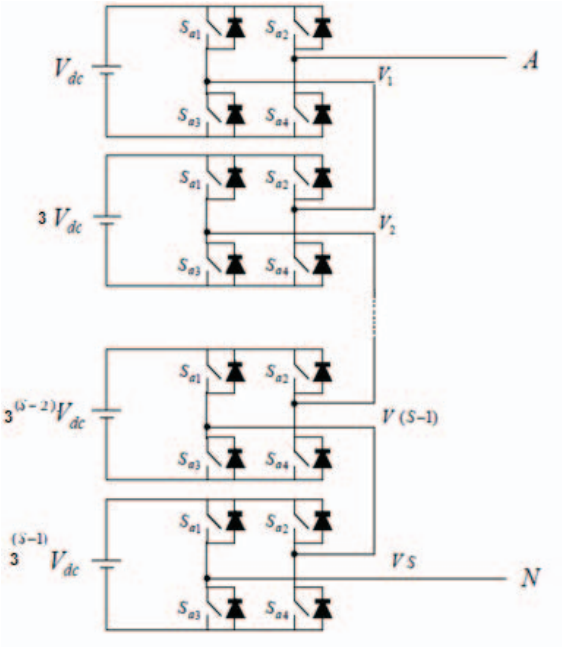

Figure 7. Incremental-reduction cascade H-bridge.

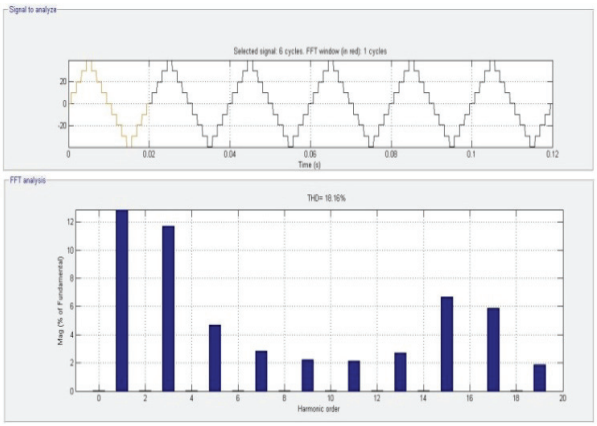

Figure 8. Output waveform and the harmonic chart of an incremental-reduction cascade H-bridge with S=2.

In the structure, each cell increases the number of the original output levels. In fact all the cells are finally gathered together like separated multilevel inverter.

The block diagram of the combined cascade multilevel inverter is presented in Fig. 9. If it uses more capacitors and auxiliary switches, the number of output voltage levels is increased. The number of output voltage levels of each cell is equal to:

$$M=2C+1 \tag{3}$$

Where, C is the number of capacitors.

Output voltage and switching state of the combined cascade multilevel inverter cell is presented in Table I.

Fig. 10 illustrates the output waveform and the harmonic chart of a combined cascade multilevel inverter for S=2 and C =2 for each cell. The output waveform has 25 levels: $\pm 6V_{DC}$, $\pm 5.5V_{DC}$, $\pm 5V_{DC}$, $\pm 4.5V_{DC}$ $\pm 4V_{DC}$, $\pm 3.5V_{DC}$, $\pm 3V_{DC}$, $\pm 2.5V_{DC}$, $\pm 2V_{DC}$, $\pm 1.5V_{DC}$, $\pm 1V_{DC}$, $\pm 0.5V_{DC}$ and 0 .

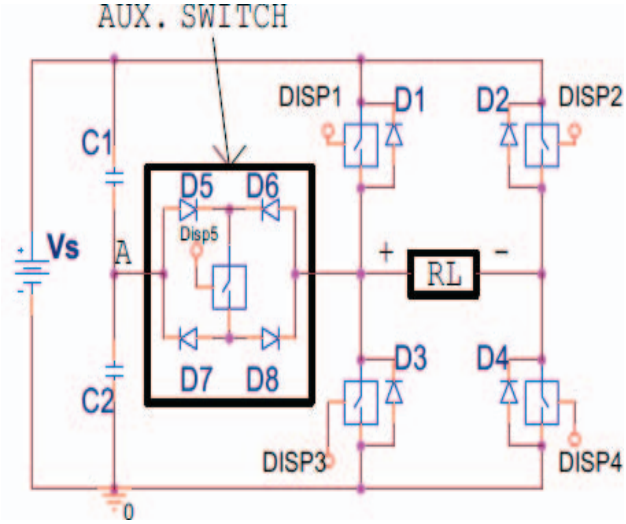

Figure 9. Combined cascade multilevel inverter cell with 5 output voltage levels.

TABLE I
OUTPUT VOLTAGE AND SWITCHING STATE OF COMBINED CASCADE MULTILEVEL INVERTER CELL

Sw1	Sw2	Sw3	Sw4	Sw5	V_{RL}
on	off	off	on	off	Vs
off	off	off	on	On	$V_s/2$
off	off	on	on	off	0
off	on	off	off	on	$-V_s/2$
off	on	on	off	off	$-V_s$

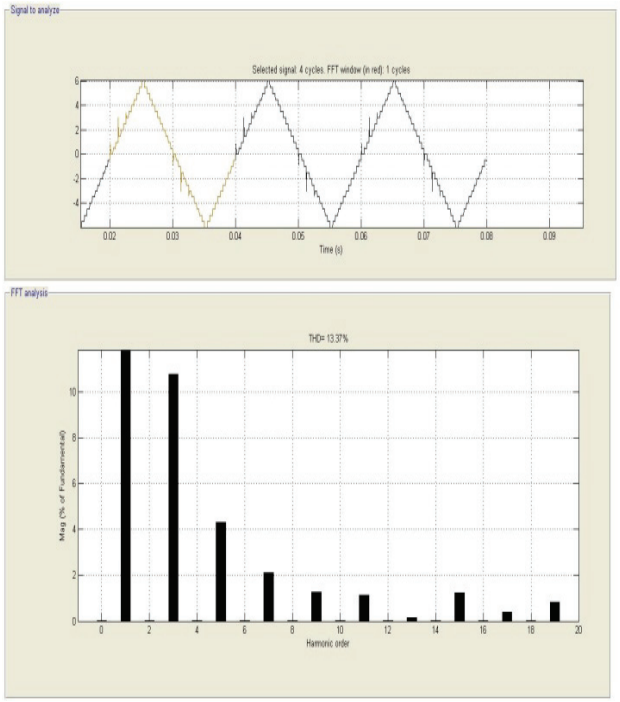

Figure 10. Output waveform and harmonic chart for combined cascade multilevel inverter for S=2.

II. COMPARISON RESULTS

Table II includes the comparison results of various multilevel inverters of the presented paper. The number of output voltage levels of the last topology is increased significantly in comparison with the others and has the highest number of levels due to the number of cells [6]. The number of switches, separated dc sources and the amount of THD [5-7] in each topology, are also shown for S=2 in Table II.

Note that several PWM techniques have been proposed for multilevel PWM control. Here, harmonic elimination PWM technique is used to eliminate lower order harmonics and reduce THD.

III. CONCLUSION

In this paper five multilevel inverter configurations were presented and compared. The multilevel inverters were simulated in MATLAB and the comparison results proved that the combined cascade multilevel inverter had the highest number of output voltage levels due to the number of cells in cascade.

Increasing the number of output voltage levels reduces the lower order harmonics and the THD. It's preferred that the output voltage has no lower order harmonics because their filtering is so hard.

In the incremental cascade H-bridge in which higher DC-link voltage has lower switching frequency, the number of switching devices and as a result the switching losses are reduced.

The incremental cascade I-bridge structure uses a technique in which fewer switches are required so it is so affordable in comparison with the other presented structures.

TABLE II
COMPARISON RESULTS FOR FIVE MULTILEVEL INVERTERS

Topology	levels number	THD	Switch number	Separated DC source
Cascade H-bridge	5	28.98%	8	2
incremental cascade H-bridge	7	21.72%	8	2
incremental cascade I-bridge	7	21.72%	8	2
incremental – reduction cascade H-bridge	9	18.16%	8	2
combined cell cascade	25	13.37%	10	2

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