Discussion

- Increasingly more & more components & features can be integrated on a single chip
- "Perhaps" transitions from single → multicore was just a matter of time.
- But why did it happen in that sequence?
  - Why did pipelining, branch prediction, superscalar issue, & caches come BEFORE multicore ??
    - Power Usage / Heat. [Power wall]
    - Could not make improvements on single core. Low Hanging Fruit Theory

[Memory wall: memory access speed growing too slow]

- Answer: Low Hanging Fruit Theory
  - Famer picks up low hanging fruit bc they require less efforts to pick up, until we run at of low hanging fruit.

• ILP Fruits

- Instruction Level Parallelism (ILP)
  - Pipelining: RISC, CISC w/ RISC backend
  - Superscalar
  - Out of Order execution
- Memory Hierarchy (Caches)
  - Exploiting spatial & temporal locality
  - Multiple Cache levels

• ILP Technique: Pipelining

A (a load)	IF	ID	EX	MEM	WB		
B		IF	ID	EX	MEM	WB	
C			IF	ID	EX	MEM	WB