

1.5A Dual High-Speed Power MOSFET Drivers

Features

- High Peak Output Current 1.5A
- Wide Operating Range
 - 4.5V to 18V
- High Capacitive Load Drive Capability 1000pF in 25nsec Typ.
- Short Delay Times 30nsec Typ.
- · Matched Rise, Fall and Delay Times
- · Low Supply Current:
 - With Logic "1" Input 1mA
 - With Logic "0" Input 100μA
- Low Output Impedance 7Ω
- Latch-Up Protected: Will Withstand 0.5A Reverse Current
- · Input Will Withstand Negative Inputs Up to 5V
- ESD Protected 4kV
- Pinouts Same as TC426/TC427/TC428

Applications

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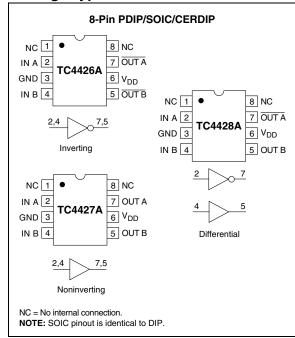
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Device Selection Table

Part Number	Package	Temp. Range
TC4426ACOA	8-Pin SOIC	0°C to +70°C
TC4426ACPA	8-Pin PDIP	0°C to +70°C
TC4426AEOA	8-Pin SOIC	-40°C to +85°C
TC4426AEPA	8-Pin PDIP	-40°C to +85°C
TC4426AMJA	8-Pin CERDIP	-55°C to +125°C
TC4427ACOA	8-Pin SOIC	0°C to +70°C
TC4427ACPA	8-Pin PDIP	0°C to +70°C
TC4427AEOA	8-Pin SOIC	-40°C to +85°C
TC4427AEPA	8-Pin PDIP	-40°C to +85°C
TC4427AMJA	8-Pin CERDIP	-55°C to +125°C
TC4428ACOA	8-Pin SOIC	0°C to +70°C
TC4428ACPA	8-Pin PDIP	0°C to +70°C
TC4428AEOA	8-Pin SOIC	-40°C to +85°C
TC4428AEPA	8-Pin PDIP	-40°C to +85°C
TC4428AMJA	8-Pin CERDIP	-55°C to +125°C

Package Type

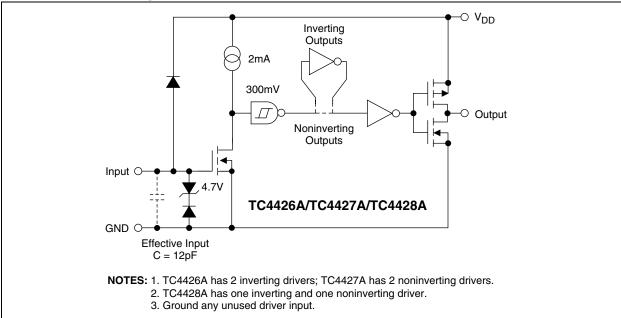


General Description

The TC4426A/TC4427A/TC4428A are improved versions of the earlier TC426/TC427/TC428 family of buffer/drivers (with which they are pin compatible). They will not latch up under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (of either polarity) occurs on the ground pin. They can accept, without damage or logic upset, up to 500mA of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against up to 4kV of electrostatic discharge.

As MOSFET drivers, the TC4426A/TC4427A/TC4428A can easily switch 1000pF gate capacitances in under 30nsec, and provide low enough impedances in both the ON and OFF states to ensure the MOSFET's intended state will not be affected, even by large transients.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage+22V Input Voltage, IN A or IN B
(V _{DD} + 0.3V) to (GND – 5V)
Package Power Dissipation (T _A ≤ 70°C)
PDIP 730mW
CERDIP 800mW
SOIC 470mW
Package Thermal Resistance
CERDIP R _{0.J-A}
CERDIP R _{0J-C} 50°C/W
PDIP R _{θJ-A} 125°C/W
PDIP R _{0J-C}
SOIC R _{0J-A} 155°C/W
SOIC R _{0.J-C} 45°C/W
Operating Temperature Range
C Version0°C to +70°C
E Version40°C to +85°C
M Version55°C to +125°C
Storage Temperature Range65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC4426A/TC4427A/TC4428A ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Over operating temperature range with $4.5 \text{V} \leq \text{V}_{DD} \leq 18 \text{V}$, unless otherwise noted.						
Symbol	Parameter	Min	Тур	Max	Units	Test Conditions
Input						
V _{IH}	Logic 1, High Input Voltage	2.4	_	_	V	
V_{IL}	Logic 0, Low Input Voltage	_	_	0.8	V	
I _{IN}	Input Current	-1 -10	_	1 10	μА	$0V \le V_{IN} \le V_{DD}$
Output				•		
V _{OH}	High Output Voltage	V _{DD} – 0.025	_	_	V	DC Test
V _{OL}	Low Output Voltage	_	_	0.025	V	DC Test
R _O	Output Resistance	_ _ _	7 7 8	9 10 11	Ω	$I_{OUT} = 10$ mA, $V_{DD} = 18$ V, $T_{A} = +25$ °C 0 °C $\leq T_{A} \leq +70$ °C -40 °C $\leq T_{A} \leq +85$ °C
I _{PK}	Peak Output Current	_	1.5	_	Α	V _{DD} = 18V
I _{REV}	Latch-Up Protection Withstand Reverse Current	0.5	_	_	А	Duty cycle \leq 2%, t \leq 300 μ sec $V_{DD} = 18V$

Note 1: Switching times ensured by design.

Symbol	Parameter	Min	Тур	Max	Units	Test Conditions
Switchin	Switching Time (Note 1)					
t _R	Rise Time	_ _ _	25 27 29	35 40 40	nsec	$T_A = +25^{\circ}C$ $0^{\circ}C \le T_A \le +70^{\circ}C$ $-40^{\circ}C \le T_A \le +85^{\circ}C$, Figure 3-1
t _F	Fall Time	_ _ _	25 27 29	35 40 40	nsec	$T_A = +25^{\circ}C$ $0^{\circ}C \le T_A \le +70^{\circ}C$ $-40^{\circ}C \le T_A \le +85^{\circ}C$, Figure 3-1
t _{D1}	Delay Time	_ _ _	30 33 35	35 40 45	nsec	$T_A = +25^{\circ}C$ $0^{\circ}C \le T_A \le +70^{\circ}C$ $-40^{\circ}C \le T_A \le +85^{\circ}C$, Figure 3-1
t _{D2}	Delay Time	_ _ _	30 33 35	35 40 45	nsec	$T_A = +25^{\circ}C$ $0^{\circ}C \le T_A \le +70^{\circ}C$ $-40^{\circ}C \le T_A \le +85^{\circ}C$, Figure 3-1
Power Su	ipply					
I _S	Power Supply Current	_	1.0 0.1	2.0 0.2	mA	V _{IN} = 3V (Both inputs) V _{IN} = 0V (Both inputs), V _{DD} = 18V

Note 1: Switching times ensured by design.

2.0 PIN DESCRIPTIONS

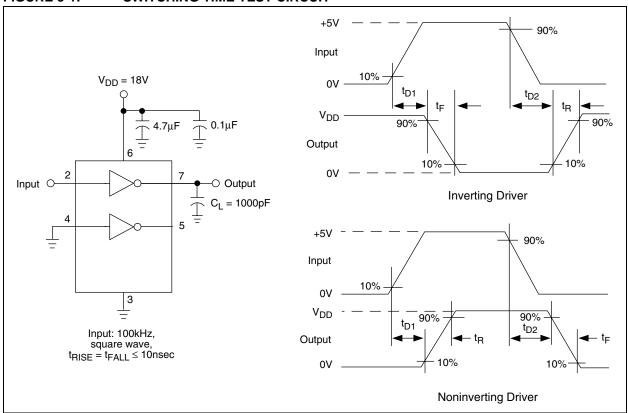
The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin No. (8-Pin PDIP, SOIC, CERDIP)	Symbol	Description
1	NC	No connect.
2	IN A	
3	GND	Ground.
4	IN B	
5	OUT B	
6	V_{DD}	
7	OUT A	
8	NC	No connect.

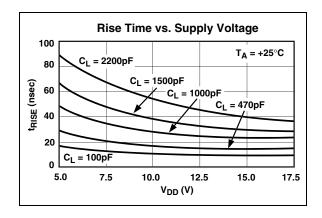
3.0 APPLICATIONS INFORMATION

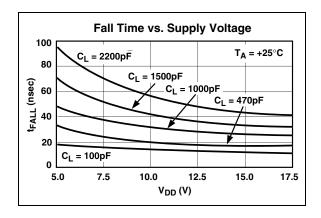
FIGURE 3-1: SWITCHING TIME TEST CIRCUIT

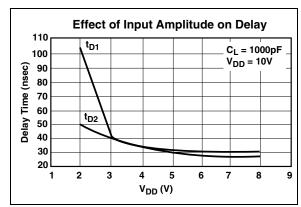


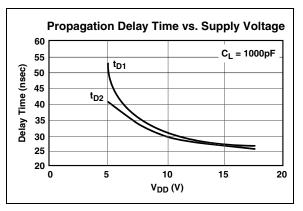
4.0 TYPICAL CHARACTERISTICS

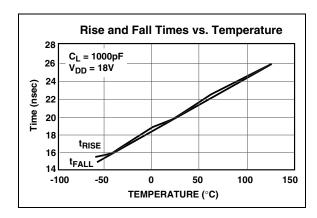
Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

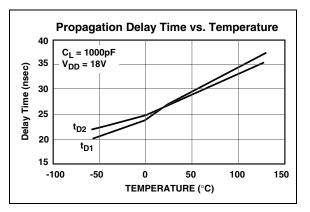




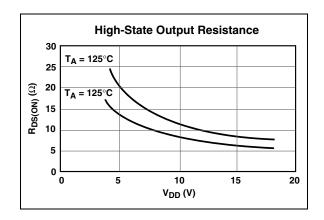


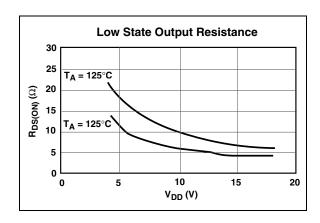


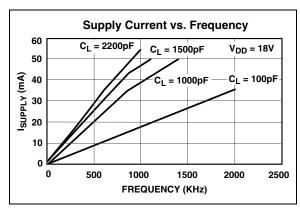


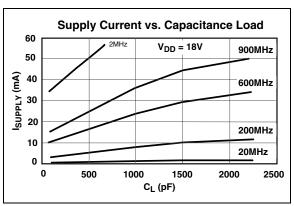


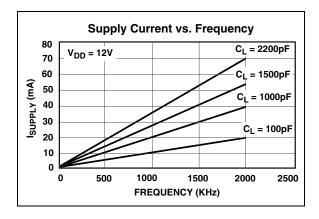
TYPICAL CHARACTERISTICS (CONTINUED)

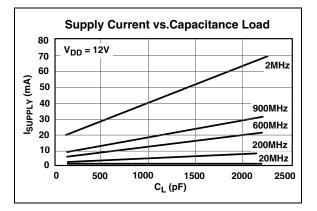




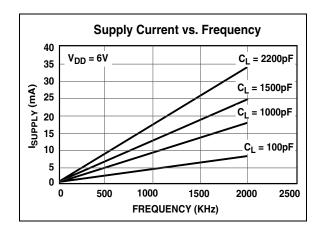


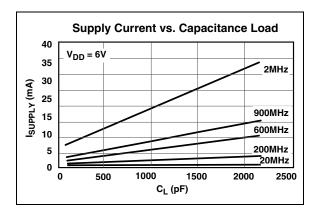


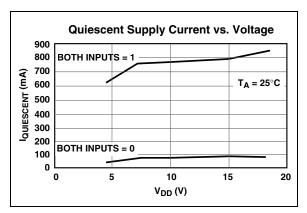


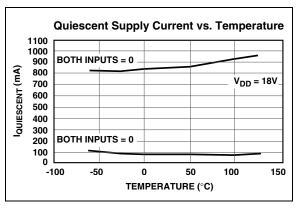


TYPICAL CHARACTERISTICS (CONTINUED)





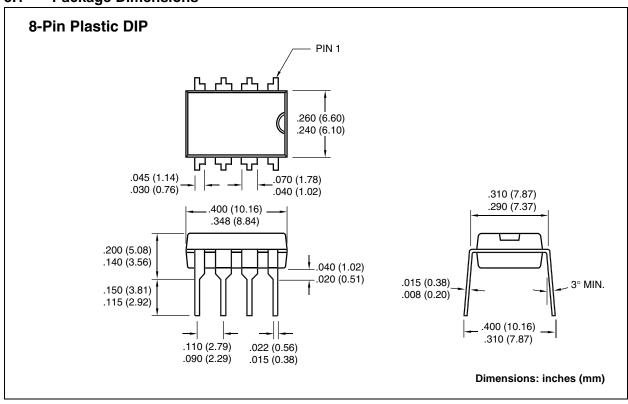


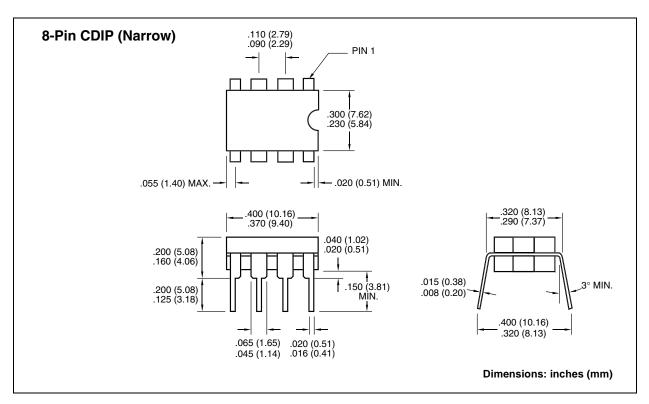


5.0 PACKAGING INFORMATION

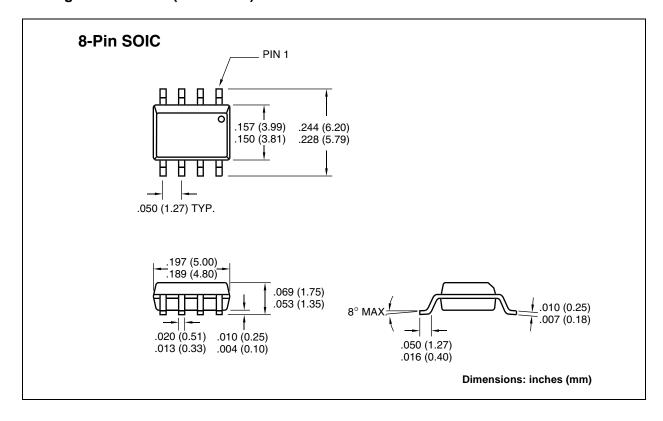
Package marking data not available at this time.

5.1 Package Dimensions





Package Dimensions (Continued)



NOTES:

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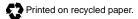
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Co., Ltd., Beijing Liaison Office Unit 915 Bei Hai Wan Tai Bldg.

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Microchip Technology Inc. India Liaison Office Divvasree Chambers 1 Floor, Wing A (A3/A4) No. 11, O'Shaugnessey Road Bangalore, 560 025, India Tel: 91-80-2290061 Fax: 91-80-2290062

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Italy

Microchip Technology SRL Centro Direzionale Colleoni Palazzo Taurus 1 V. Le Colleoni 1 20041 Agrate Brianza Milan, Italy Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom

Arizona Microchip Technology Ltd. 505 Eskdale Road Winnersh Triangle Wokingham Berkshire, England RG41 5TU Tel: 44 118 921 5869 Fax: 44-118 921-5820

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