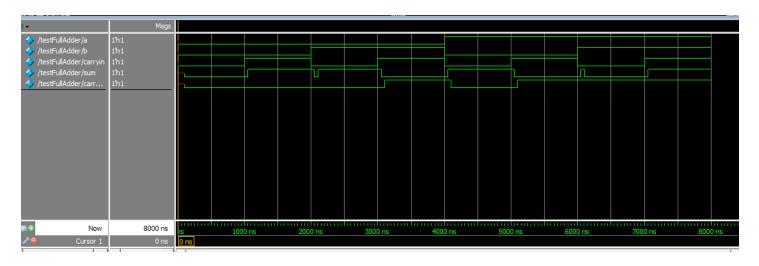
CA Homework 2

Kyle Mayer

9/22/2014

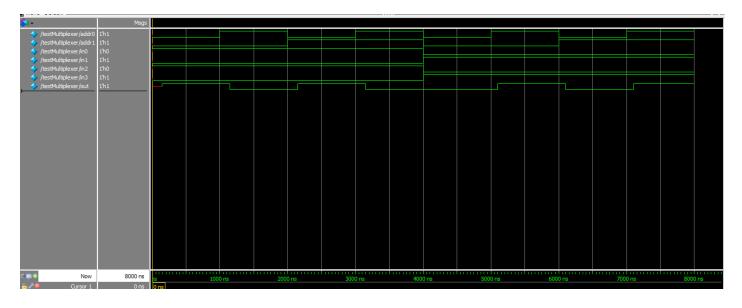
Full Adder:



```
# vsim -gui
# Start time: 13:33:36 on Sep 22,2014
# Loading work.testFullAdder
# Loading work.structuralFullAdder
     b Cin | Cout sum | Expected Output
                    0
                          Zero
                                 (00)
                    1
                        | One
                                 (01)
                        | One
                                 (01)
                    0
                        Two
                                 (10)
        0 1
               0
                                 (01)
                    1
                        | One
               1
                    0
                        | Two
                                 (10)
  1
               1
     1
        0
                    0
                        | Two
                                 (10)
  1
               1
                    1
                        | Three (11)
```

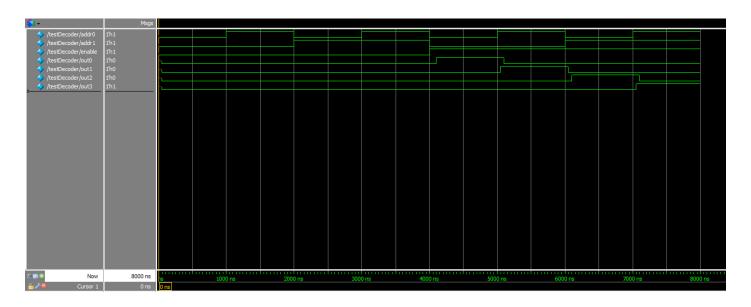
## Multiplexer:

Note: only two combinations of a0,a1,a2,a3 are shown below to reduce the size of the truth table



```
# vsim
# Start time: 20:59:24 on Sep 22,2014
# Loading work.testMultiplexer
# Loading work.structuralMultiplexer
# A1 A0 | in3 in2 in1 in0 | out | Expected Output
     0
               1
                   0
                       1
                             1
                                  Input 0 (1)
  0
           0
               1
                                 | Input 1 (0)
  0
     1
           0
                   0
                       1
                             0
                               | Input 2 (1)
               1
 1
     0
           0
                   0
                             1
                               | Input 3 (0)
# 1
               1
                   0
     1
           0
                         | 0
     0
           1
               0
                  1
                       0
                             0 | Input 0 (0)
# 0
                 1
                         | 1 | Input 1 (1)
# 0
     1 | 1
              0
                     0
                   1
                               | Input 2 (0)
           1
# 1
     0
               0
                       0
                             0
           1
                   1
     1
               0
                       0
                             1
                                  Input 3 (1)
```

## Decoder:



```
# vsim
# Start time: 21:08:17 on Sep 22,2014
# Loading work.testDecoder
# Loading work.structuralDecoder
 En A0 A1 | 00 01 02 03 | Expected Output
               0
                  0
                       | All false
 0
               0
                       | All false
                    0 | All false
           0 0 0
                    0 | All false
    0 0 | 1 0 0
                    0 | 00 Only
 1
    1 0 | 0 1 0
                    0 | 01 Only
    0 1 1
            0 0 1
                    0 | 02 Only
                    1 | 03 Only
```