Clockhands is a newly developed instruction set architecture (ISA) aimed at improving power efficiency by eliminating the need for register renaming. Unlike the **STRAIGHT** ISA, Clockhands allows flexible instruction placement while maintaining a similar instruction count to traditional **RISC** architectures. In evaluations, Clockhands demonstrated a **7.4% reduction in energy consumption** compared to RISC, which increased to **24.4%** when using a wider front-end.

Clockhands is a novel instruction set architecture (ISA) that eliminates the need for register renaming, resulting in a **7.4% reduction in energy consumption** compared to traditional **RISC** architectures. It supports flexible instruction placement, helping to minimize the instruction count. Clockhands performs particularly well on wide-fetch processors, with **FPGA implementation** confirming its efficiency in reducing resource usage.

Clockhands is an instruction set architecture (ISA) that eliminates register renaming by utilizing multiple register groups for operand specification. This approach reduces false dependencies, lowers instruction overhead, and decreases power consumption, all while preserving the efficiency of out-of-order execution.

Clockhands is an instruction set architecture (ISA) that enables efficient out-of-order execution without the need for register renaming. By employing multiple register groups, it reduces instruction count and avoids the inefficiencies present in traditional **RISC** and **STRAIGHT** architectures.