Green University of Bangladesh
Department of Computer Science and Engineering (CSE)

Faculty of Sciences and Engineering

Semester:(Spring, Year:2024), B.Sc. in CSE (Day)

Lab Report NO:

Course Title: Digital Logic Design Lab

Course Code: CSE 204 Section: 231-D1

Lab Experiment Name: Verification of truth tables of the basic Flip-Flops with synchronous and asynchronous modes.

Student Details

	Name	ID
1.	Promod Chandra Das	231002005

Lab Date :

Submission Date :

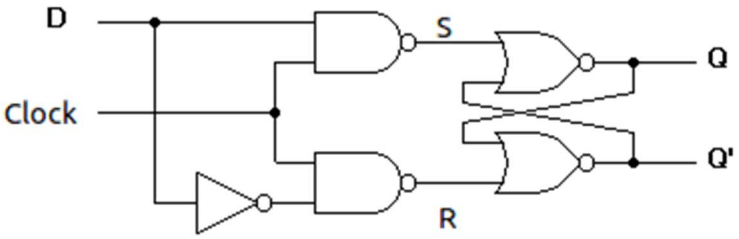
Course Teacher's Name : Md. Shihab Hossain

Lab Report Status

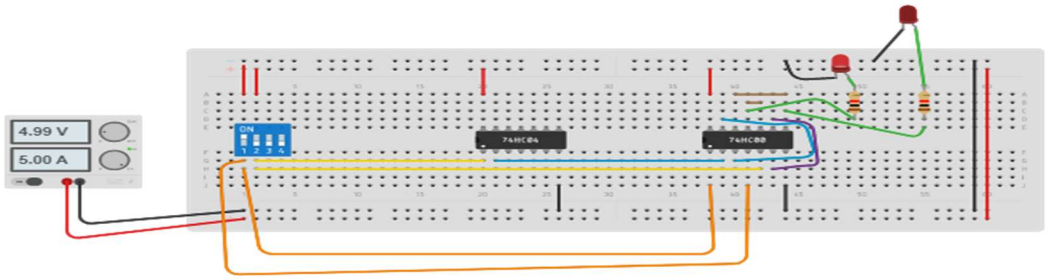
Marks: …… **Signature:.....**

Comments:..... **Date:.....**

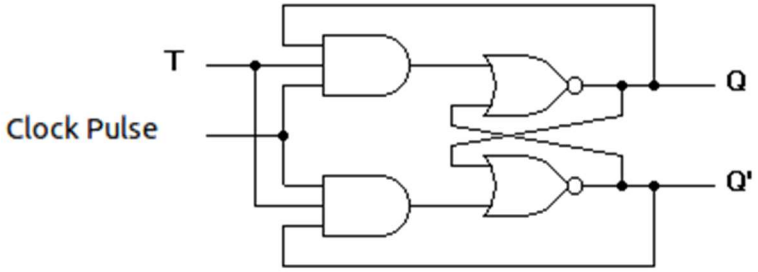
- **Implement D flip-flop and verify with truth table**



Input			Output	
D	reset	clock	Q	Q'
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	0	1



- **Implement T flip-flop and verify with truth table**



T flip-flop

T	Clock	Q	Q'
0	↑	Q	Q'
1	↑	Q'	Q
X	↓	Q	Q'