	Resource	Usage	%
1	Logic utilization (ALMs needed / total ALMs on device)	947 / 41,910	2 %
2	ALMs needed [=A-B+C]	947	
1	[A] ALMs used in final placement [=a+b+c+d]	1,016 / 41,910	2 %
1	[a] ALMs used for LUT logic and registers	432	
2	[b] ALMs used for LUT logic	419	
3	[c] ALMs used for registers	165	
4	[d] ALMs used for memory (up to half of total ALMs)	0	
2	[B] Estimate of ALMs recoverable by dense packing	74 / 41,910	< 1 %
3	[C] Estimate of ALMs unavailable [=a+b+c+d]	5 / 41,910	< 1 %
1	[a] Due to location constrained logic	2	
2	[b] Due to LAB-wide signal conflicts	1	
3	[c] Due to LAB input limits	2	
4	[d] Due to virtual I/Os	0	
3			
4	Difficulty packing design	Low	
5			
6	Total LABs: partially or completely used	166 / 4,191	4 %
1	-- Logic LABs	166	
2	-- Memory LABs (up to half of total LABs)	0	
7			
8	Combinational ALUT usage for logic	1,532	
1	-- 7 input functions	17	
2	-- 6 input functions	222	
3	-- 5 input functions	237	
4	-- 4 input functions	401	
5	-- <=3 input functions	655	
9	Combinational ALUT usage for route-throughs	145	
10	Dedicated logic registers	1,321	
1	-- By type:		
1	-- Primary logic registers	1,194 / 83,820	1 %
2	-- Secondary logic registers	127 / 83,820	< 1 %
2	-- By function:		
1	-- Design implementation registers	1,195	
2	-- Routing optimization registers	126	
11			
12	Virtual pins	0	
13	I/O pins	114 / 342	33 %
1	-- Clock pins	4 / 10	40 %
2	-- Dedicated input pins	0 / 33	0 %
14	I/O registers	226	
15			
16	Hard processor system peripheral utilization		
1	-- Boot from FPGA	1 / 1 (100 %)	

	Resource	Usage	%
2	-- Clock resets	1 / 1 (100 %)	
3	-- Cross trigger	0 / 1 (0 %)	
4	-- S2F AXI	1 / 1 (100 %)	
5	-- F2S AXI	1 / 1 (100 %)	
6	-- AXI Lightweight	1 / 1 (100 %)	
7	-- SDRAM	1 / 1 (100 %)	
8	-- Interrupts	0 / 1 (0 %)	
9	-- JTAG	0 / 1 (0 %)	
10	-- Loan I/O	0 / 1 (0 %)	
11	-- MPU event standby	0 / 1 (0 %)	
12	-- MPU general purpose	0 / 1 (0 %)	
13	-- STM event	0 / 1 (0 %)	
14	-- TPIU trace	1 / 1 (100 %)	
15	-- DMA	0 / 1 (0 %)	
16	-- CAN	0 / 2 (0 %)	
17	-- EMAC	1 / 2 (50 %)	
18	-- I2C	0 / 4 (0 %)	
19	-- NAND Flash	0 / 1 (0 %)	
20	-- QSPI	0 / 1 (0 %)	
21	-- SDMMC	1 / 1 (100 %)	
22	-- SPI Master	0 / 2 (0 %)	
23	-- SPI Slave	0 / 2 (0 %)	
24	-- UART	1 / 2 (50 %)	
25	-- USB	0 / 2 (0 %)	
17			
18	Global signals	3	
19	M10K blocks	7 / 553	1 %
20	Total MLAB memory bits	0	
21	Total block memory bits	38,080 / 5,662,720	< 1 %
22	Total block memory implementation bits	71,680 / 5,662,720	1 %
23	Total DSP Blocks	0 / 112	0 %
24	Fractional PLLs	0 / 6	0 %
25	Global clocks	3 / 16	19 %
26	Quadrant clocks	0 / 66	0 %
27	Horizontal periphery clocks and Vertical periphery clocks	0 / 18	0 %
28	SERDES Transmitters	0 / 100	0 %
29	SERDES Receivers	0 / 100	0 %
30	JTAGs	0 / 1	0 %
31	ASMI blocks	0 / 1	0 %
32	CRC blocks	0 / 1	0 %
33	Remote update blocks	0 / 1	0 %
34	Hard IPs	0 / 1	0 %
35	Standard RX PCSs	0 / 6	0 %

	Resource	Usage	%
36	HSSI PMA RX Deserializers	0 / 6	0 %
37	Standard TX PCSs	0 / 6	0 %
38	HSSI PMA TX Serializers	0 / 6	0 %
39	Channel PLLs	0 / 6	0 %
40	Impedance control blocks	1 / 4	25 %
41	Hard Memory Controllers	1 / 2	50 %
42	Average interconnect usage (total/H/V)	0% / 0% / 1%	
43	Peak interconnect usage (total/H/V)	13% / 11% / 20%	
44	Maximum fan-out	1329	
45	Highest non-global fan-out	198	
46	Total fan-out	12977	
47	Average fan-out	3.32	