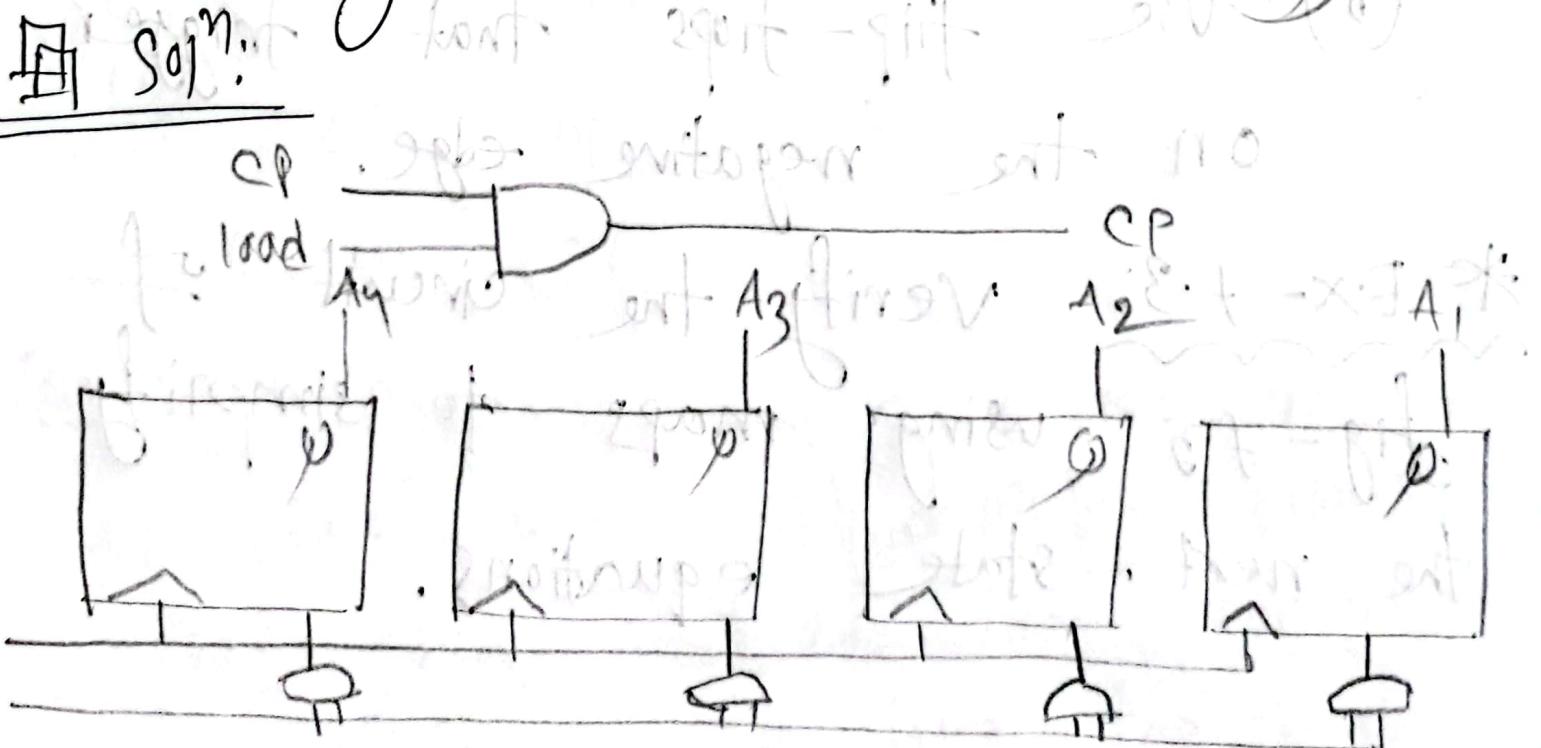


Chapter-07

* Ex-7.1: The register of fig-7.1
transfers the input information into the
flip-flops when the CP input goes through
a positive-edge transition. modify the
circuit so that the input information
is transferred into the register when a
CP through a negative-edge transition,
provided a load input control is equal
to binary 1.



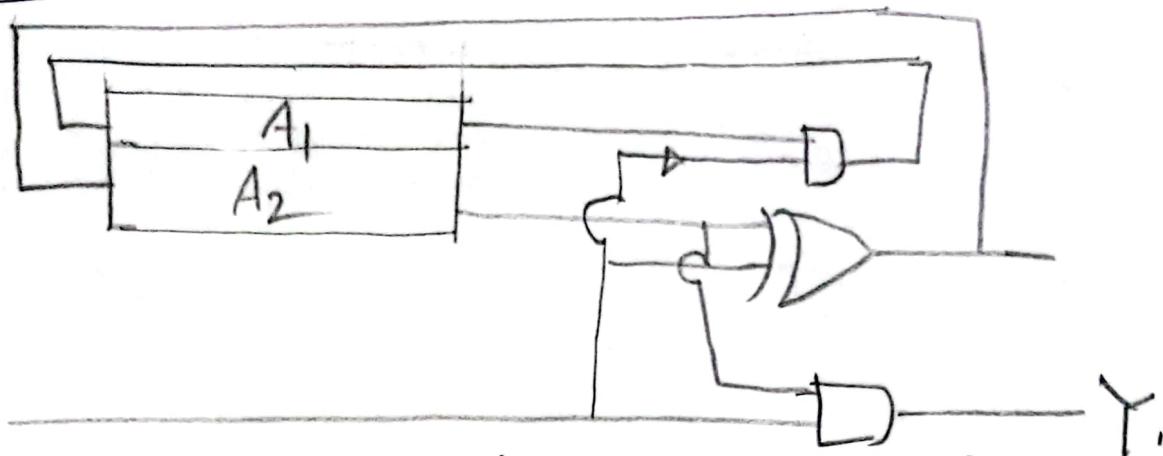
* Ex-7.2: The Register of fig-7.3 loads the inputs during a negative transitions of a clock pulse. What internal changes are necessary for the inputs to be loaded during the positive edge of pulse?

Soln:

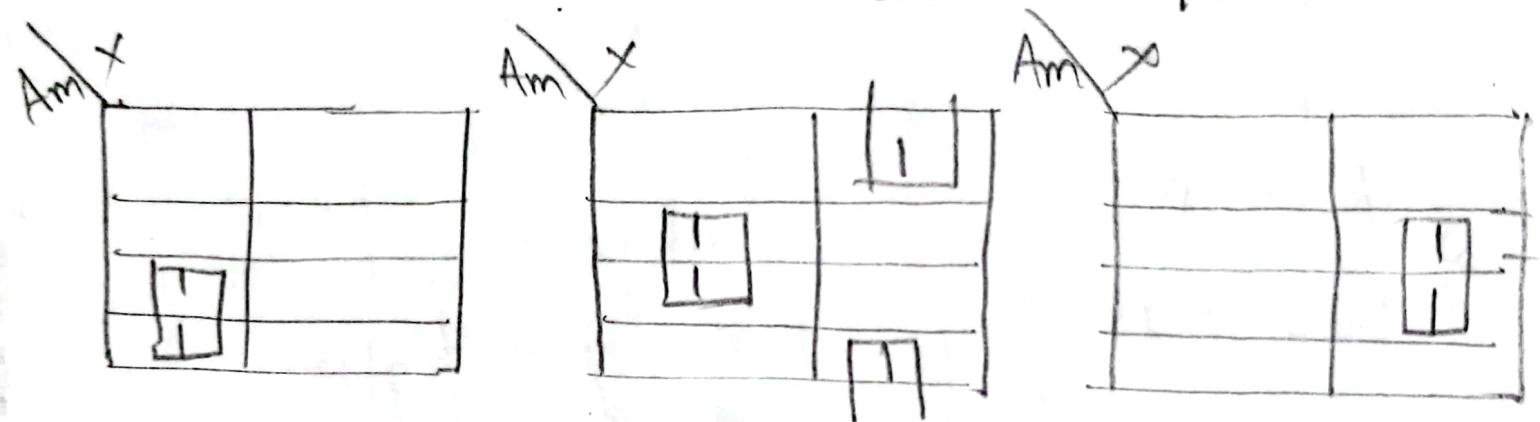
- (a) Change inverter associated with CP into a buffer gate or.
- (b) Use flip-flops that trigger on the negative edge.

* Ex-7.3: Verify the circuit of fig-7.5 using maps to simplify the next-state equations.

Soln:

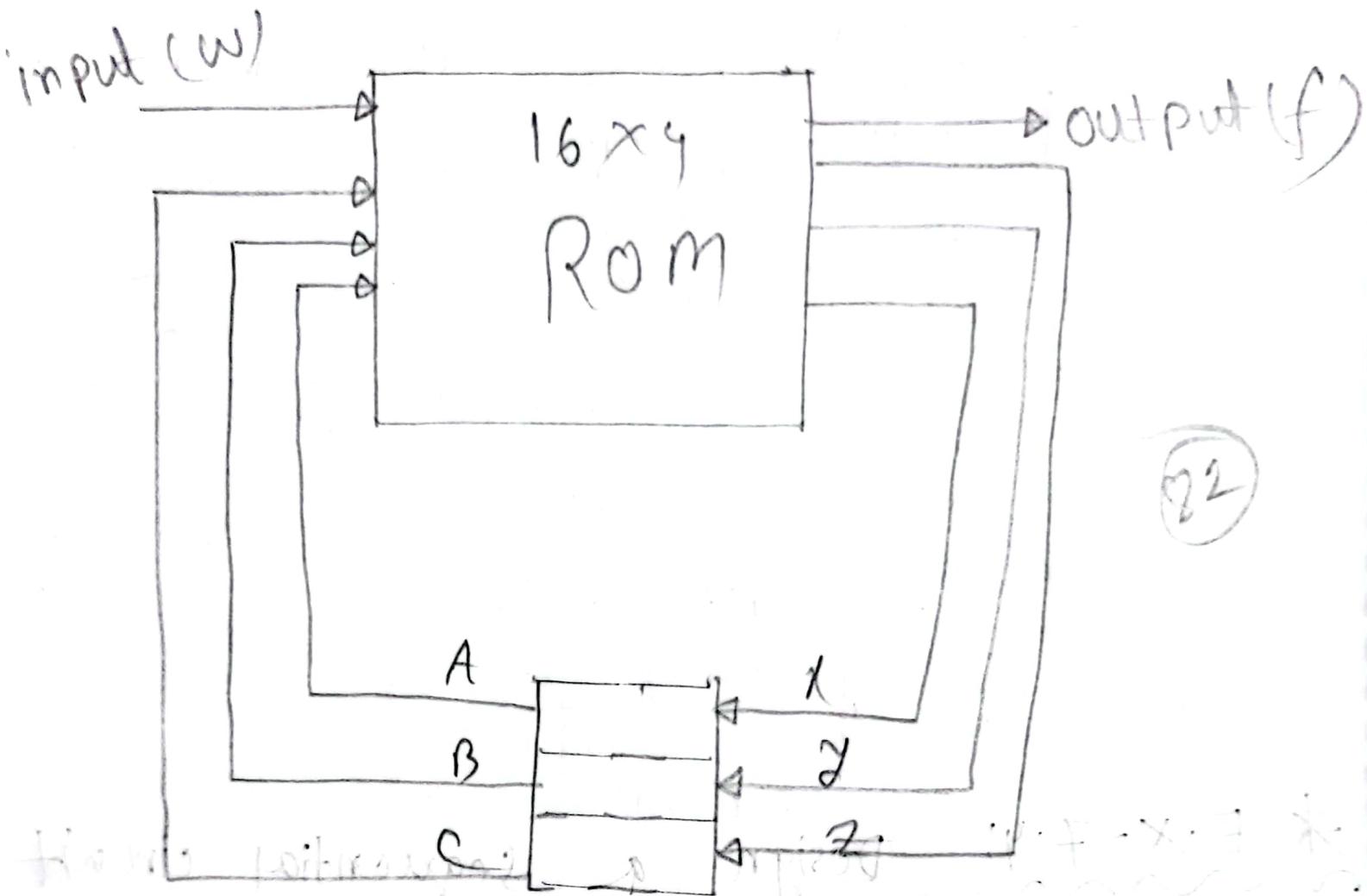


(81)



* Ex-7.4: Design a sequential circuit whose state diagram is given in fig-#27 using a 3-bit Register and a 16×9 ROM.

Soln: Connect a 3-bit Register and a 16×9 ROM as depicted below. Treat each bit of the register as a D flip-flop and design the circuit.



~~Home laboratory~~ using 3-bit serial
bit register file a given problem.

* Ex-7.5: The content of a 4-bit
shift register is initially 1101. The
register is shifted six times to
the right, with the serial input being
10101. What is the content of the
register after each shift?

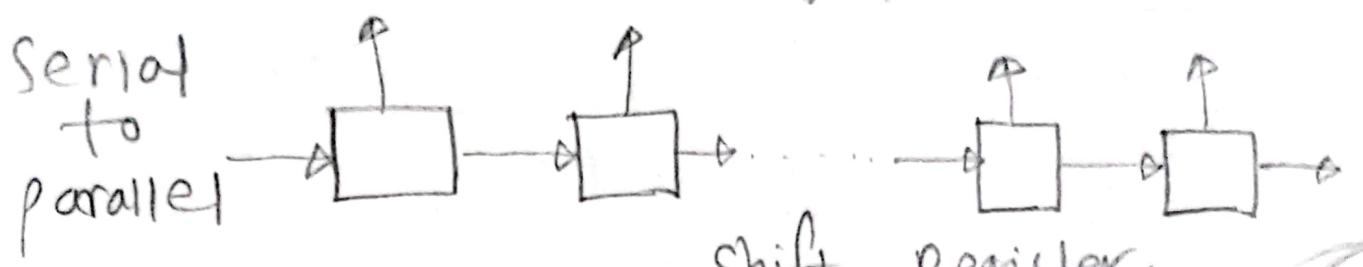
Ex 7.6:

Timing pulse	Serial input	Shift gets (cont)
initial value (T_0)	10110	1101
After (T_1)	1011	1110
T_2	1011	0111
T_3	101	1011
T_4	10	1101
T_5	1	1110
T_6		1011

(Q3)

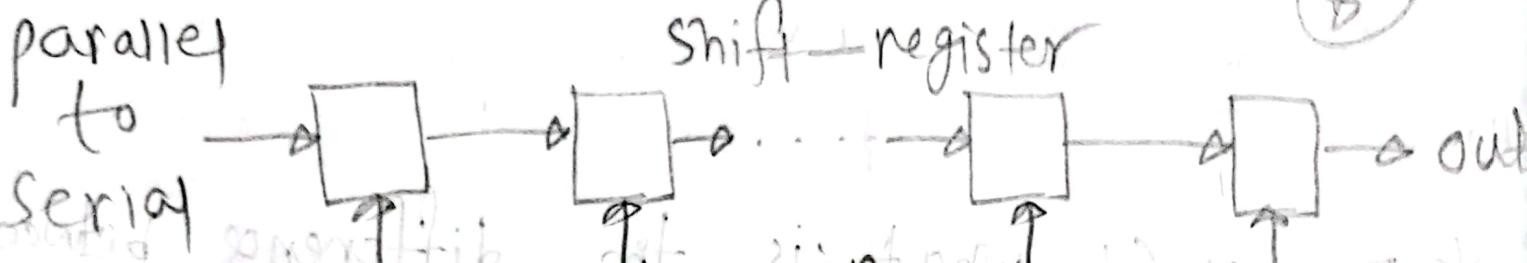
* Ex-7.6: what is the difference between serial and parallel transfer? what type of register is used in each case?

Soln: In a serial transfer, the data is transferred in sequence one bit at a time (per clock period, if it is synchronous), whereas in a parallel transfer, all bits are transferred at the same time. A shift register can be used to do serial to parallel or parallel to serial transfer as depicted below.



Shift - Register.

(B4)

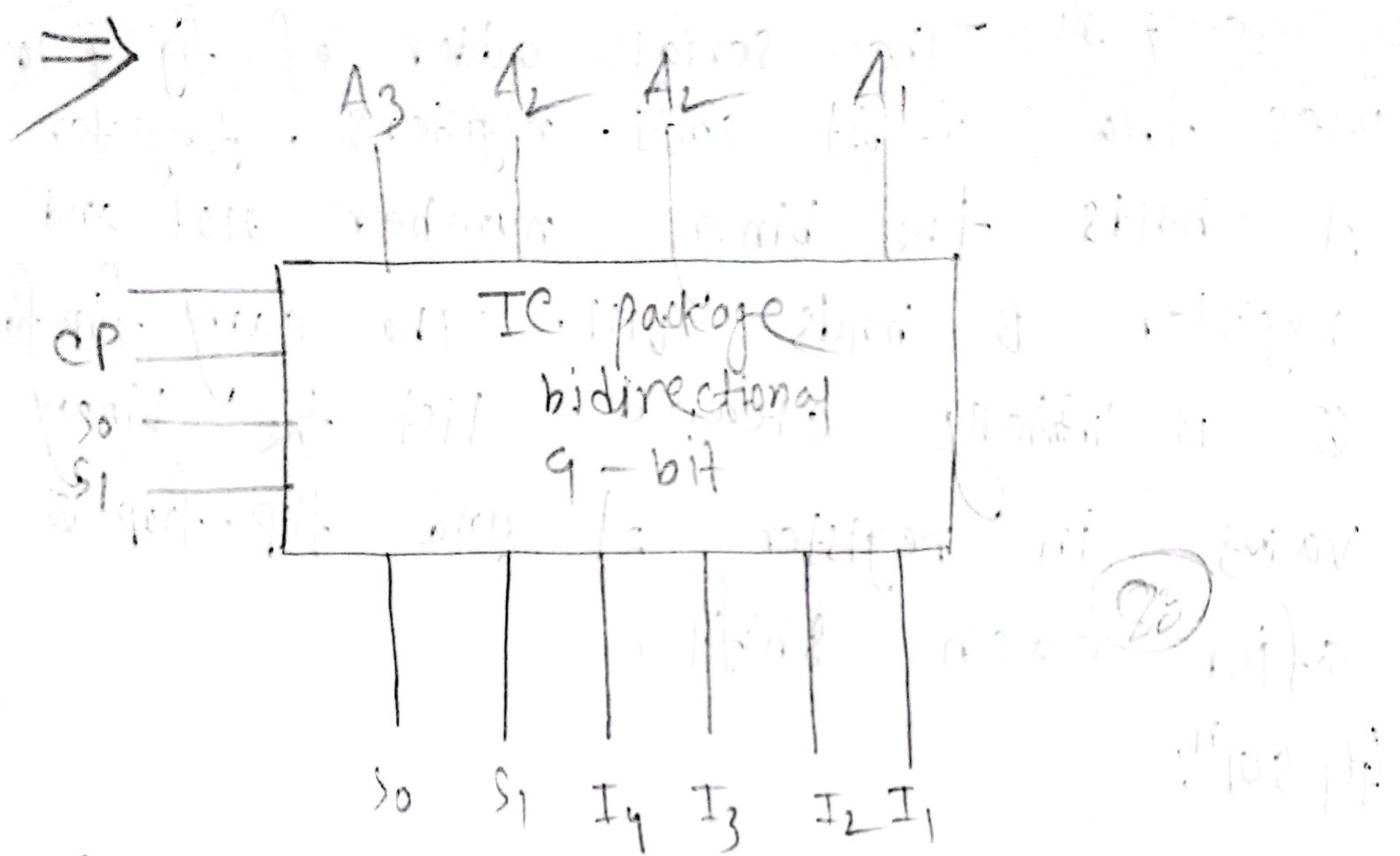


Shift - register

* Ex-7.7: The 4-bit bidirectional shift register of fig-7.9 is enclosed within one IC package.

- Draw a block diagram of the IC showing all inputs and outputs.
- Draw a block diagram using three ICs to produce a 12-bit bidirectional shift register.

Soln: S_R = Serial input for shift right
 S_L = Serial input for shift left
 S_1 = Selection line
 S_0 = Selection line



\Rightarrow

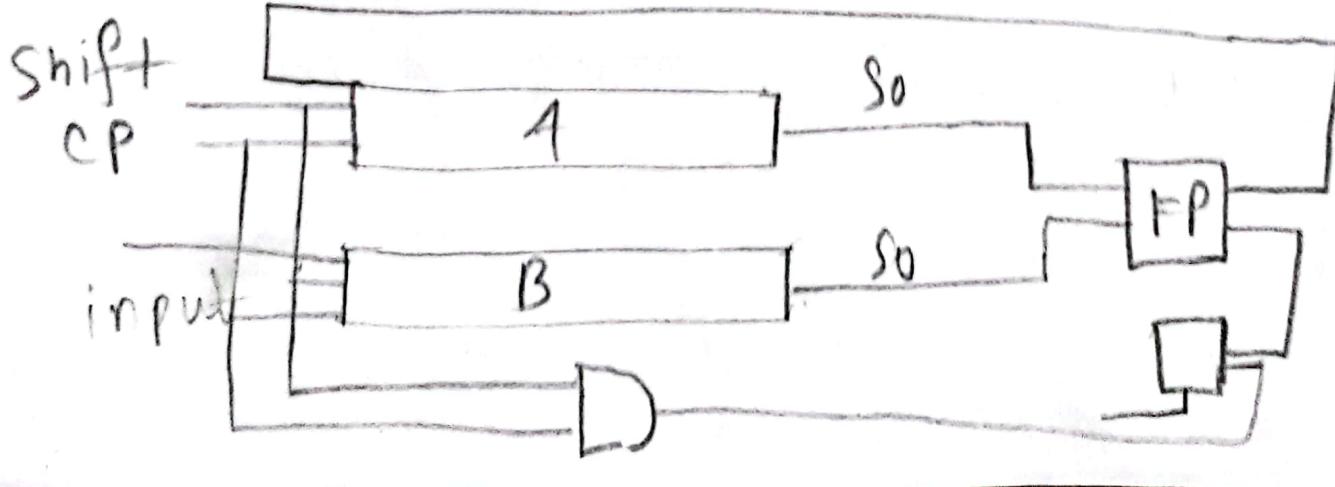
S_1	S_0	
0	0	—
0	1	Shift Right
1	0	Shift register
1	1	parallel load

* Ex-7.8: The serial adder of fig-7.10 uses two 4-bit shift registers. Register A holds the binary number 0101 and register B holds 0111. The carry flip-flop is initially cleared. List the binary values in register A and flip-flop after each shift.

Soln:

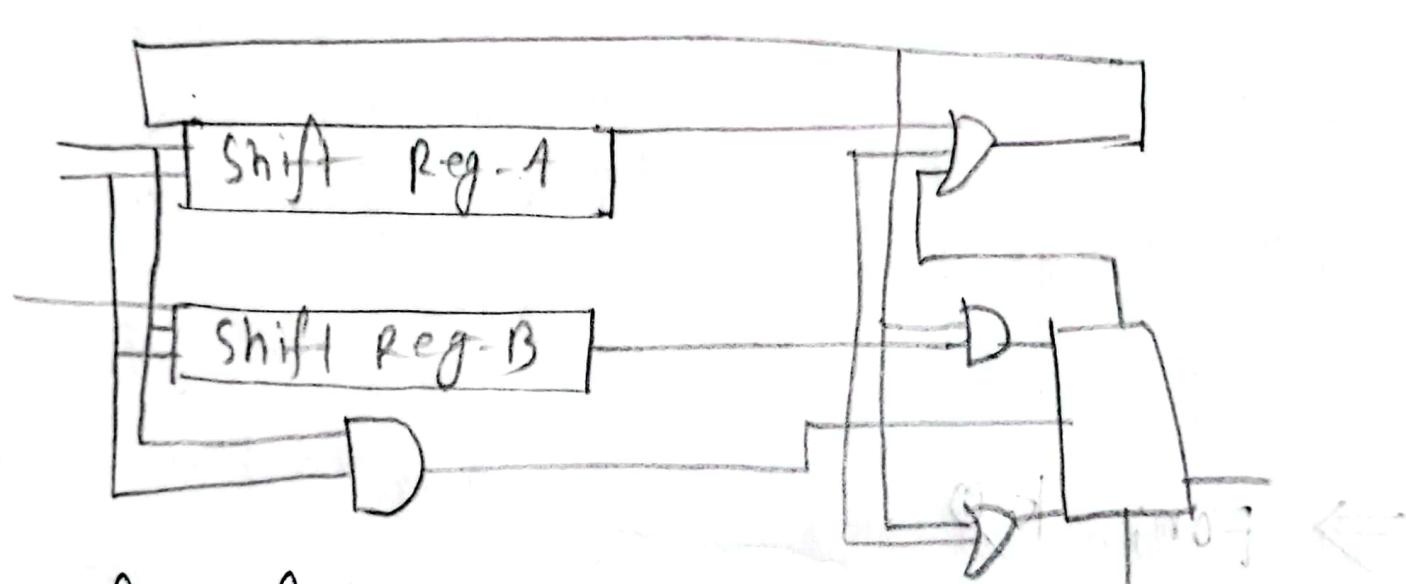
(86)

pulse	Reg-A		Reg-B
initial	0101	011	0
After T1	0010	011	1
T2	0001	01	1
T3	1000	0	1
T4	1100		0



*Ex-7.9. what changes are needed in the circuit of fig-7.11 to convert it to a circuit that subtracts the content of B from the content of A?

桶 SOLⁿ:



\Rightarrow flip-flop excitation table subscription:

X	Y	Z	BD	SO	TIO
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	1	1	X
0	1	1	1	X	0
1	0	0	0	0	X
1	0	1	0	X	1
1	1	0	0	0	0
1	1	1	1	X	X

\Rightarrow For: D

		00	01	11	10
		0	1	1	1
x/y	0	1	X	X	X
	1	X	1	X	

$$D = 1 \oplus y \oplus z$$

\Rightarrow For: $J\varnothing$

		00	01	11	10
		0	X	X	1
x/y	0	1	X	X	
	1	X	1	X	

$$J\varnothing = x'y$$

\Rightarrow For: $K\varnothing$

		00	01	11	10
		0	X		X
x/y	0	X	1		
	1	X	1		X

$$\begin{aligned} K\varnothing &= xy' \\ &= (x' + y)' \end{aligned}$$

(Q8)

Ex-7: A flip-flop has a 20-ns delay from the time its CP input goes from 0 to 1 to the time the output is complemented. What is the maximum delay in a 10-bit binary ripple counter that uses these flip-flops? What is the maximum frequency the counter can operate at reliably?

Sol:

$$\Rightarrow \text{Total delay} = \text{Number of stages} \times \text{DPS}$$
$$= 10 \times 20 \text{ ns}$$
$$= 200 \text{ ns}$$

$$\Rightarrow \text{maximum frequency} = 1 / \text{maximum delay}$$
$$= 1 / 200 \text{ ns}$$
$$= 5 \text{ MHz}$$

* Ex-7.12: How many flip-flops must be complemented in a 10-bit binary ripple counter to reach the next count after 01111111?

Soln.: Since we are using a binary ripple counter, the carry ripples from one stage to the next, causing the least significant '1' bit to flip. In this case, the least significant '1' bit is the first bit from the right (the LSB). Therefore, only one flip-flop needs to be complemented to reach the next count after 01111111.

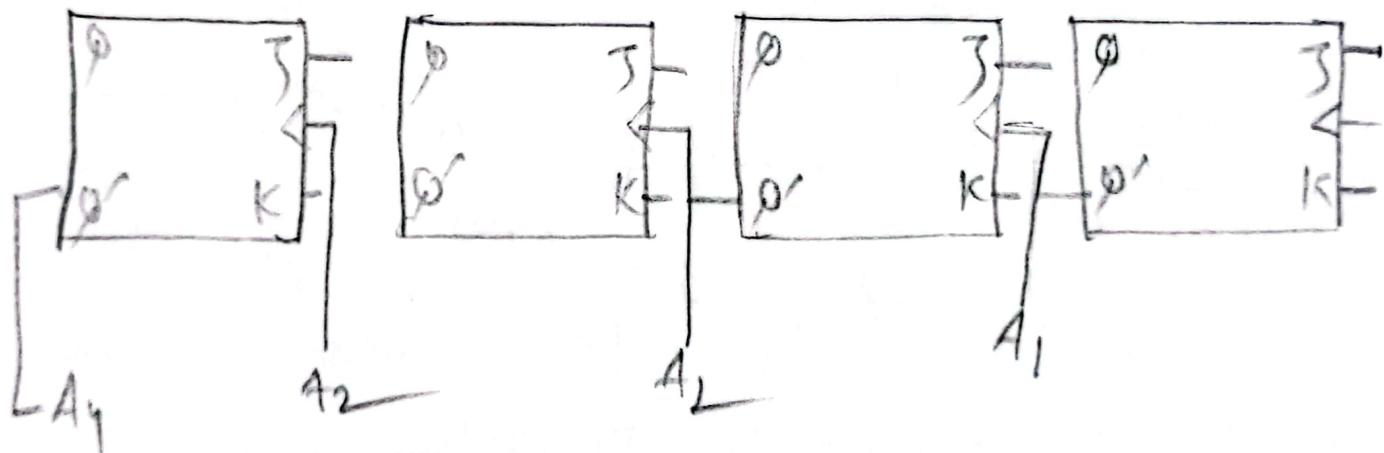
Thus, a single flip-flop must be complemented in the 10-bit binary ripple counter.

* Ex-7.13'. Draw the diagram of a 4-bit binary ripple down-counter using flip-flops that trigger on the

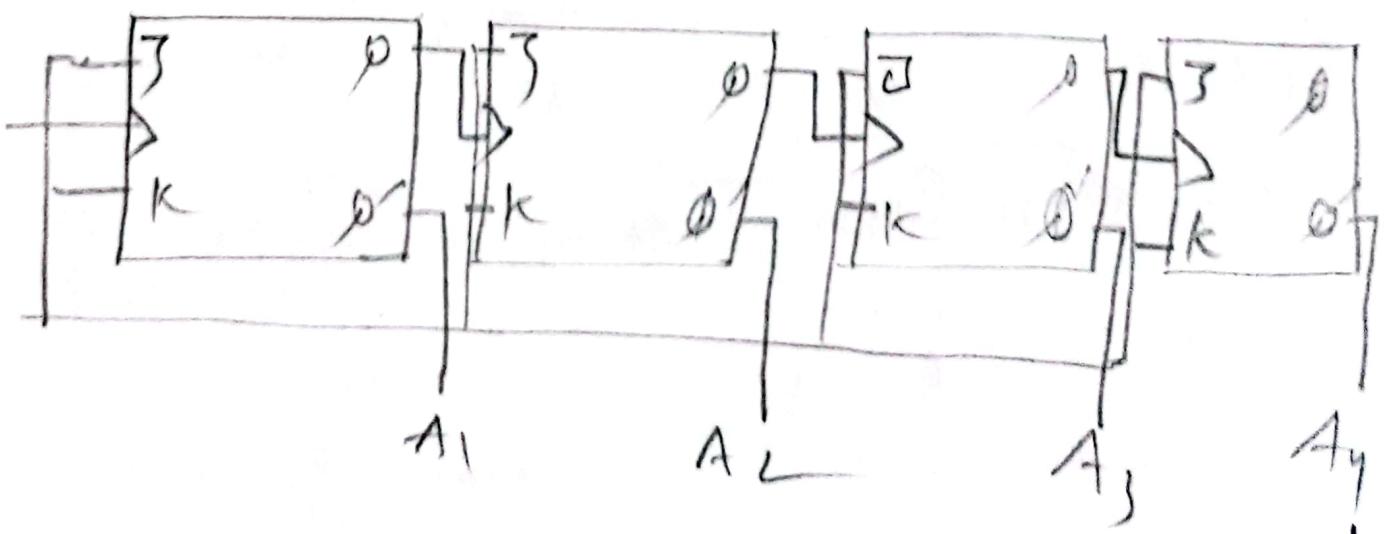
(a) positive-edge transition
(b) negative-edge transition.

Solⁿ:

(a)

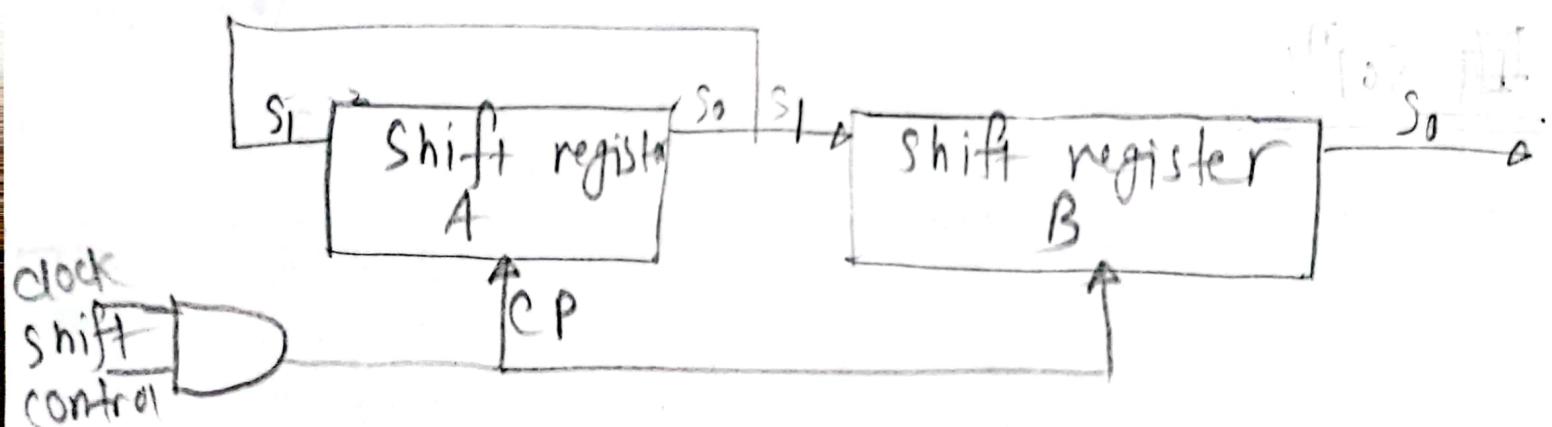


(b)

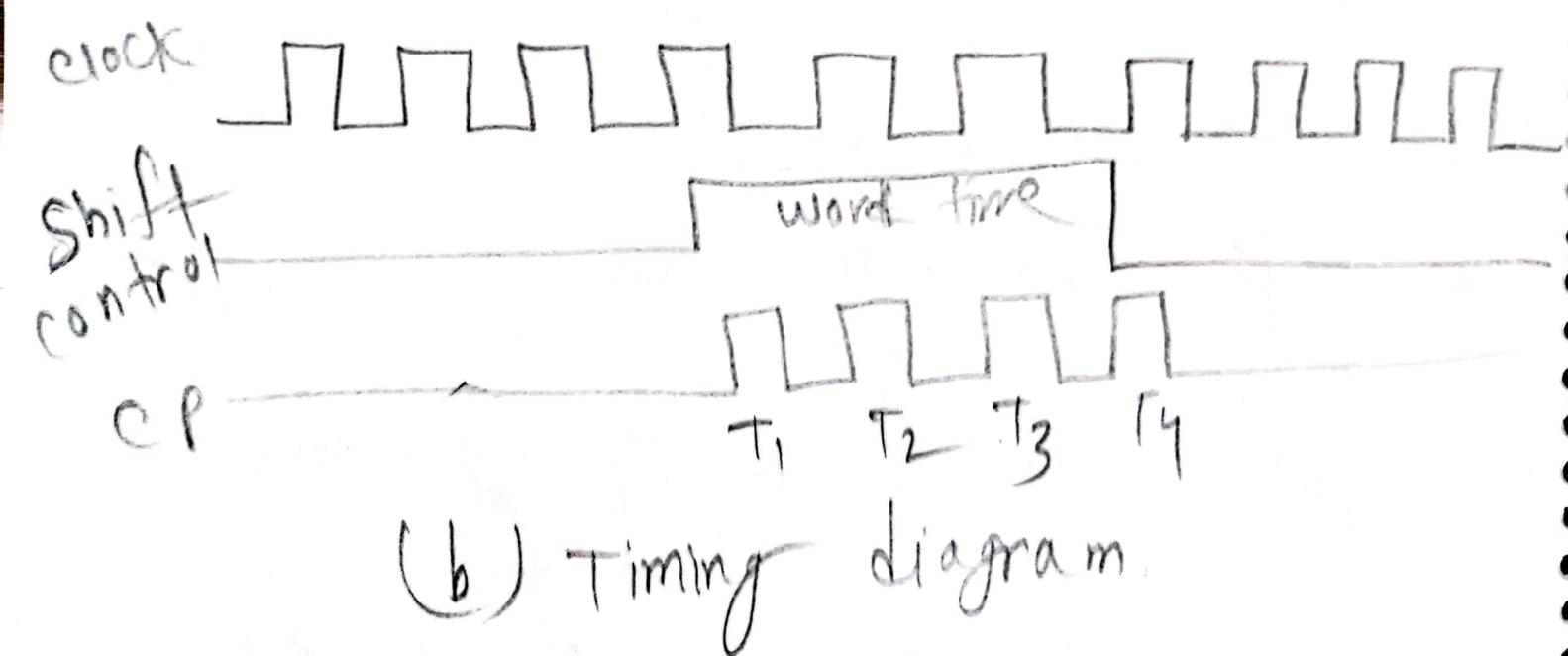


* Ex-7.14: Draw a timing diagram similar to that in Fig-7.15 for the binary ripple counter of fig-7.12.

Ans S01^n:



(a) Block Diagram



(b) Timing diagram.

* Ex - 7.15: Determine the next state for each of the six unused states in the BCD ripple counter. Fig. 7.14. Is the counter self-starting?

Sol:

$$1010 \rightarrow 1011 \rightarrow 0100$$

$$1100 \rightarrow 1101$$

$$1110 \rightarrow 1111 \rightarrow 0000$$

Self-starting.

* Ex - 7.16: The ripple counter shown in fig. P7-18 uses flip-flops that trigger on the negative-edge transition of the CP input. Determine the count sequence of the counter. Is the counter self-starting?

Sol:

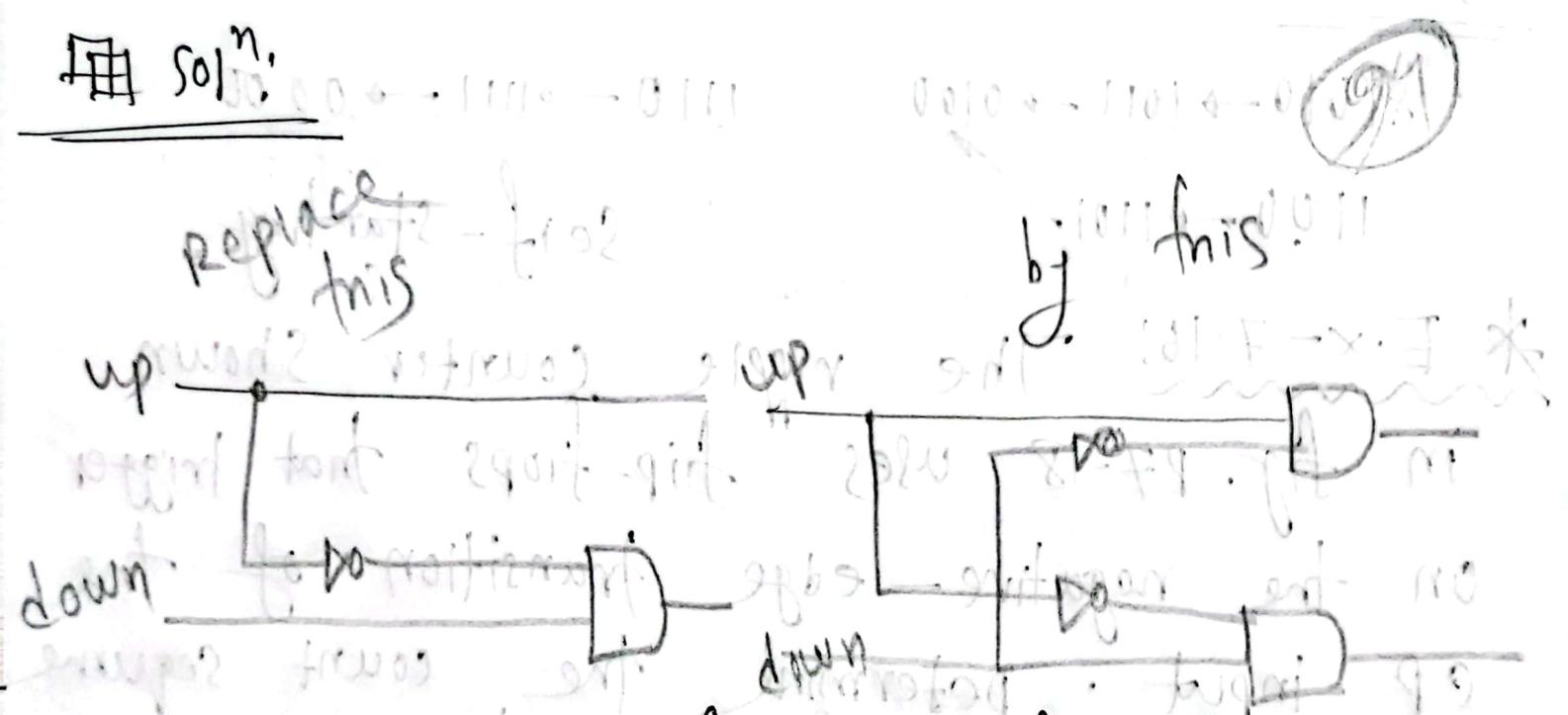
$$000 \rightarrow 0001 \rightarrow 0010 \rightarrow 0101 \rightarrow 1010$$

$$101 \rightarrow 110, 111$$

Not self-starting.

* Ex-7.17: what happens to the counter of fig. 7.18 if both the up and down inputs are equal to 1 at the same time? Modify the circuit so that it will count up if this condition occurs.

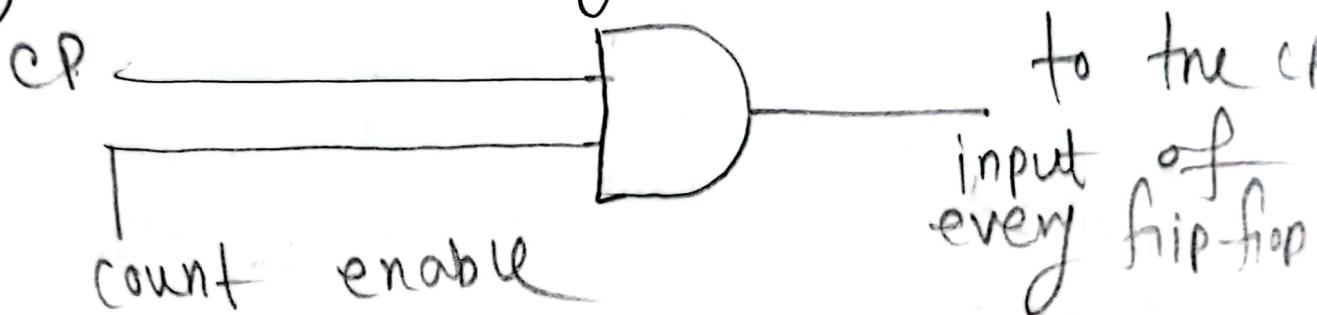
Sol:



* Ex-7.18: Verify the flip-flop input functions of the synchronous BCD counter specified in table 7.5. Draw the logic diagram of the BCD counter and include a count-enable control input.

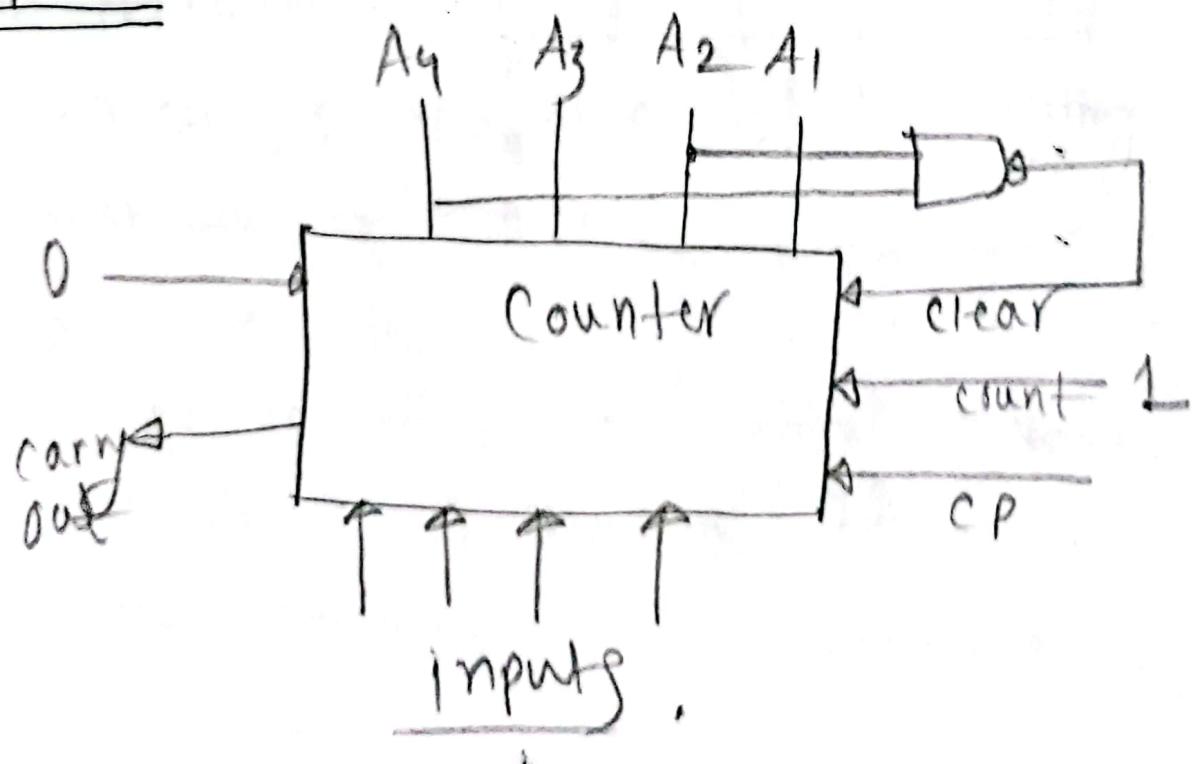
Ques:

- (1) construct the k-map of each input function and simplify it.
- (2) provide the counter enable input by using the following circuit.



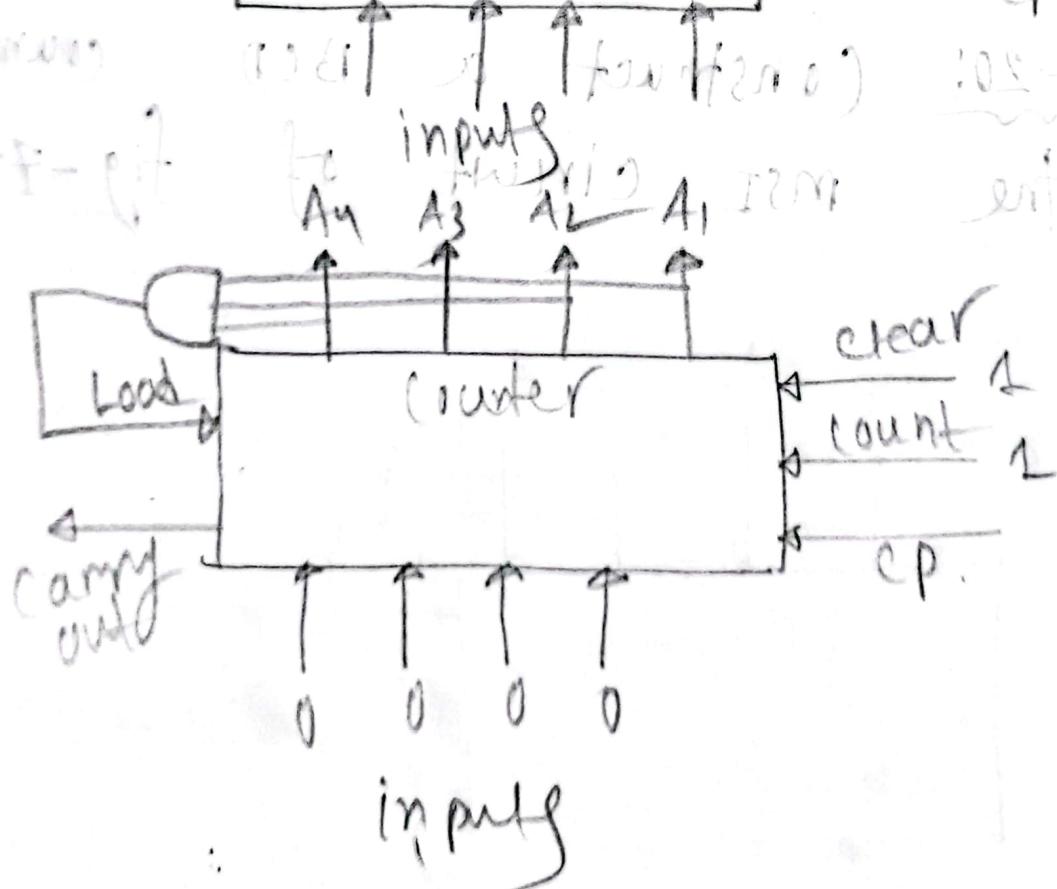
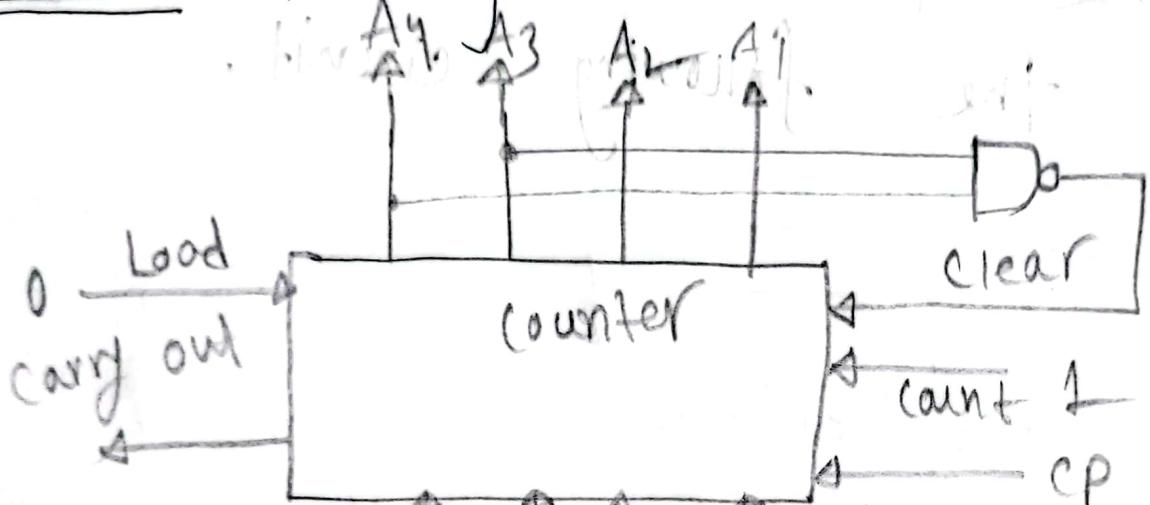
* Ex-7.20: Construct a BCD counter using the MSI circuit of fig-7.19.

Soln:



* Ex-7.21: Construct a mod-12 counter using the MSI circuit specified in fig-7. Give four alternatives.

Soln: two possible designs



②6

⇒ Register:

- # The register is a group of memory elements that work together as a single unit.
- # It is used in microprocessors digital, digital computer.

⇒ Flip-flop:

- # The memory element used in clocked sequential circuit is called flip-flop
- # It is used in digital computers.

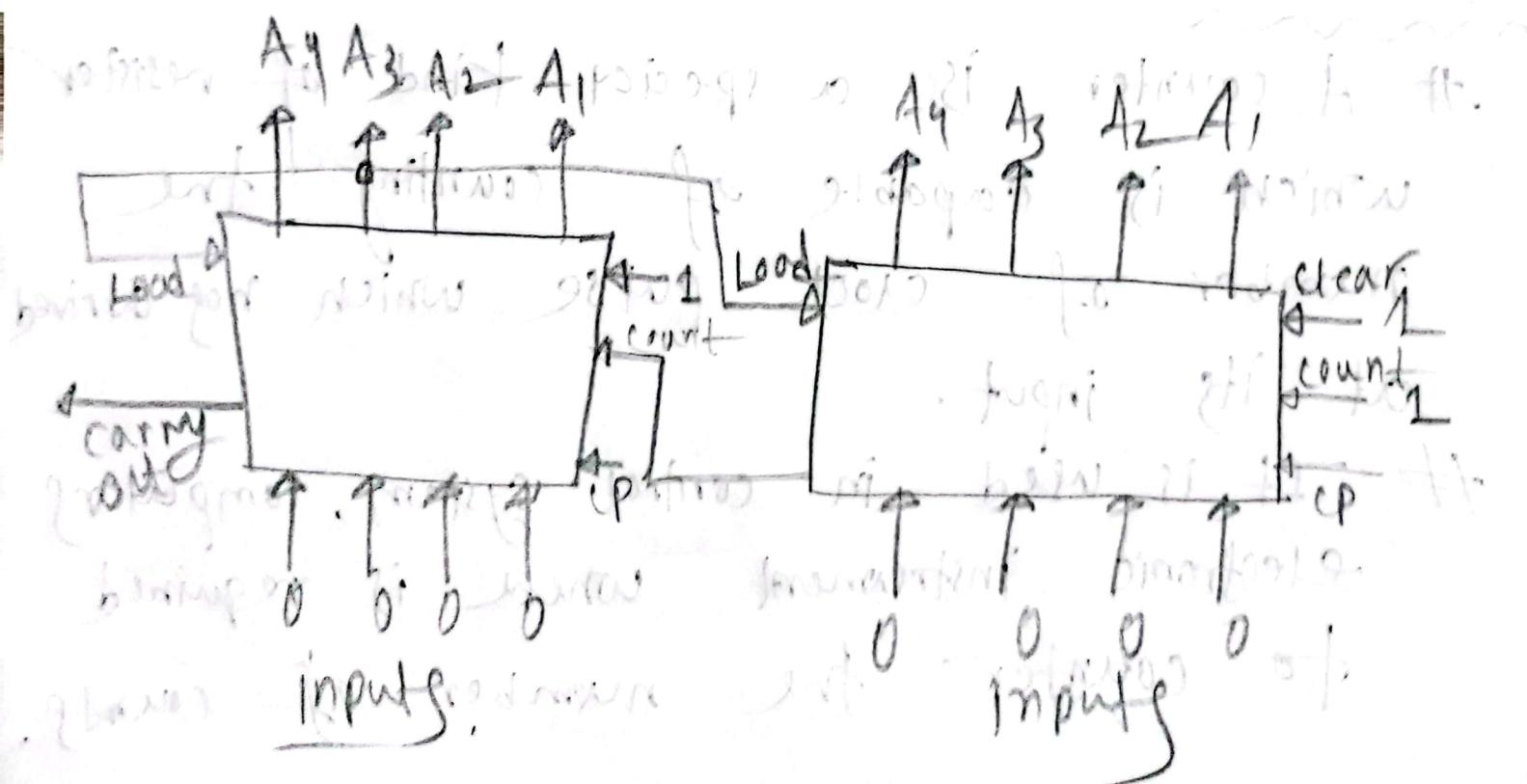
⇒ counter:

- # A counter is a special kind of register which is capable of counting the number of clock pulse which has arrived at its input.
- # It is used in control system, computers, electronic instrument where it is required to count the number of counts.

→ memory:

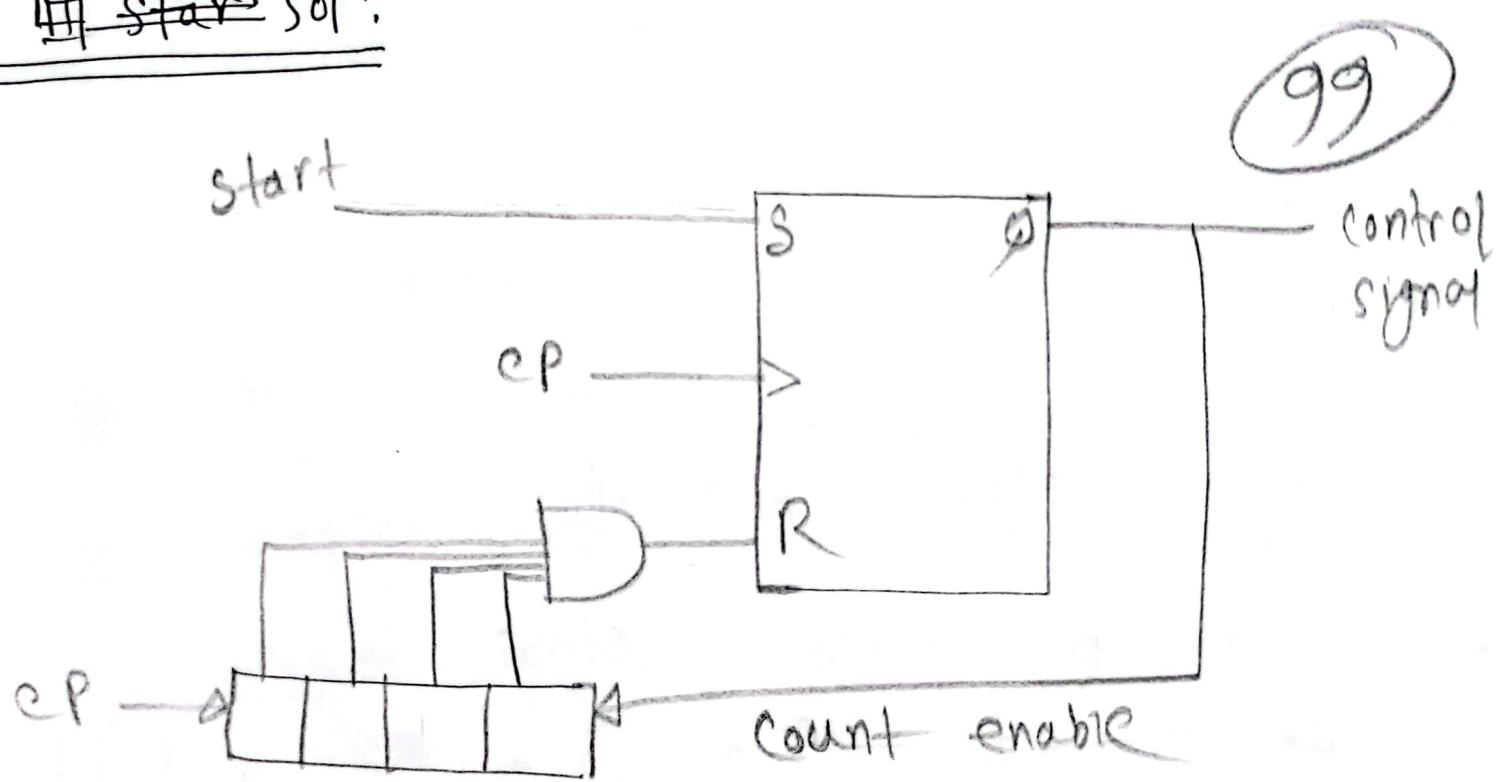
A ~~unit~~ memory unit is a collection of storage registers together with the associated circuits needed for transfer information in and out of the registers.

* Ex-7.22: Using two MSI circuits as specified in fig. 7-19, construct a binary counter that counts from 0 to binary 64 (specifying all logic levels).
Soln.



* Ex-7.23: Using the stop variable from fig-7.21 as a start signal, construct a second wind-time control that stays on for a period of 16 clock pulses.

start Solⁿ:



* Ex-7.26: Complete the design of the Johnson counter of fig. 7-23, showing the outputs of the eight timing signals.

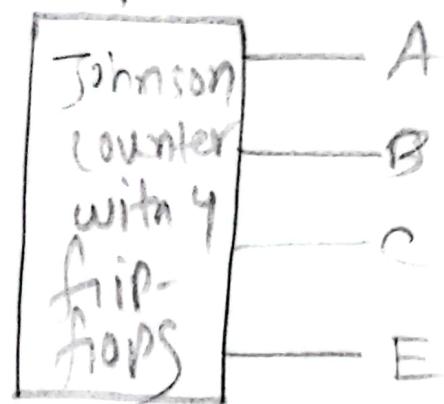
Q1: Sol:

(100)

Explain how the flip-flop

is used for this

using logic



* Ex-7.27: List the eight unused states in the switch-ring counter of fig. 7. Determine the next state for each unused state and how that, if the circuit finds itself in an invalid state

it does not return to a valid state
(b) modify the circuit as recommended in the text and show that
(1) the circuit produces the same sequence of states as listed in fig - 7.23(b) and (2) the circuit reaches a valid state from any one of the unused states.

10t

Soln:

(a) unused states (in decimal): 2 9 5 6 9 10
11 13

Next state (in decimal): 9 10 2 11 9 13 5 6

(b) $2 \rightarrow 9 \rightarrow 4 \rightarrow 8 \rightarrow 10 \rightarrow 13 \rightarrow b \rightarrow 11 \rightarrow 5 \rightarrow 0$

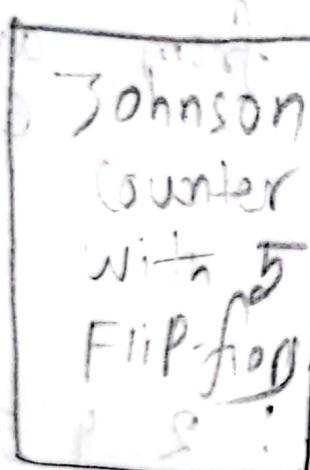
8 is valid state.

0 is valid state.

* Ex-7.28: Construct a Johnson counter with ten timing signals.

(102)

Sol:



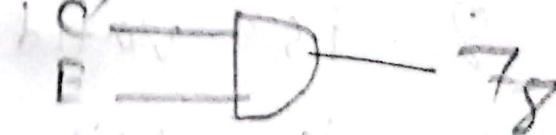
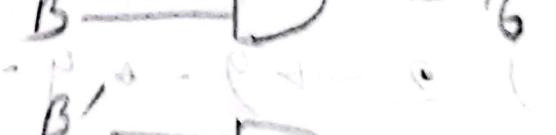
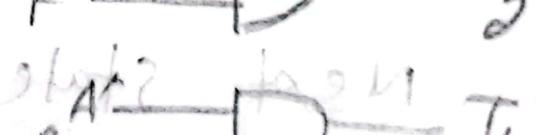
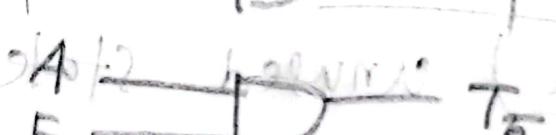
A

B

C

D

E



* Ex-7.29: (a) The memory unit of fig 7.29 has a capacity of 8192 words of 32 bits per word. How many flip-flops are needed for the memory address register and memory buffer register?

(b) How many words will the memory unit contain if the address register has 15 bits?

501ⁿ:

103

(a) Since the number of memory locations is 8192, we need 13 bits to represent these addresses ($2^{13} = 8192$). Therefore the memory address register requires 13 flip-flops.

(b) In this case, the memory address register has 15 bits, so the number of words the memory unit can contain is $2^{15} = 32,768$ words.

* Ex-7.32: It is required to construct a memory with 256 words, 16 bits per word, organized as in fig-7.33. Cores are available in a matrix of 16 rows and 16 columns.

- (a) How many matrices are needed?
→ 16 matrices needed.
- (b) How many flip-flops are in the address and buffer registers?
→ 8, 16.
- (c) How many cores receive current during a read cycle?
→ 16
- (d) How many cores receive at least half-current during a write-cycle?
→ $16 + 255K$ where K is the number of 1's in the word to be stored.