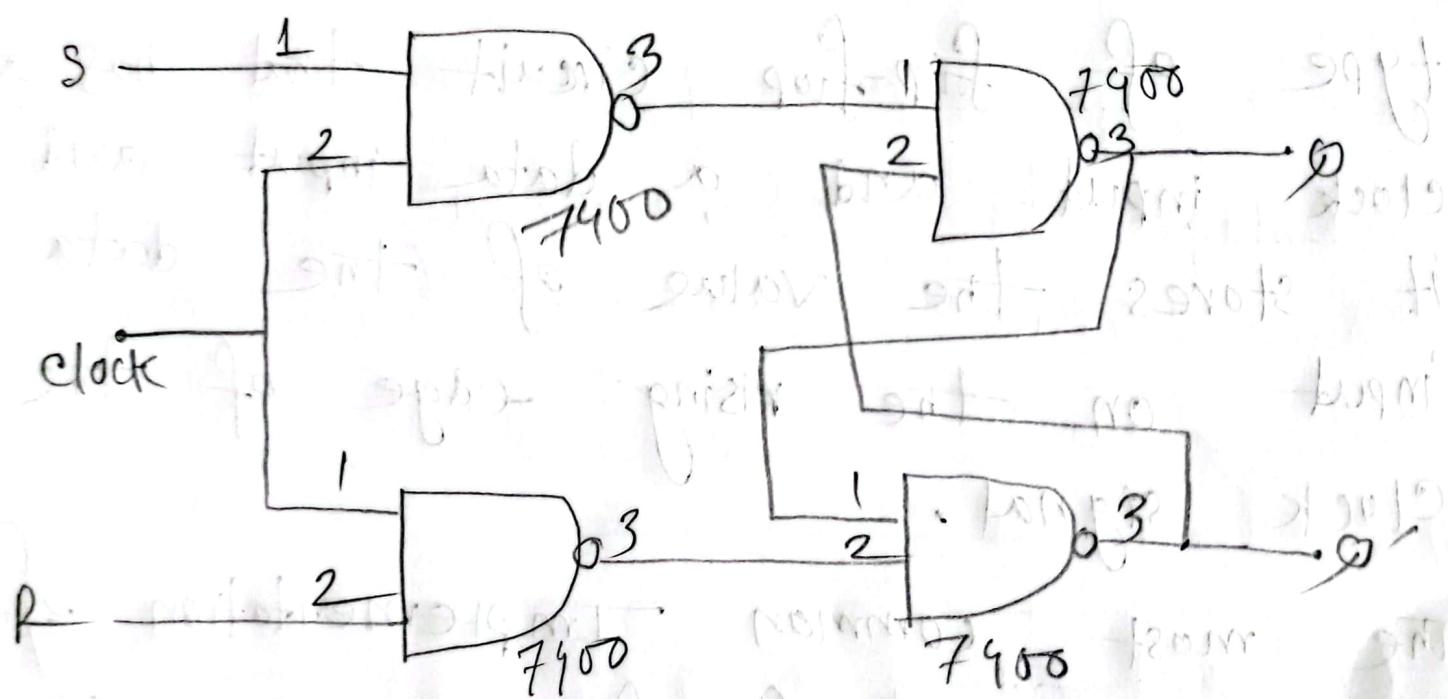


## Chapter-06: Sequential circuit.

\* Ex-6.1: Show the logic diagram of a clocked RS flip-flop with four NAND gates.

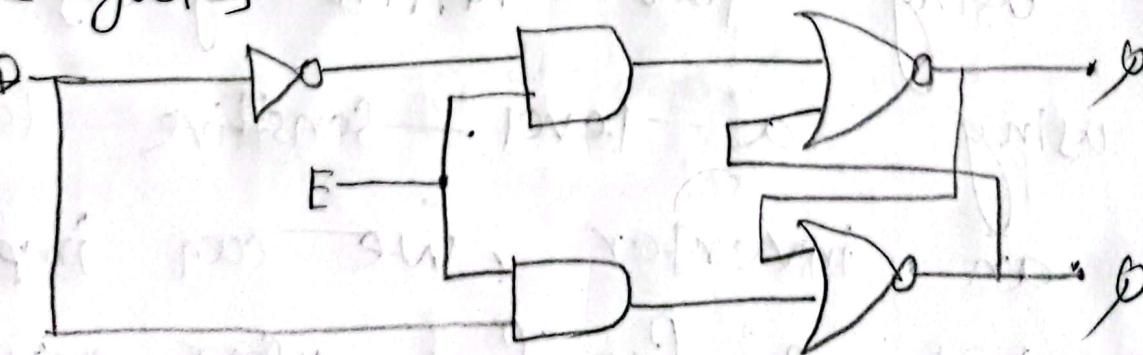
# Sol<sup>n</sup>:

(43)



\* Ex-6.2: Show the logic diagram of a clocked D flip-flop with AND and NOR gates.

# Sol<sup>n</sup>:



\* Ex-6.3: Show that the clocked D flip-flop of fig-6.5(a) can be reduced by one gate.

(56)

# Sol<sup>n</sup>: A clocked 'D' flip-flop is a type of flip-flop circuit that has a clock input and a data input and it stores the value of the data input on the rising edge of the clock signal.

The most common implementation of a clocked D flip-flop is the positive edge triggered D flip-flop, which is built using two NAND gates.

By using a level-sensitive latch and an inverter, we can implement a clocked D flip-flop using only three gates.

\* E.X-6.4: Consider a JK' flip, i.e. a JK flip-flop with an inverter between input  $J'$  and internal input  $K$ .

(a) obtain the flip-flop characteristics

table

Soln:

47

$\varphi$	$J$	$K'$	$\varphi(t+1) = \bar{J}\varphi + K'\varphi$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	0	1

(b) obtain the characteristics equation:

# Soln. we can draw derive the characteristics equation from above table

\* Ex-6.5: A set-dominant flip-flop has a set and reset input. It differs from a conventional RS flip-flop in that an attempt to simultaneously set and reset results in setting the flip-flop.

(a) Obtain the characteristic table and equation for the set-dominant flip-flop.

# soln:

54

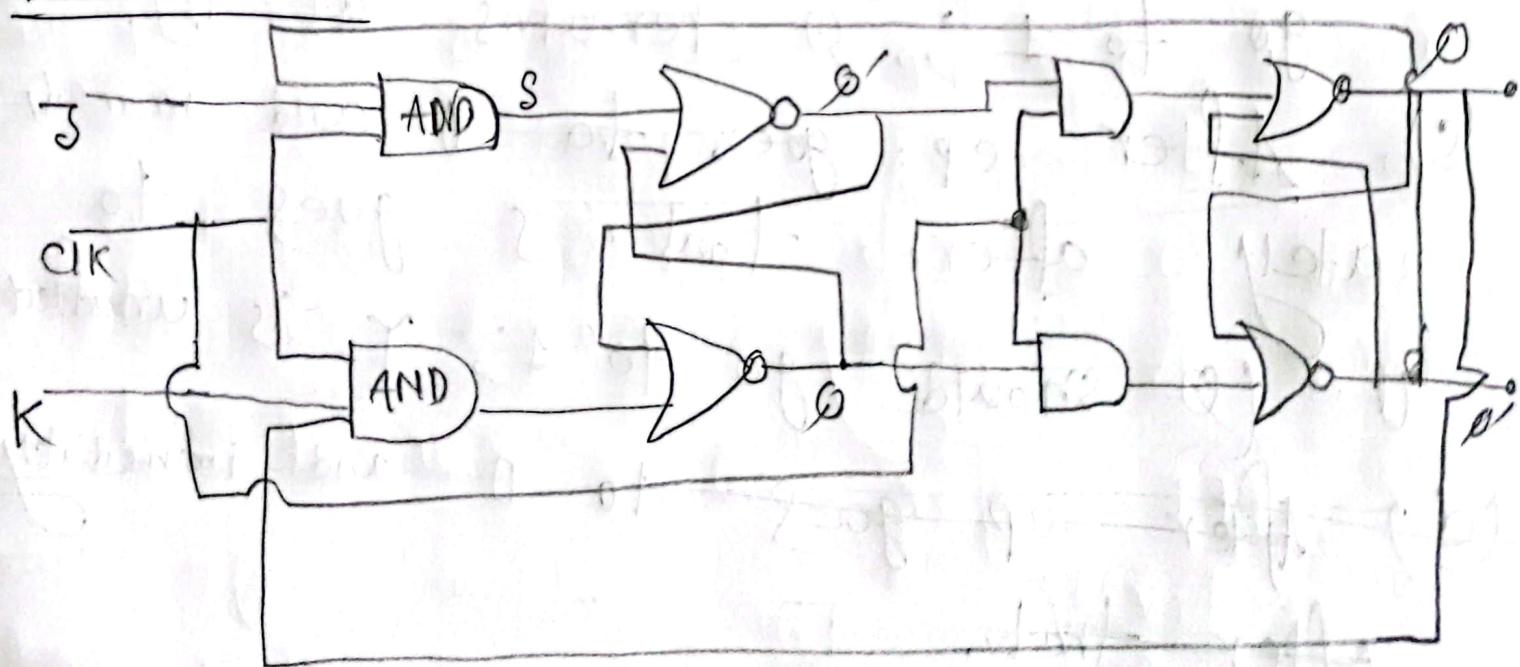
$Q$	SD	R	$Q(t+t) = S + R\bar{Q}$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

→ Now, we can derive the characteristic equation from above table.

\* Ex-6.6: Obtain a logic diagram for an asynchronous set dominate flip-flop of a master slave JK flip-flop with AND and NOR gates. Include a provision for setting and clearing the flip-flop asynchronously (without a clock).

(19)

# Soln:



\* Ex-6.7: This problem investigates the operation of the master-slave JK flip-flop through the binary values (0 or 1) in the output of the nine gates when the input to the circuit go through the following sequence:

- (a)  $cp = 0$ ,  $J = 0$ ,  $K = 0$ , and  $T = 1$
- (b) After  $cp$  goes to 1 ( $T$  should go to 1;  $Q$  remains at 0).
- (c) After  $cp$  goes to 0 and immediately after that  $J$  goes to 0 ( $Q$  should go to 1;  $T$  is unaffected)
- (d) After  $cp$  goes to 0 and immediately after that.

- (d) After CP goes to 1 again (Y should go to 0)
- (e) After CP goes back to 0 and immediately after that K goes to 0.
- (f) All succeeding pulses have no effect as long as J and K remain at 0. 51

~~Soln:~~

	1	2	3	4	5	6	7	8	9
--	---	---	---	---	---	---	---	---	---

(a)

1	1	0	1	1	0	0	1	1
---	---	---	---	---	---	---	---	---

(b)

0	1	0	1	0	0	1	0	1
---	---	---	---	---	---	---	---	---

(c)

1	1	0	1	1	1	1	0	0
---	---	---	---	---	---	---	---	---

(d)

1	0	0	0	1	1	1	0	0
---	---	---	---	---	---	---	---	---

(e)

0	1	0	0	1	1	0	0	1
---	---	---	---	---	---	---	---	---

$\{ \text{CP} = 0 \}$

$\{ \text{CP} = 1 \}$

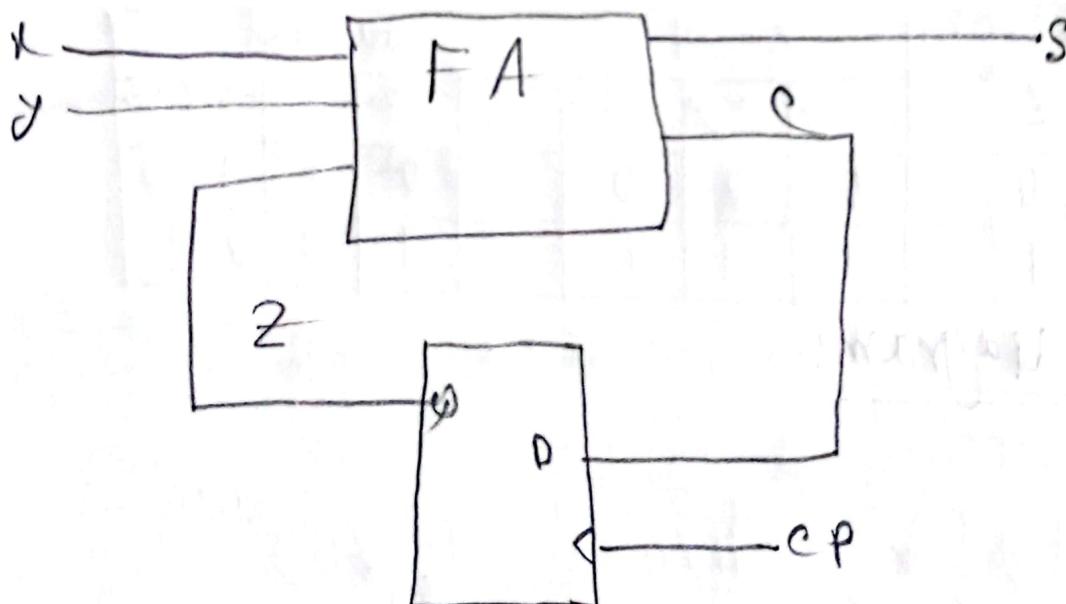
\* Ex-6.8. Connect an asynchronous clear terminal to the inputs of gates 2 and 6 of the flip-flop in Fig-6.12.

(a) Show that when the clear input is 0, the flip-flop is cleared and remains cleared, regardless of the values of CP and D inputs.

# Sol: When a asynchronous clear input is connected to gates 2 and 6 of a D flip-flop, it allows the flip-flop to be cleared regardless of the clock and data inputs. The clear input is typically denoted as 'CLR' or 'PRE' for "clear" or "preset" respectively. The positive logic convention for an asynchronous clear input is that a logic 0 on the input

\*Ex-6.9: The full-adder of fig. PG-10 receives two external inputs  $x$  and  $y$ ; the third input  $z$  comes from the output of a D flip-flop. The carry output is transferred to the flip-flop every clock pulse. The external S output gives the sum of  $y$  and  $z$ . Obtain the state table and state diagram of the sequential circuit.

(53)



# Soln:

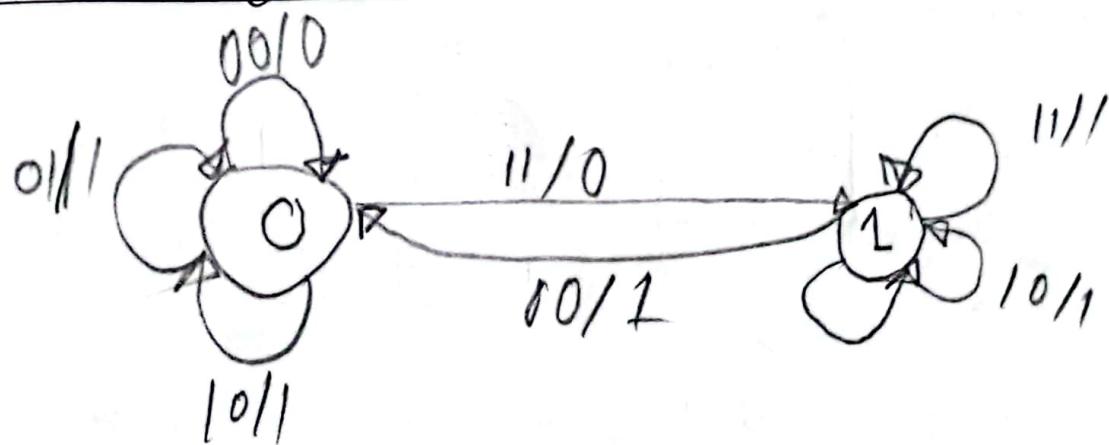
# Truth table:

x	y	z	c	s
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

# State table:

present z	next				output			
	xy	xy	xy	xy	xy	xy	xy	xy
0	0	0	0	1	0	1	1	0
1	0	1	1	1	1	0	0	1

# State diagram:



\* E-X-6-10: Derive the state table and state diagram of the sequential circuit of fig. P6-11. What is the function of the circuit?

(55)

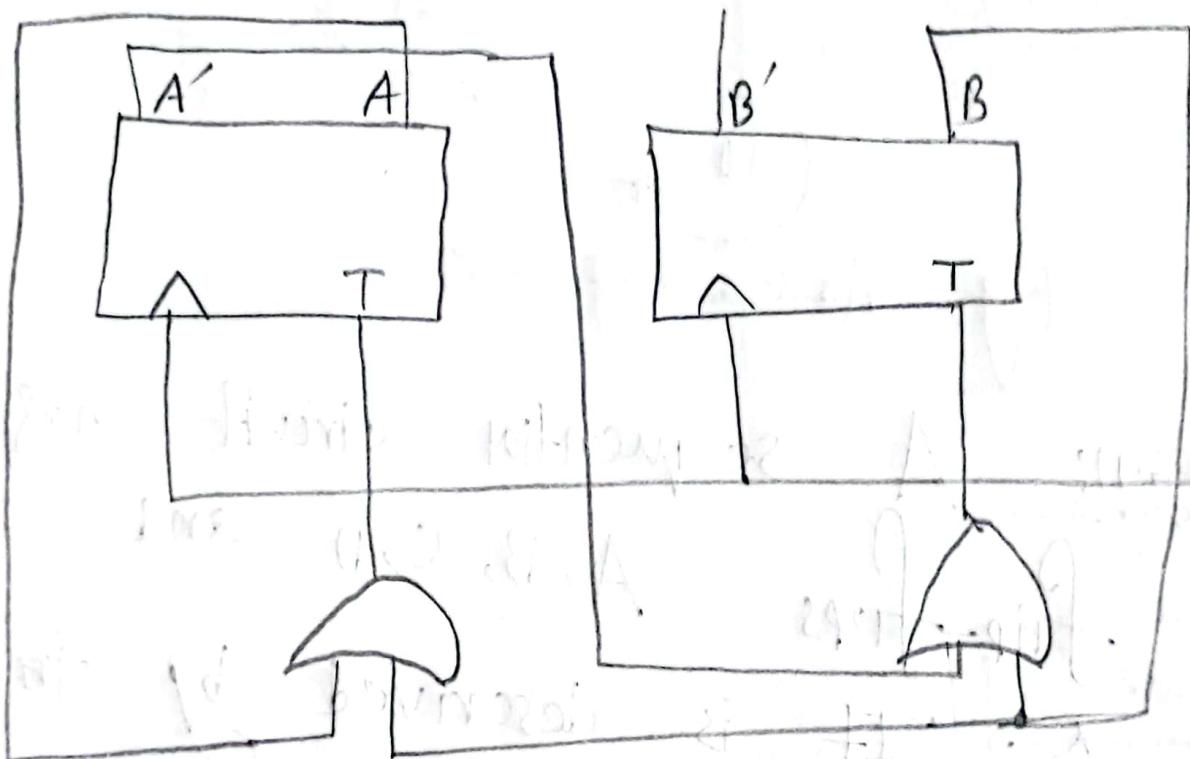


Fig-P6-11

# Sol<sup>n.</sup>:

$\Rightarrow$  State table:

present		Next state	
A	B	A	B
0	0	0	0-0
0	1	1	0-00
1	0	0	0-00
1	1	0	0-00

## # state diagram:

(56)

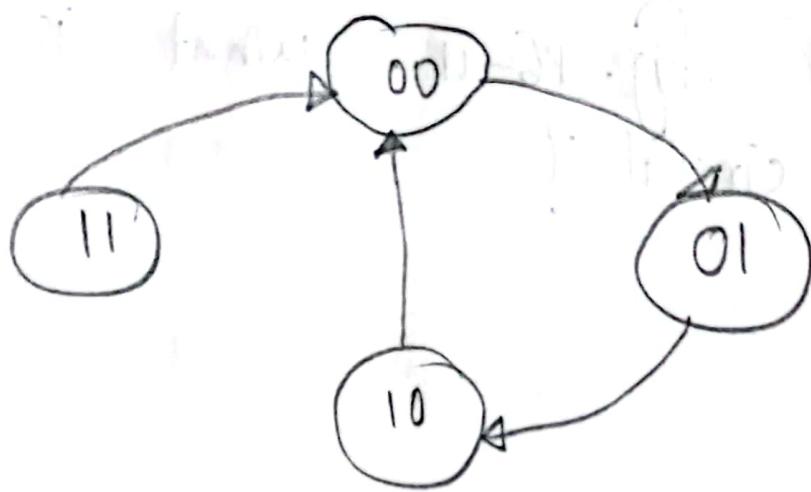


Fig. State diagram

\* Ex-6.11: A sequential circuit has four flip-flops A, B, C, D and an input x. It is described by the following state equations:

$$A(t+1) = (C_D + C'_D)x + (C_D + C'_D)x'$$

$$B(t+1) = A$$

$$C(t+1) = B$$

$$D(t+1) = C.$$

(a) obtain the sequence of states when  
 $\lambda = 1$ , starting from state  $ABCD = 0001$

# soln:

$$A(t+1) = CD + C'D + 0$$

$$B(t+1) = C \oplus D$$

$$C(t+1) = A$$

$$D(t+1) = B$$

$$D(t+1) = C$$

0 0 0 1	0 0 0 1
↓	↑
1 0 0 0	0 0 1 1
↓	↑
0 1 0 0	0 1 1 1
↓	↑
0 0 1 0	1 1 1 1
↓	↑
1 0 0 1	1 1 1 0
↓	↑
1 1 0 0	1 1 0 1
↓	↑
0 1 1 0	1 0 1 0
↓	↑
1 0 1 1	0 1 0 1

C	D	X
0	0	0
0	1	1
1	0	1
1	1	0

(b) obtain the sequence of states when  
 $\lambda = 0$ , starting from state  $ABCD$   
 $= 0000$ .

#Soln:

$$A(t+1) = C_0 + C_0' D = A \oplus D$$

$$B(t+1) = A, \quad C(t+1) = B$$

$$D(t+1) = C$$

C	D	Y
0	0	1
0	1	0
1	0	0
1	1	1

0000 → 1000 → 1100 → 1110 → 0111

0100 ← 1001 ← 1100 ← 0110 ← 1101 ← 1011

1010 → 0101 → 0010 → 0001 → 0000

~~Ex - 6.12:~~ A sequential circuit has two flip-flops (A and B), two inputs ( $x_1$  and  $x_2$ ) and an output (Z). The flip-flop input functions and the circuit

output function are as follows:

$$J_A = xB + y'B'$$

$$K_A = xy'B' ; \bar{J}_D = xA'$$

$$KB = xy + A$$

$Z = xyA + x'y'B$  obtain the logic diagram, state table, state diagram and state equations

# Sol<sup>n</sup>!!

present	$x = 0, y = 0$ A B	$x = 0, y = 1$ A B	$x = 1, y = 0$ A B	$x = 1, y = 1$ A B	$x = 0, y = 0$ A B	$x = 0, y = 1$ A B	$x = 1, y = 0$ A B	$x = 1, y = 1$ A B
00	10							
01	00							
10	10							
11	00							

⇒ now, we can derive each requirement from the above table.

\* Ex-6.13: Reduce the number of states in the following state table and tabulate the reduced state table.

(60)

present state	next state		output	
	$\lambda=0$	$\lambda=1$	$\lambda=0$	$\lambda=1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	f	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1

#Soln:

stack	a	f	f	b	d	g	g	d	a	b	a
Input	0	0	1	0	0	0	1	1	1	1	1
Output	0	1	1	0	1	0	1	0	0	1	0

Ex-6.14. Starting from state a of the state table in problem 6.14. find the output sequence generated with an input sequence 01110010011.

# Soln:

(61)

state	a	f	b	c	c	d	g	h	g	g	h	a
input	0	1	1	1	0	0	1	0	0	1	1	
output	0	1	0	0	0	1	1	0	1	0	1	

\*Ex-6.15: Repeat problem 6.15 using the reduced table of problem 6.14. Show that the same output sequence is obtained.

# Soln:

Stack:	a	f	b	a	b	d	g	d	g	g	d	a
Input:	0	1	1	1	0	0	1	0	0	1	1	
Output:	0	1	0	0	0	1	1	1	0	1	0	

\*Ex-6.17: obtain the excitation table of the JK' flip-flop described in problem 6.4.

# Soln:

$J$	$K'$	$\rho(t+1)$	$\rho(t)$	$\rho(t-1)$	$J$	$K'$
0	0	0	0	0	0	$\times$
0	1	$\rho(t)$	0	1	1	$\times$
1	0	$\rho'(t)$	1	0	$\times$	0
1	1	1	1	1	$\times$	1

\* Ex-6.18: obtain the excitation table  
of the set-dominated flip-flop  
described in problem 6.5.

~~#~~ 501^n:

SD	R	$\phi(t+1)$	$\phi(t)$	$\phi(t+1)$	SD	R
0	0	$\phi(t)$	0	0	0	x
0	1	0	1	0	1	x
1	0	1	1	1	0	1
1	1	1	1	1	x	0

\* Ex-6.19: A sequential circuit has one input and one output. The state diagram is shown in fig. Pf-20. Design the sequential circuit with.

(a) T flip-flops,

# Soln:

$$TA = A + B'x; TB = A + BC'x + BCx' + B'C'x'$$

$$TC = Ax = rx + A'B'C'n'$$

(b) RS flip-flops,

# Soln:

$$SA = A'B'x; RA = \bar{A}; SB = A + C'x'$$

$$RB = BC'x + Cx'; SC = A'B'x + Ax$$

$$RC = A'x.$$

(c) JK flip-flops:

# Soln:

$$JA = B'x, KA = 1; JB = A + C'x'$$

$$KB = Cx + Cx'; JC = A'Bx + Ax$$

$$KC = 1; x = A'x.$$

\* Ex-6.21: Repeat Example 6.1 with binary assignment 3 of Table 6.5. Use JK flip-flops.

# Soln:  $J_A = K_A = 1; J_B = A_n'; K_B = 1$   
 $J_C = B_n + A_n, K_C = B_n'$

\* Ex-6.22: Design a BCD counter with JK flip-flops

# Soln:

A	B	C	input	A	B	C	$J_A$	$K_A$	$J_B$	$K_B$	$J_C$	$K_C$	Y
0	0	0	0	0	1	1	0	X	1	X	1	X	0
0	0	0	1	1	0	0	1	X	0	X	0	X	1
0	0	1	0	0	0	1	0	X	0	X	X	0	0
0	0	1	1	1	0	0	1	X	0	X	X	1	1
0	1	0	0	0	1	0	0	X	X	0	0	X	0
0	1	0	1	0	0	0	0	X	X	1	0	X	1
0	1	1	0	0	0	1	0	X	X	1	X	0	0
0	1	1	1	0	1	0	0	X	X	0	X	1	1
1	0	0	0	0	1	0	X	1	1	X	0	X	0
1	0	0	1	0	1	1	X	1	1	X	1	X	0

## # Logic diagram:

(63)

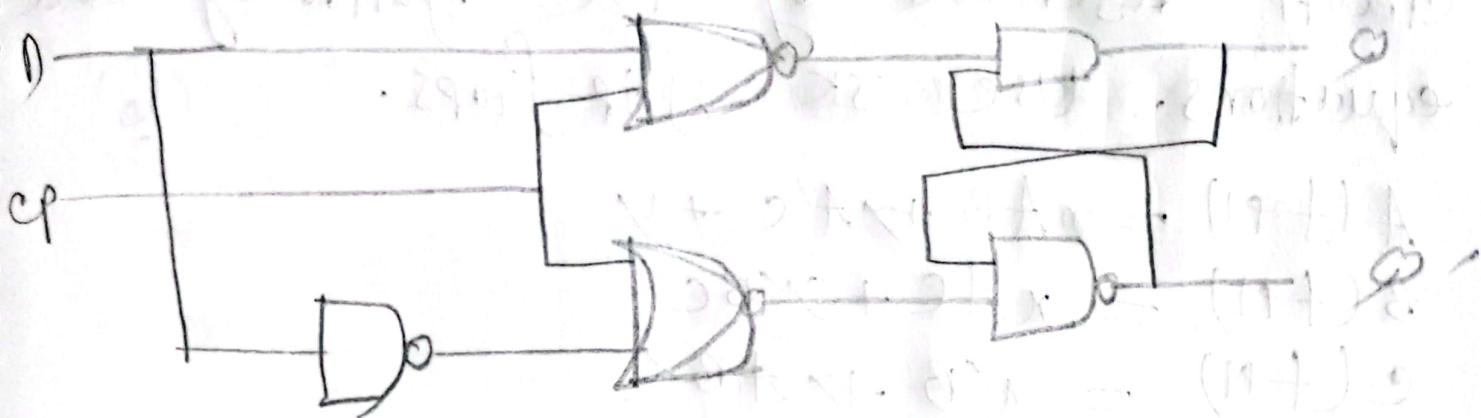


Fig. Logic diagram with NANDgates

\*Ex-6.23: Design a counter that counts the decimal digits according to the 2, 4, 2, 1 code (Table 9.2) use T flip-flops.

## # Soln:

$$\begin{bmatrix} 2 & 4 & 2 & 1 \\ A & B & C & D \end{bmatrix} ; TA = BCD + A'B$$

$$TB = CD + A'B$$

$$TC = D + A'B$$

$$TD = 1$$

\* E-X-6.25! Design the sequential circuit described by the following state equations. Use JK flip-flops.

(b)

$$A(t+1) = \bar{x}AB + xA'C + xy$$

$$B(t+1) = xAC + y'BC'$$

$$C(t+1) = x'B + x'AB$$

# Sol'n:

$$\begin{aligned} A(t+1) &= \bar{x}AB + xA'C + xy(A+PA') \\ &= A(Bx + xy) + A'(C\bar{x} + xy) \\ &= Ak' + \bar{A}'j \end{aligned}$$

$$\begin{aligned} K(A) &= Bx + xy, \quad JA = CY + xz \\ K_A &= (Bx + xy)' \\ &= (B' + x')(x' + y') \\ &= x' + B'y' \end{aligned}$$

$$\begin{aligned} B(t+1) &= xAC(B + B') + BY'C \\ &= (xAC + Y'C')B + B'xAC \\ &= KB + B'j. \end{aligned}$$

$$\begin{aligned}
 K_B &= (XAC + Y'C')' \\
 &= (XYAC + X'Y'A'C + XY'A'C' + X'Y'A'C' \\
 &\quad + XY'A'C' + X'Y'A'C + XY'A'C)' \\
 &= (XYAC + X'Y'A'C + XY'A'C')'
 \end{aligned}$$

(67)

AC		00	01	11	10
Y		00	01	11	10
	00	1	0	0	1
	01	0	0	0	0
	11	0	0	1	0
	10	1	0	1	1

$$K_B = X'C'Y'C + X'A'C$$

$$J_B = XAC$$

A B. X - 6.26: (a) Derive the state equations for the sequential circuit specified by table 6.6, section 6-5.

List the don't care terms.

#SOP:

(B)

Present			X	Next			T <sub>A</sub>	T <sub>B</sub>	T <sub>C</sub>	X
A	B	C	input	A	B	C				
0	0	0	0	0	1	1	0	1	1	0
0	0	0	1	1	0	0	1	0	0	1
0	0	1	0	0	0	1	0	0	0	0
0	0	1	1	1	0	0	1	0	1	1
0	1	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	1	0	1
0	1	1	0	0	0	1	0	1	0	0
0	1	1	1	0	1	0	0	0	1	1
1	0	0	0	0	1	0	1	1	0	0
1	0	0	1	0	1	1	1	1	1	0

AB	00	01	11	10
00	00	1	1	
01				
11	x	x	x	x
10	x	x	x	x

AB	00	01	11	10
00	x			
01	x	x	x	x
11	x	x	x	x
10	x	x	x	x

$$T_A = A + B'x$$

$$T_B = A + B'C'x + BCx + B'Cx$$

	00	01	11	10
00	1			
01				
11	x	x	x	x
10	x	x	x	x

(b) Derive the flip-flop input functions from the state equation (and don't care terms) using the method outlined in Example - 6.5. Use JK flip-flops.

#Soln:

(b)

SA	RA	CB	RB	SC	RC
0	X	1	0	1	0
1	0	0	X	0	X
0	X	0	X	X	0
1	0	0	X	0	1
0	X	X	0	0	X
0	X	0	1	0	X
0	X	X	0	0	X
0	1	1	0	0	X
0	1	1	0	1	0

AB	00	01	11	10
00	0	1	1	
01				
11	X	X	X	X
10		X	X	X

SA = A'B'X

AB	00	01	11	10
00	X			X
01	X	X	X	X
11	X	X	X	X
10	1	1	X	X

RA = A

\* Ex-6.27: Differentiate between sequential circuit and combinational circuit.

Sol: The combinational circuit is time-independent. The output it generates does not depend on any of its previous inputs. On the other hand, sequential circuits are the ones that depend on clock cycles. They depend entirely on the past as well as the present inputs for generating outputs.

Ex-6.28: What is the problem fund in RS flip-flop? Explain how it is solved in JK flip-flop.

# Soln: — The RS (Reset+Set) flip-flop is a type of digital circuit that has two inputs, namely the set and reset inputs and two outputs, namely the  $Q$  and  $Q'$  outputs.

When the  $S$  input is high and the  $R$  input is low, the  $Q$  output is set to high and when the  $S$  input is low and the  $R$  input is high, the  $Q$  output is reset to low.

However, when both  $S$  and  $R$  inputs is high, or both are low, the output state becomes unpredictable resulting in a condition known as "forbidden state" or "race condition". This problem can lead to errors.

in digital circuits and it must be avoided.

(x2)

\* Ex-6.29: what is the necessity of master-slave flip-flop? Explain working of D master-slave flip-flop. Realize with all NOR gates.

Soln: The master-slave flip-flop is a type of flip-flop that is commonly used in digital circuits. It is designed to avoid timing problems that can occur in simple flip-flops, due to changes in input signals during the output transition. The master-slave flip-flop is composed of two basic flip-flops, a master flip-flop and a slave flip-flop.

which are connected in series to form a single flip-flop.

(13)

\* Ex-6.30: Convert 'T' flip-flop to 'D' flip-flop.

# Sol:

Step-01: write the truth table of the required flip-flop is D flip-flop.

Hence, we need to write the truth table of D flip-flop which is,

D	$Q_N$	$Q_{N+1}$
0	0	0
0	1	0
1	0	1
1	1	1

Step-02: write the excitation table of the given flip-flop In this case the given flip-flop is T

flip-flop. Therefore we need to write the excitation table of T flip-flop which is:

$D_N$	$D_{N+1}$	T
0	0	0
0	1	1
1	0	1
1	1	0

# Step-03: write the conversion table!

D	$D_N$	$D_{N+1}$	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

# Step-04: Find the Boolean expression for the inputs of the given flip flop.

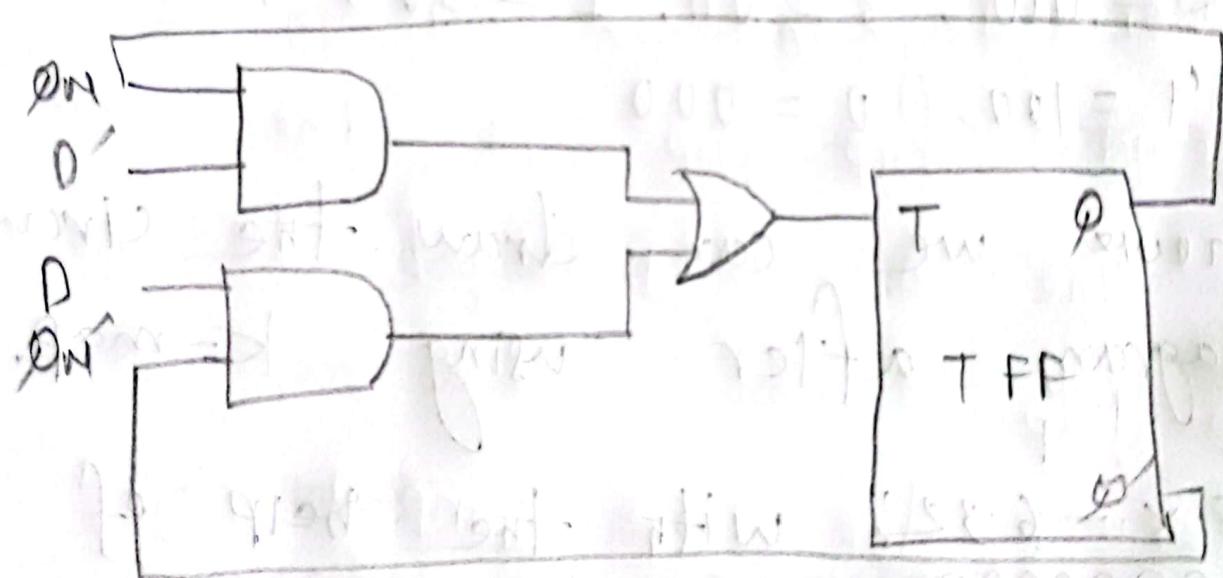
$\bar{Q}_N$	$Q_N$
0	1
1	0

(2)

Expression for T would be,

$$T = D' \bar{Q}_N + D Q_N'$$

# Step-05: Draw the circuit for implementing D flip-flop from T flip-flop



\* Ex-6.31: with help of JK flip-flop design a counter which counts following binary sequence 2, 3, 1, 7, 4, 0 and repeat.

# Sol<sup>n</sup>: Since we have 6 different numbers in the sequence, we need at least 3 flip-flops ( $2^3 = 8$  which is greater than 6)

⇒ now, we can use a 3-bit binary sequence to represent the numbers in the following way:

$$2 = 010, 3 = 011, 1 = 001, 7 = 111$$

$$4 = 100, 0 = 000$$

(16)

⇒ now we can draw the circuit diagram after using k-map.

\* Ex - 6.32: with the help of RS flip-flop design a counter which counts following binary sequence 1, 3, 5, 7, 9 and repeat.

# Soln: Since, we have 5 different number of flip-flops and implement a circuit required to count, we need at least 3 flip-flops ( $2^3 = 8$  which is greater than 5) 17

⇒ 3-bit binary sequence to represent the numbers in the following way:

① 1 = 001, 3 = 011, 5 = 101, 7 = 111  
9 = 001, this is the same as 1  
so the sequence repeat

⇒ we can use two RS flip-flops as follows:

□ Connect the S output of the first flip-flop to the R input of the second flip-flop.

□ Connect the Q output of the

second flip-flop to the R input of the first flip-flop.

□ Connect the S input of the first flip-flop to the complement of the Q output of the second flip-flop.

□ Connect the S input of the second flip-flop to the complement of the Q output of the first flip-flop.

□ Connect the clock input of each flip-flop to a common clock signal.

□ Connect the Q output of the third flip-flop to a 3-bit binary-to-decimal converter to display the count.

(A8)