EHSAN QASEMI

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RESEARCH INTEREST

Dynamic **Software Engineer** with strong **mathematic background,** skilled at developing complex solutions with high performance and low cost, with strong creative thinking skills, high energy, and integrity. Experienced in working in teams with different cultures and skills, seeking **summer internship for summer 2017**.

EDUCATION

MSC. IN COMPUTER ENGINEERING (GPA 3.38/4) : University of Wisconsin at Madison, **(Graduate: May 2017)**

- **CERTIFICATE IN ENTREPRENEURSHIP:** University of Wisconsin Madison, Madison, WI, USA

BSC. IN ELECTRONICS ENGR. /DIGITAL SYS. (GPA 16.12/20) : University of Tehran, **(Graduate: February 2015)**

- **Ranked 1'st** in Iran's 1st National Digital System Design Contest HW/SW co-design league. 2013
- **Ranked 1'st** in **2D Soccer Simulation** Contest 2008
- **Ranked** as **57** among 500,000 students in National Universities Entrance Exam Spring 2010
- Qualified for Iran's **National Physics Olympiad** semi-final round (top 100) 2009

KEY COMPETENCE

Matlab	C/C++	HTML
Python	Java	CSS
R	Scala	JavaScript
Octave	Lua	OpenMP
Julia	OpenCL	MPI
Cuda	Assembly (X86, Arm, Mips)	SQL

PROFESSIONAL EXPERIENCE

LEAD HARDWARE DESIGNER/PROGRAMMER/VERIFICATION ENGINEER AUGUST 2014-JULY 2015
IWIN CO. Tehran, IRI

- Design, implement and test an FPGA-based **Hardware Security Module (HSM)** to provide a secure platform for bank applications such as money transactions, on Zync7100 SoC platform.
- Implement the low-level OS kernel functions to communicate with the AXI-STREAM and AXI-FULL interfaces to gain maximum performance in C
- Manage the HW team to Design the FPGA-based hardware to implement wide range of cryptography algorithms in Chisel HDL (RSA, AES, 3DES, ECC, etc.)
- Design the FPGA-based interfaces and HW wrappers to communicate to Linux-based custom OS in Chisel HDL.
- Design and Implement the HW verification procedure to perform the **NIST** test on HW in an automated environment in Java, Scala, and Chisel HDL.

PROGRAMMER/EMBEDDED ENGINEER MAY 2016-AUGUST 2016
PARDIS CO. Tehran, IRI

- Generate the Costume Linux based OS for Atmel sam9 and Qualcomm Atheros micro-controllers
- Patch and Cross Compile the **python 2.7.3** source code for Atmel sam9
- Write a python based **web server** to manage a cryptographic network node to **secure the communication**.
- write a low-level C application as the backbone of the **server** to get maximum **Enc/Dec** performance.

PROGRAMMER/ANALYST JUNE 2013-JANUARY 2014
S.T.FARABI CO. SANANDAJ, IRI

- Design and implement a low-cost **Genetic algorithm (GA)** based controller hardware to operate a mechanical arm on FPGA platform.
- Design set of procedures to automate the test and verification steps of the product.

PUBLICATIONS

- M. Biglari, **E. Qasemi**, B. PourMohseni, "Maestro: A High-Performance AES Encryption/Decryption System", The 17th CSI International Symposium on Computer Architecture & Digital Systems (CADS 2013), October 30-31, 2013, School of Computer Science, IPM, Tehran, Iran.
- **Ehsan Qasemi**, Mohammad H. Shadmehr, Bardia Azizian, Amir Samadi, Sajjad Mozaffari,Amir Shirian and Bijan Alizadeh, "Highly Scalable, Shared Memory , Monte-Carlo Tree Search based Blokus Duo Solver on FPGA ", International Conference on Field-Programmable Technology (FPT), 2014.
- Ghasem Pasandi, Sied Mehdi Fakhraie, and **Ehsan Qasemi**, "A New Tri-State Based Static Random Access Memory (SRAM) Cell with Improved Write Ability and Read Stability," accepted for publication in CSI Journal on Computer Science and Engineering, April 2014.
- Ghasem Pasandi, **Ehsan Qasemi**, and Sied Mehdi Fakhraie, "A New Low Leakage TGate Based 8T SRAM Cell with Improved Write-Ability in 90nm CMOS Technology," in 22nd Iranian Conference on Electrical Engineering (ICEE), Tehran, Iran. May 2014.

RESEARCH EXPERIENCE

PERSEPOLIS RESEARCH GROUP — University of Wisconsin-Madison
Prof. Amir Assadi — Current

- Work as research assistant on Study on novel **clustering and associated data visualization** methods to achieve personalized therapies for Autistic children
- Manage and process **massive heterogeneous datasets and bigdata** that includes video, genome sequence etc.

DESIGN, VERIF. & DEBUGG OF EMBEDDED SYSTEMS (DVDES) LAB — University of Tehran
Prof. Bijan Alizadeh — 2014-15

- HW/SW co-design of **Highly parallel** Blokus-Duo Solver based on **Monte Carlo Tree Search (MCTS)** Engine on Terasic DE2-115 FPGA board.
- Research on a **Monte-Carlo Tree Search(MCTS)** Based Scheduling algoritm.

SILLICON INTELIGENCE AND VLSI SIGNAL PROCESSING(SI) LAB — University of Tehran
Prof. Sayed Mehdi Fakhrae — Summer & Fall 2013

- Design an electronic design automation procedure to obtain custom designs in layout using SKILL scripting language.
- Work as research assistant on low power SRAM memory cells to operate in subthreshold voltages.
- Design & Implementation of an Automatic SRAM Memory Generator CAD tool with capability of designing Low-power SRAMs with configurable cells working in both Sub-threshold and super-threshold regions in 180nm technology.

COMPUTER-AIDED DESIGN(CAD) AND TLM LABS — University of Tehran
Prof. Zain Navabi — Summer & Fall 2012

- Research on **formal verification** methods using temporal logic
- Hardware implementation of a synthesizable Utopia ATM communication module in System Verilog on Terasic DE2 FPGA board.
- Implementing an Object-Oriented based random constrained test bench as Verification method.
- HW/SW co-design of **AES encryption/decryption** algorithm on FPGA platform (Terasic DE2-115 FPGA board) (FPGASoC Design Competition).

VOLUNTARY AND LEADERSHIP EXPERIENCE

- **President** at **Persian Student's Society of UW Madison (PSS)** **2015-2017**
- **Organize and Lead** group of undergrad students to participate in:
  ICFPT Design Competition **Summer and Fall 2014-15**
  FPGASoC Design competition **Winter 2014**
- **Member of Graduation Ceremony Board** for Electrical Engineering Students **Fall 2014**
  Assisted in organization and board member of graduation ceremony
- Assisted in **Cultural Music Events & Concerts in UoT Campus** **Fall 2013**
  hosted by ISociety at University of Tehran
- World-Wide Culture day at Madison's East High School **Fall 2016**

NOTABLE ACADEMIC PROJECTS

Graduate:

- Study on **Monte-Carlo Tree Search** Algorithms for Parallel Platforms in CUDA, OpenMP, and MPI CS759
- Study on **Security analysis** of Split Manufacturing method in Chip manufacturing CS756
- **XSS, XSFR, SQLI,** and **Phishing** attacks and their countermeasures in websites (HTML, JS) CS642
- Low-level **OS** exploits using Aleph One's code (**Stack Smashing, Double free, Format String**) CS642
- **Neural Network** based Sonar Radar in Python with Keras CS760
- **Hand writing recognition** with Neural networks in Python with Keras CS760
- Study on **Data predictions** (TAGE and V-TAGE) in Modern Processor Architecture CS752

Undergraduate:

- **Skin Detection** Algorithm for NVIDIA GPU platforms in CUDA ECE403
- Study on parallel sorting methods (RADIX, Bubble, Merge, and Quick) in MPI ECE403
- Harmonic Synthesizer with Gender Identification Based on AC Pitch Estimation Method. ECE991
- Real-time, **RLS based**, **Adaptive noise cancellation** FIR filter on DSK6700, DSP boards. ECE991
- Automated **adaptive voice recorder** tool based on **PESQ** speech quality evaluation method ECE403
- Client/Server **Cloud Storage** Application in Python ECE412