PROJECT PROPOSAL

Title: FPGA implementation with machine learning

Proposer: Prosper Su

Supervisor: Dr David Boland

Project Brief

The aim of the project is to explore possible outcomes of implementations between FPGA hardware and machine learning algorithms. While the existing developments for either machine learning algorithms or FPGA hardware implementation are mature independently, their integrations can lead to performance challenges. To address this, the various techniques such as debugging tools or new implementation methodology will be employed to generate and execute new tests. These new results then are compared against with the previous benchmarks to evaluate the new outcomes whether they are positive or negative. This exploration of software-hardware implementation which mainly based on recent optimised machine learning algorithms and FPGA hardware will provide better vision and potentials for further development within FPGA and machine learning aspects.

Milestone

Project Milestone

PROJECT TITLE	FPGA implementation with machine learning
PROPOSER	Prosper Su
SUPERVISOR	Dr David Boland
DATE	Friday, 15 March 2024

TASK ID	TASK TITLE	PCT OF TASK COMPLETE
1	Project Initiation	
1.1	Project Topic	100%
1.2	Project Proposal	100%
2	Project Planning & Design	
2.1	Background Research	0%
2.2	Basic implementation	0%
2.3	Technique Design	0%
2.4	Progress Report	0%
3	Project Execution & Performance	
3.1	1st Design implementation	0%
3.2	Design Updates	0%
3.3	*2nd Design implementation	0%
4	Project Anaylsis	
	Result anaylsis	0%
5	Project Report	
5.1	Draft Thesis	0%
5.2	Final Thesis	0%
5.3	Thesis Presentation	0%

Approvals

_____15/03/2024_____ _____Dr David Boland_____ _____

Date *Supervisor name* *Supervisor Signature*