

[Link to my github](#)

# Lab 03-vivado

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## 1. Table SW+LED

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SW	SW_PORT	LED	LED_PORT
SW0	J15	LED0	H17
SW1	L16	LED1	K15
SW2	M13	LED2	J13
SW3	R15	LED3	N14
SW4	R17	LED4	R18
SW5	T18	LED5	V17
SW6	U18	LED6	U17
SW7	R13	LED7	U16
SW8	T8	LED8	V16
SW9	U8	LED9	T15
SW10	R16	LED10	U14
SW11	T13	LED11	T16
SW12	H6	LED12	V15
SW13	U12	LED13	V14
SW14	U11	LED14	V12
SW15	V10	LED15	V11

## 2. Two-bit wide 4-to-1 multiplexer

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VHDL architecture

```

architecture Behavioral of mux_2bit_4to1 is
begin
    f_o <= a_i when (sel_i = "00" ) else
           b_i when (sel_i = "01" ) else
           c_i when (sel_i = "10" ) else
           d_i;

end architecture Behavioral;

```

## VHDL stimulus process

```

p_stimulus : process
begin

    s_a <= "00"; s_b <= "01"; s_c <= "10"; s_d <= "11";
    s_sel <= "00"; wait for 100 ns;

    s_a <= "00"; s_b <= "01"; s_c <= "10"; s_d <= "11";
    s_sel <= "10"; wait for 100 ns;

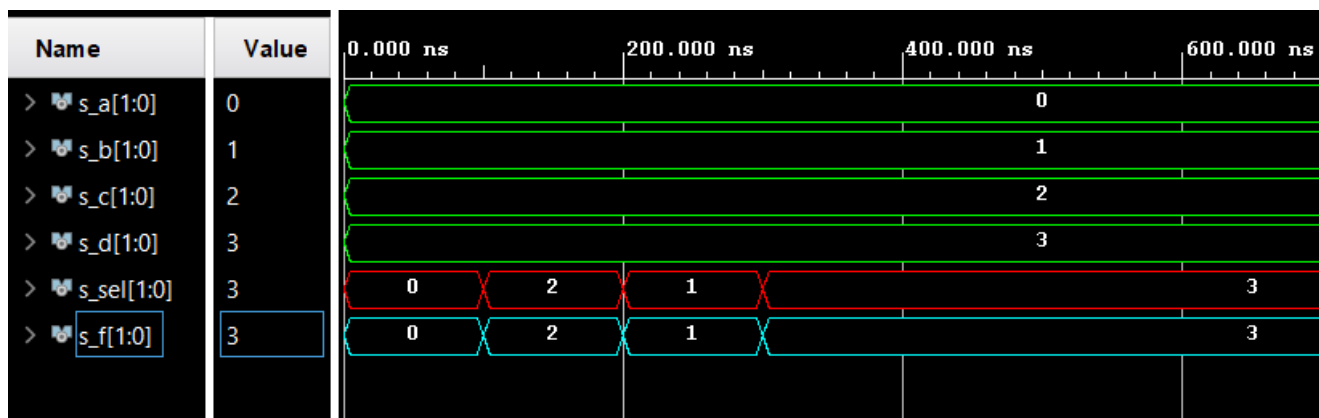
    s_a <= "00"; s_b <= "01"; s_c <= "10"; s_d <= "11";
    s_sel <= "01"; wait for 100 ns;

    s_a <= "00"; s_b <= "01"; s_c <= "10"; s_d <= "11";
    s_sel <= "11"; wait for 100 ns;

    wait;
end process p_stimulus;

```

## Screenshot of simulated waveforms

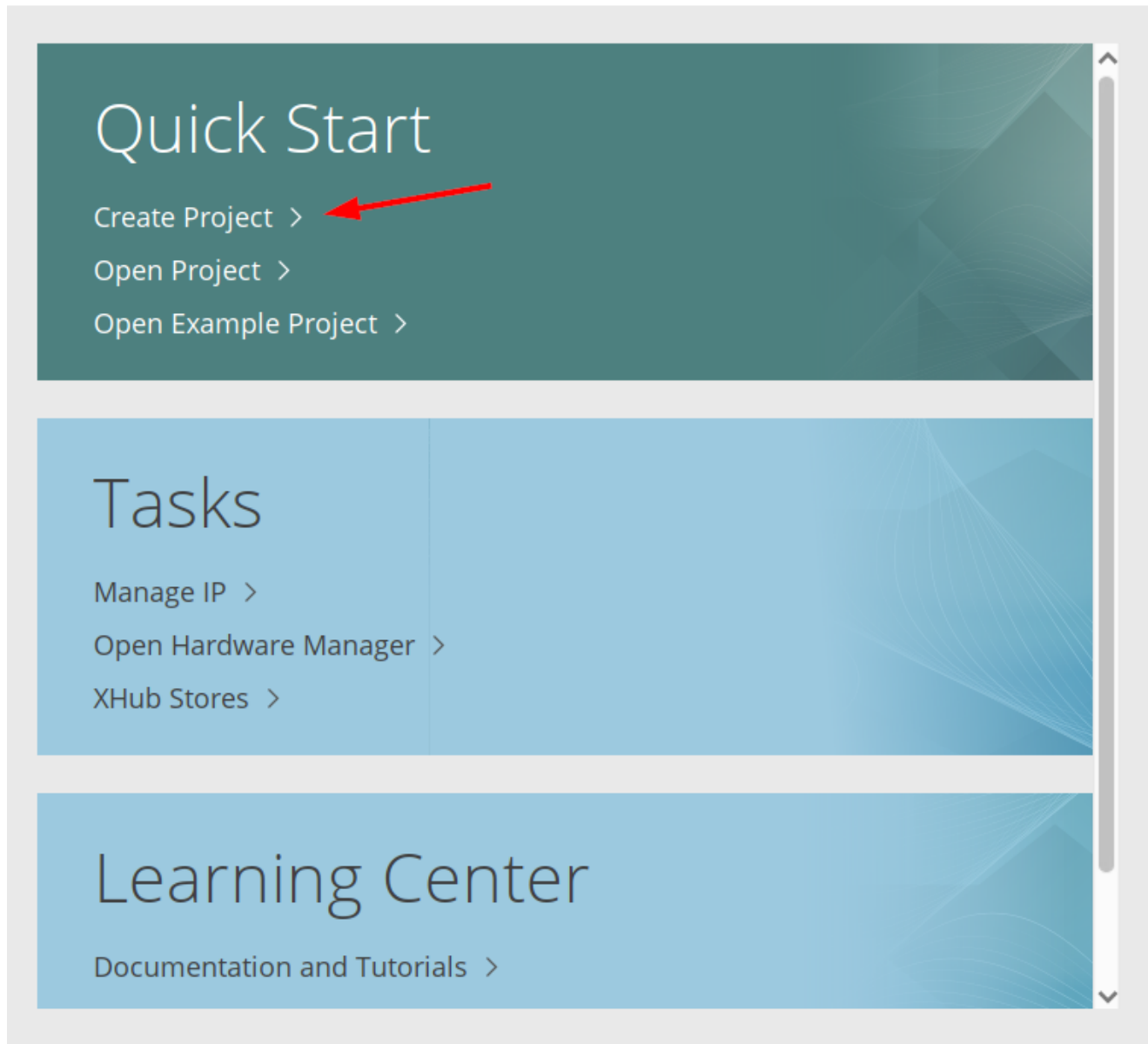


### 3. Vivado tutorial

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#### Create new projekt

HLX EDITIONS



#### Choose project name and directory

## Project Name

Enter a name for your project and specify a directory where the project data files will be stored.



Project name:

Project location:

☒ Create project subdirectory

Project will be created at: D:/path\_to\_project/project\_name



< Back

Next >

Finish

Cancel

## Select project type

### Project Type

Specify the type of project to create.



- ☒ **RTL Project**  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
- ☐ Do not specify sources at this time
- ☐ Project is an extensible Vitis platform
- ☐ **Post-synthesis Project**  
You will be able to add sources, view device resources, run design analysis, planning and implementation.
- ☐ Do not specify sources at this time
- ☐ **I/O Planning Project**  
Do not specify design sources. You will be able to view part/package resources.
- ☐ **Imported Project**  
Create a Vivado project from a Synplify, XST or ISE Project File.
- ☐ **Example Project**  
Create a new Vivado project from a predefined template.



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Next >

Finish

Cancel

## Add design/constraint sources

### Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.



The screenshot shows the 'Add Sources' dialog in Vivado. A 'Create Source File' sub-dialog is open, showing 'File type' set to VHDL, 'File name' as 'design', and 'File location' as '<Local to Project>'. Red arrows with numbers 1 through 5 indicate the following steps: 1. Click the 'Create File' button at the bottom right. 2. Click the 'File name' text box in the 'Create Source File' dialog. 3. Click the 'File type' dropdown in the 'Create Source File' dialog. 4. Click the help icon (?) at the bottom left of the main dialog. 5. Click the 'Next >' button at the bottom right of the main dialog. Below the sub-dialog, there are buttons for 'Add Files', 'Add Directories', and 'Create File'. Further down, there are checkboxes for 'Scan and add RTL include files into project', 'Copy sources into project', and 'Add sources from subdirectories' (which is checked). At the bottom, there are dropdowns for 'Target language' and 'Simulator language', both set to VHDL, and a final set of buttons: '< Back', 'Next >', 'Finish', and 'Cancel'.

## Choose a part

## Default Part

Choose a default Xilinx part or board for your project.



Parts | **Boards** 1

[Reset All Filters](#) Install/Update Boards

Vendor: All Name: All Board Rev: Latest

Search: Q- 2

Display Name	Preview	Vendor	File Version	Part	I/O Pin Count	Board Rev	Available IOBs	LUT Elements
<a href="#">Nexys A7-50T</a> <span>3</span>		digilentinc.com	1.0	xc7a50ticsg324-1L	324	D.0	210	32600
<a href="#">Artix-7 AC701 Evaluation Platform</a> <a href="#">Add Companion Card</a> <a href="#">Connections</a>		xilinx.com	1.4	xc7a200tfg676-2	676	1.1	400	134600
<a href="#">Spartan-7 SP701 Evaluation Platform</a>		xilinx.com	1.0	xc7s100fgga676-2	676	1.0	400	64000



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Next >

Finish

Cancel

## Finish creating



### New Project Summary

- i A new RTL project named 'project\_name' will be created.
- i 1 source file will be added.
- w No constraints files will be added. Use Add Sources to add them later.
- i The default part and product family for the new project:  
Default Part: xc7k70tfg676-1  
Product: Kintex-7  
Family: Kintex-7  
Package: fbg676  
Speed Grade: -1



To create the project, click Finish



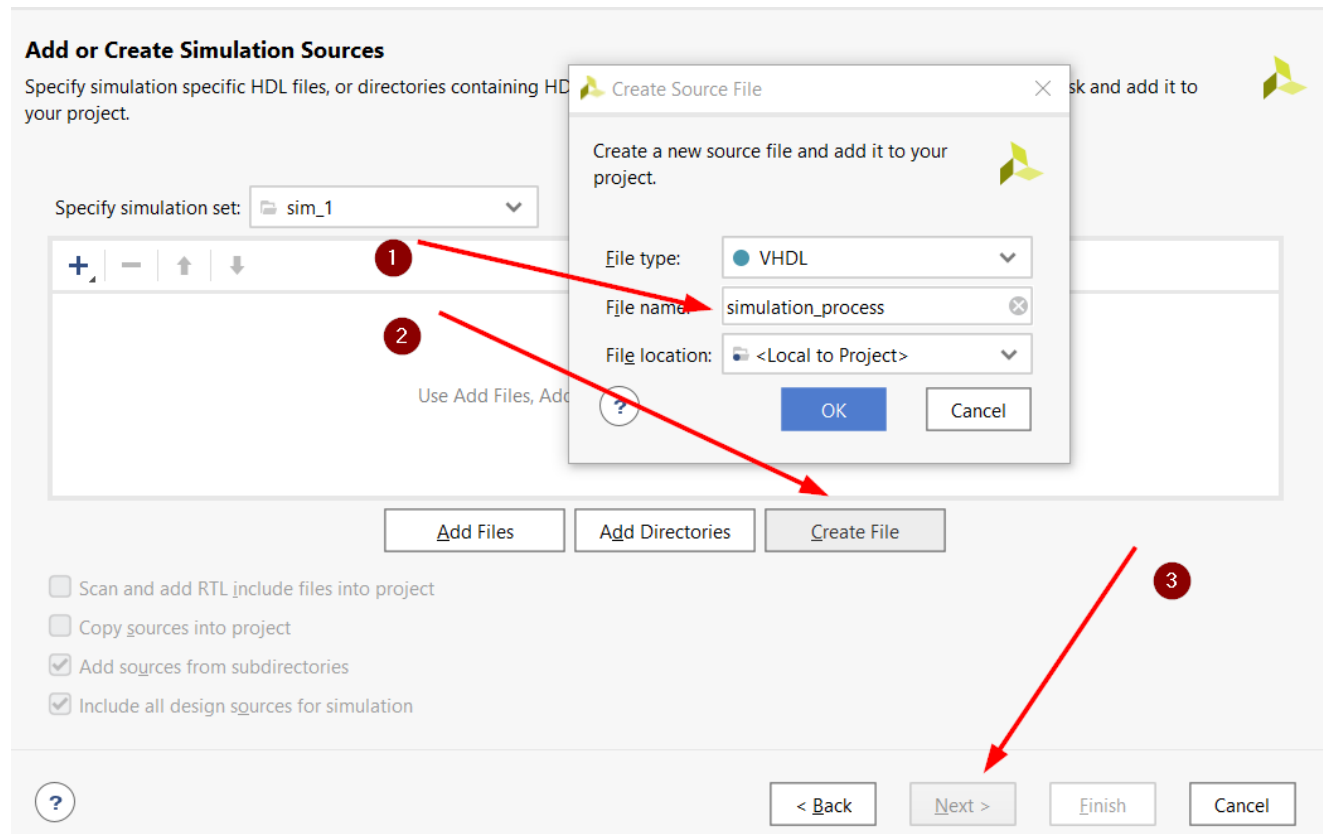
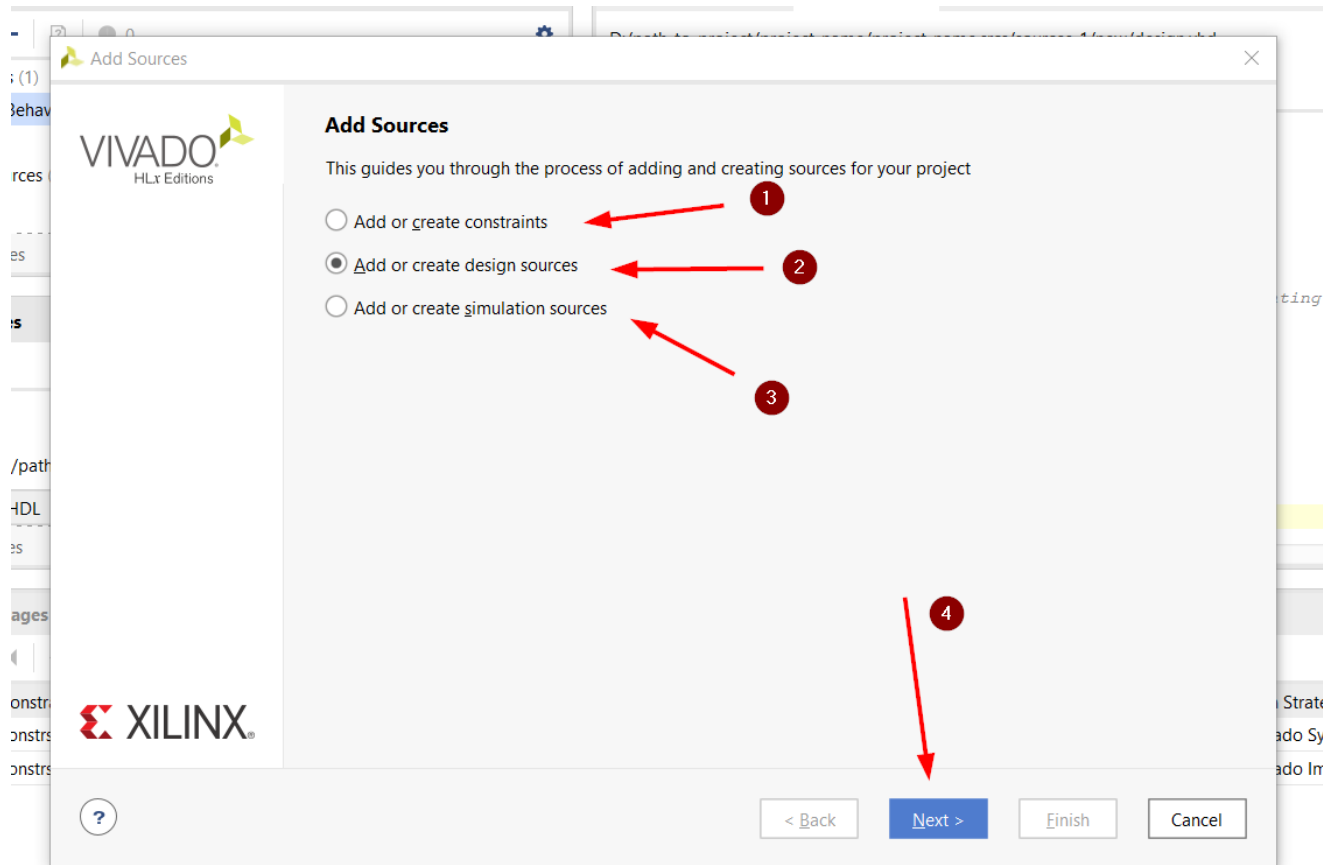
< Back

Next >

Finish

Cancel

## Add Sources (Alt+A)



# Run simulation

The screenshot shows the Xilinx IDE interface with the 'Flow' menu open. The 'Run Simulation' option is highlighted, and its sub-menu is also open, showing 'Run Behavioral Simulation' as the selected option. Red arrows and numbers 1, 2, and 3 indicate the steps to follow.

1. Click 'Flow' in the menu bar.

2. Click 'Run Simulation' in the dropdown menu.

3. Click 'Run Behavioral Simulation' in the sub-menu.

The 'Flow Navigator' on the left shows the project structure, including 'PROJECT MANAGER', 'IP INTEGRATION', 'SIMULATION', 'RTL ANALYSIS', and 'SYNTHESIS'. The 'Design Runs' tab at the bottom shows a table of simulation runs.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power
synth_1	constrs_1	Not started						