TOY ISA 1

Instruction Set Architecture Specification

Proteus Lab

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Table of Contents

J

Encoding

31:26	25:0
100111	index

Assembler

```
J target
```

Semantics

```
PC ← PC[31:28] || instr_index || 0b00
```

SYSCALL

Encoding

31:26	25:6	5:0
000000	code	111110

Assembler

```
SYSCALL
```

Semantics

```
SigException(SystemCall)
```

Notes

`X8` — system call number, `X0` - `X7` — args, `X0` — result, see man syscall

STP

Encoding

31:26	25:21	20:16	15:11	10:0
001000	base	rt1	rt2	offset

Assembler

```
STP rt1, rt2, offset(base)
```

Semantics

```
addr ← X[base] + sign_extend(offset)
```

```
memory[addr] ← X[rt1]
```

```
memory[addr + 4] ← X[rt2]
```

Notes

The lowest 2 bits of the `#offset` field must be zero. If they are not, the result of the instruction is undefined (misaligned access).

RORI

Encoding

31:26	25:21	20:16	15:11	10:0
111011	rd	rs	imm5	00000000000

Assembler

```
RORI rd, rs, #imm5
```

Semantics

```
X[rd] ← rotate_right(X[rs], imm5)
```

Notes

Rotates the bits of the `X[rs]` register to the right by `#imm` bits

SLTI

Encoding

31:26	25:21	20:16	15:0
010110	rs	rt	imm

Assembler

```
SLTI rt, rs, #imm
```

Semantics

```
X[rt] ← X[rs] < sign_extend(imm)
```

ST

Encoding

31:26	25:21	20:16	15:0
000011	base	rt	offset

Assembler

```
ST rt, offset(base)
```

Semantics

```
memory[X[base] + sign_extend(offset)] ← X[rt]
```

Notes

The lowest 2 bits of the `#offset` field must be zero. If they are not, the result of the instruction is undefined (misaligned access).

BDEP

Encoding

31:26	25:21	20:16	15:11	10:6	5:0
000000	rd	rs1	rs2	00000	111010

Assembler

```
BDEP rd, rs1, rs2
```

Semantics

```
X[rd] ← bit_deposit(X[rs1], X[rs1])
```

Notes

Places the least significant bits of `X[rs1]` into the positions specified by the mask `X[rs2]`. The remaining bits are filled with zeros.

CLS

Encoding

31:26	25:21	20:16	15:6	5:0
000000	rd	rs	0000000000	111001

Assembler

```
CLS rd, rs
```

Semantics

```
X[rd] ← count_leading_signs(X[rs])
```

Notes

Counts the number of leading ones bits in the `X[rs1]` register.

ADD

Encoding

31:26	25:21	20:16	15:11	10:6	5:0
000000	rs	rt	rd	00000	101011

Assembler

```
ADD rd, rs, rt
```

Semantics

```
X[rd] ← X[rs] + X[rt]
```

BNE

Encoding

31:26	25:21	20:16	15:0
100100	rs	rt	offset

Assembler

```
BNE rs, rt, #offset
```

Semantics

```
target ← sign_extend(offset || 0b00)
```

```
cond ← (X[rs] != X[rt])
```

```
PC ← if (cond) PC + target else PC + 4
```

BEQ

Encoding

31:26	25:21	20:16	15:0
000010	rs	rt	offset

Assembler

```
BEQ rs, rt, #offset
```

Semantics

```
target ← sign_extend(offset || 0b00)
```

```
cond ← (X[rs] == X[rt])
```

```
PC ← if (cond) PC + target else PC + 4
```

LD

Encoding

31:26	25:21	20:16	15:0
011010	base	rt	offset

Assembler

```
LD rt, offset(base)
```

Semantics

```
X[rt] ← memory[X[base] + sign_extend(offset)]
```

Notes

The lowest 2 bits of the `#offset` field must be zero. If they are not, the result of the instruction is undefined (misaligned access).

AND

Encoding

31:26	25:21	20:16	15:11	10:6	5:0
000000	rs	rt	rd	00000	101101

Assembler

```
AND rd, rs, rt
```

Semantics

```
X[rd] ← X[rs] and X[rt]
```

SSAT

Encoding

31:26	25:21	20:16	15:11	10:0
001111	rd	rs	imm5	00000000000

Assembler

```
SSAT rd, rs, #imm5
```

Semantics

```
X[rd] ← saturate_signed(X[rs], imm5)
```

Notes

Saturation of the signed value in `X[rs]` to N bits, where N = `#imm`