GC9A01

a-Si TFT LCD Single Chip Driver

240RGBx240 Resolution

Data Sheet

Rev.1.1

2020-05-03

GENERATION REVISION HISTORY

REV.	EFFECTIVE DATE	DESCRIPTION OF CHANGES	PREPARED BY
1.0	2019-07-02	New Created	June
1.1	2020-05-03	modified	Aaron

Table of Content

1. Introduction

GC9A01 is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 240RGBx240 dots, comprising a 360-channel source driver, a 32-channel gate driver, 129,600 bytes GRAM for graphic display data of 240RGBx240 dots, and power supply circuit.

GC9A01 supports parallel 8-/9-/12-/16-/18-bit data bus MCU interface, 6-/12-/16-/18-bit data bus RGB interface and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

GC9A01 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the GC9A01 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

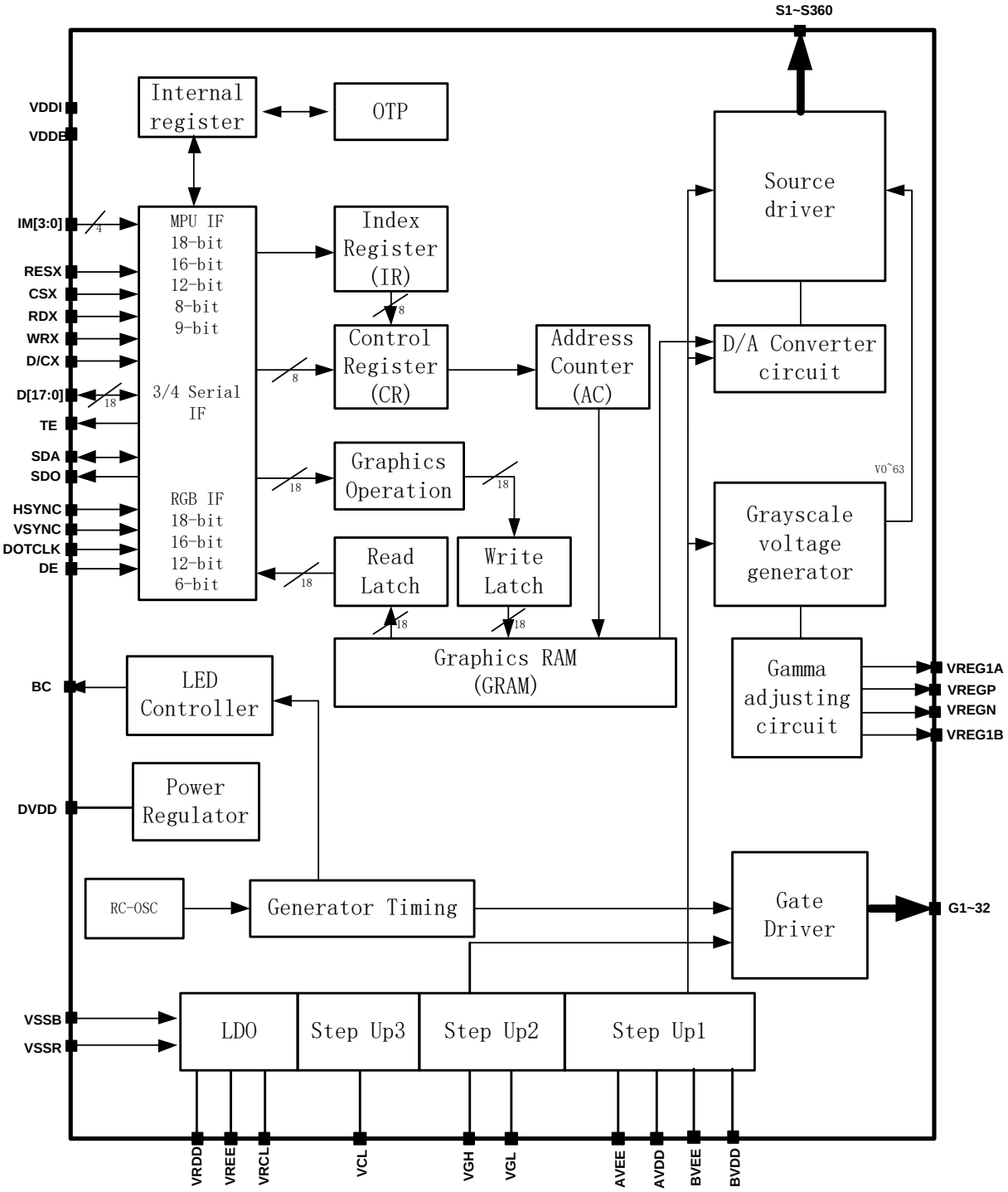
2. Features

- Dual gate TFT LCD driver with 0D 0C
- Display resolution: [240xRGB](H) x 240(V)
- Output:
  - 360 source outputs
  - 32 gate outputs
- Resolution:
  80x160：S121-S240
  120x120 120x240：S91-S270
  128x128：S85-S276
  160x160：S61-S300
  240x240：S1-S360
- a-TFT LCD driver with on-chip full display RAM: 129,600 bytes
- System Interface
  - 8-bits, 9-bits, 12-bits,16-bits, 18-bits interface with 8080-I /8080-II series MCU
  - 6-bits, 12-bits, 16-bits, 18-bits RGB interface with graphic controller
  - 8-bits, 9-bits 24bit Serial Peripheral Interface (SPI) and 2 data lane SPI
- Display mode:
  - Full color mode (Idle mode OFF): 262K-color (selectable color depth mode by software)
  - Reduce color mode (Idle mode ON): 8-color
- Power saving mode:
  - Sleep mode
- Frame rate
  -Normal mode（20hz~90hz）
  -Idle mode （1Hz~60Hz）
- On chip functions:
  - Timing generator
  - Oscillator
  - DC/DC converter
  - Dot/column inversion
- Low -power consumption architecture
  - Low operating power supplies:
    - VDDI = 1.65V ~ 3.3V (logic)
    - VDDB = 2.5V ~ 3.3V (analog)
- LCD Voltage drive:
  - Source/Gamma power supply voltage
    - GVDD - GVCL = 6.4V ~-4.6V
  - Gate driver output voltage
    - VGH - GND = 8.0V ~ 12.0V
    - VGL - GND = -11.0V ~ -7.0V
  - VCOM connect to GND
- Operate temperature range: -40℃to 80℃

3. Block Diagram

3.1. Block diagram

Figure1



3.2. Pin Description

Table 1.

Power Supply Pins			
Pin Name	I/O	Connect Pin	Descriptions
VDDI(IOVCC)	I	VDDI	Low voltage power supply for interface logic circuits(1.65~3.3V)
VDDB	I	VDDB	High voltage power supply for analog circuit blocks(2.5~3.3V)
VSSB/VSSR	I	GND	System ground level

Table 2

<table>
<tr><th colspan="4">Interface Logic Signals</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Connect Pin</th><th>Descriptions</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>(VDDI/ GND)</td><td>-Select the MCU interface mode
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">MCU-Interface</th><th colspan="2">Pins in use</th></tr>
<tr><th>Register</th><th>GRAM</th></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>8080 MCU 8-bit bus interface I</td><td>D[7:0]</td><td>D[7:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>8080 MCU16-bit bus interface I</td><td>D[7:0]</td><td>D[15:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>8080 MCU 9-bit bus interface I</td><td>D[7:0]</td><td>D[8:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>8080 MCU18-bit bus interface I</td><td>D[7:0]</td><td>D[17:0]</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td>3-wire 9-bit data serial interface I</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>2 data line serial interface I</td><td colspan="2">SDA: In/OUT
DCX:In</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>4-wire 8-bit data serial interface I</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 16-bit bus interface II</td><td>D[8:1]</td><td>D[17:10] ,D[8:1]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 8-bit bus interface II</td><td>D[17:10]</td><td>D[17:10]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 18-bit bus interface II</td><td>D[8:1]</td><td>D[17:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 9-bit bus interface II</td><td>D[17:10]</td><td>D[17:9]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface II</td><td colspan="2">SDA: In/SDO:OUT</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>4-wire 8-bit data serial interface II</td><td colspan="2">SDA: In/SDO:OUT</td></tr>
</table>
MPU Parallel interface bus and serial interface select
If use RGB Interface must select serial interface.
Fix this pin at VDDI or GND.</td></tr>
<tr><td>RESX</td><td>I</td><td>MCU (VDDI/GND)</td><td>This signal will reset the device and must be applied to properly initialize the chip.
Signal is active low.</td></tr>
<tr><td>CSX</td><td>I</td><td>MCU (VDDI/GND)</td><td>Chip select input pin("Low" enable).
This pin can be permanently fixed "Low" in MPU interface mode only.</td></tr>
<tr><td>D/CX (SCL)</td><td>I</td><td>MCU (VDDI/</td><td>This pin is used to select "Data or Command" in the parallel interface
When DCX='1', data is selected.</td></tr>
</table>

		GND)	When DCX='0', command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. If not used, this pin should be connected to VDDI or GND.
RDX	I	MCU (VDDI/ GND)	8080-I/8080-II system (RDX): Serves as a read signal and MCU read data at the rising edge. Fix to VDDI level when not in use
WRX (D/CX)	I	MCU (VDDI/ GND)	8080-I/8080-II system (WRX): Serves as a write signal and writes data at the rising edge. 4-line system (D/CX): Serves as command or parameter select. Fix to VDDI level when not in use.
D[17:0]	I/O	MCU (VDDI/ GND)	18-bit parallel bi-directional data bus for MCU system and RGB interface mode Fix to GND level when not in use
SDA	I/O	MCU (VDDI/ GND)	When IM[3]:Low, Serial in/out signal in 3-wire 9-bit/4-wire 8-bit serial data interface. When IM[3]:High, Serial input signal in 3-wire 9-bit/4-wire 8-bit serial data interface. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VDDI or GND.
SDO	O	MCU (VDDI/GND)	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin
TE	O	MCU (VDDI/ GND)	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
DOTCL K	I	MCU (VDDI/GND)	Dot clock signal for RGB interface operation. Fix to VDDI or GND level when not in use.
VSYNC	I	MCU (VDDI/GND)	Frame synchronizing signal for RGB interface operation. Fix to VDDI or GND level when not in use.
HSYNC	I	MCU (VDDI/ GND)	Line synchronizing signal for RGB interface operation. Fix to VDDI or GND level when not in use.
DE	I	MCU (VDDI/ GND)	Data enable signal for RGB interface operation. Fix to VDDI or GND level when not in use.

Note:

1. If CSX is connected to GND in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.

2. When CSX='1', there is no influence to the parallel and serial interface.

Table 3

LCD Driver Input/Output Pins			
Pin Name	I/O	Connect Pin	Descriptions
S360~S1	O	LCD	Source output signals. Leave the pin to open when not in use.
G1~G32	O	LCD	Gate output signals. Leave the pin to open when not in use.
VCOM	O	GND	Connect to GND.
VRDD	O	Power	Power supply for AVDD.
VREE	O	Power	Power supply for AVEE.
VRCL	O	Power	Power supply for VCL.
AVDD	O	Power	Analog power for Source.
AVEE	O	Power	Analog power for Source.
VGH	O	Power	Power supply for the gate driver(Positive).
VGL	O	Power	Power supply for the gate driver(Negative).
VREG1A	O	Ref	VREG1A is the highest positive grayscale reference voltage of source driver.
VREG_VREF	O	Ref	VREG_VREF is the lowest positive grayscale reference voltage of source driver.
VREGP	O	Ref	VREGP is the highest negative grayscale reference voltage of source driver.
VREGN	O	Ref	VREGN is the highest negative grayscale reference voltage of source driver.
BC	O	Dig IO	Output pin for PWM(Pulse width Modulation) signal of LED driving. If not used, open this pin.

Table 4

Test Pins			
Pin Name	I/O	Connect Pin	Descriptions
OSC_IN	I/O	Open	Test pin
OSC_TEST	I/O	Open	Test pin
VPP	I/O	Open	Test pin
DUMMY	-	Open	Input pads used only for test purpose at IC-side. During normal operation ,leave these pads open.

Liquid crystal power supply specifications Table

Table 5

No.	Item		Description
1	TFT Source Driver		support 240*RGB（max）
2	TFT Gate Driver		32 pins
3	TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	S1~S360	V0~V63 grayscales
		G1~G32	VGH-VGL
5	Input Voltage	VDDI	1.65~3.30V
		VDDB	2.50~3.30V
6	Liquid Crystal Drive Voltages	AVDD	6.5~7.5V
		AVEE	-5.5V~-4.5V
		VGH	8.0~12.0V
		VGL	-11.0~-7.0V
		VCL	-3.0~-1.5V
7	Internal Step-up Circuits	AVDD	VDDB*3
		AVEE	VDDB*-2
		VGH	VDDB*5
		VGL	VDDB*-5
		VCL	VDDB*-1

3.3. PAD coordinates

No.	Pad name	X	Y
1	VCOM	-4904.5	-306
2	VCOM	-4854.5	-306
3	VCOM	-4804.5	-306
4	VCOM	-4754.5	-306
5	VCOM	-4704.5	-306
6	DUM0	-4654.5	-306
7	VGH	-4604.5	-306
8	VGH	-4554.5	-306
9	VGH	-4504.5	-306
10	VGH	-4454.5	-306
11	VGH	-4404.5	-306
12	VGL	-4354.5	-306
13	VGL	-4304.5	-306
14	VGL	-4254.5	-306
15	VGL	-4204.5	-306
16	VGL	-4154.5	-306
17	VCL	-4104.5	-306
18	VCL	-4054.5	-306
19	VCL	-4004.5	-306
20	VRCL	-3954.5	-306
21	VRCL	-3904.5	-306
22	VRCL	-3854.5	-306
23	AVDD	-3804.5	-306
24	AVDD	-3754.5	-306
25	AVDD	-3704.5	-306
26	AVDD	-3654.5	-306
27	VRDD	-3604.5	-306
28	VRDD	-3554.5	-306
29	VRDD	-3504.5	-306
30	VSSB	-3454.5	-306
31	VSSB	-3404.5	-306
32	VSSB	-3354.5	-306
33	VSSB	-3304.5	-306
34	VSSB	-3254.5	-306
35	VDDB	-3204.5	-306
36	VDDB	-3154.5	-306
37	VDDB	-3104.5	-306
38	VDDB	-3054.5	-306
39	VDDB	-3004.5	-306
40	DUM1	-2954.5	-306
41	BVDD	-2904.5	-306
42	BVDD	-2854.5	-306
43	BVDD	-2804.5	-306
44	BVEE	-2754.5	-306
45	BVEE	-2704.5	-306
46	BVEE	-2654.5	-306
47	DUM2	-2604.5	-306
48	DUM2	-2554.5	-306
49	DUM2	-2504.5	-306
50	DUM3	-2454.5	-306
51	DUM3	-2404.5	-306
52	DUM3	-2354.5	-306
53	DUM4	-2304.5	-306
54	DUM4	-2254.5	-306
55	DUM4	-2204.5	-306
56	DUM5	-2154.5	-306
57	DUM5	-2104.5	-306
58	DUM5	-2054.5	-306
59	DUM6	-2004.5	-306
60	DVDD	-1954.5	-306
61	DVDD	-1904.5	-306
62	DVDD	-1854.5	-306
63	VDDSF	-1804.5	-306
64	VDDSF	-1754.5	-306
65	VDDSF	-1704.5	-306
66	VSSB	-1654.5	-306
67	VSSB	-1604.5	-306
68	VSSB	-1554.5	-306
69	VSSB	-1504.5	-306
70	VSSB	-1454.5	-306
71	VDDB	-1404.5	-306
72	VDDB	-1354.5	-306
73	VDDB	-1304.5	-306
74	VDDB	-1254.5	-306
75	VDDB	-1204.5	-306
76	VDDI	-1154.5	-306
77	VDDI	-1104.5	-306
78	VDDI	-1054.5	-306
79	VDDI	-1004.5	-306
80	VDDI	-954.5	-306
81	REF_TEST	-896	-306
82	REF_TEST	-836	-306
83	RESX	-776	-306
84	WRX	-716	-306
85	CSX	-656	-306
86	DCX	-596	-306
87	RDX	-536	-306
88	DOTCLK	-476	-306
89	ENABLE	-416	-306
90	VSYNC	-356	-306
91	HSYNC	-296	-306
92	BC	-236	-306
93	TE	-176	-306
94	SDO	-116	-306
95	SDA	-50	-306
96	DB<17>	22	-306
97	DB<16>	94	-306
98	DB<15>	166	-306
99	DB<14>	238	-306
100	DB<13>	310	-306
101	DB<12>	382	-306
102	DB<11>	454	-306
103	DUM7	526	-306
104	DB<10>	598	-306
105	DB<9>	670	-306
106	DUM8	742	-306
107	DUM9	843	-306
108	DB<8>	915	-306
109	DB<7>	987	-306
110	DB<6>	1059	-306
111	DB<5>	1131	-306
112	DB<4>	1203	-306
113	DB<3>	1275	-306
114	DB<2>	1347	-306
115	DB<1>	1419	-306
116	DB<0>	1491	-306
117	DUM10	1554.5	-306
118	IM<0>	1604.5	-306
119	IM<1>	1654.5	-306
120	IM<2>	1704.5	-306
121	IM<3>	1754.5	-306
122	OSC_IN	1804.5	-306
123	OSC_TEST	1854.5	-306
124	DUM11	1904.5	-306
125	VSSB	1954.5	-306
126	VSSB	2004.5	-306
127	VSSB	2054.5	-306
128	VSSB	2104.5	-306
129	VSSB	2154.5	-306
130	VSSR	2204.5	-306
131	VSSR	2254.5	-306
132	VSSR	2304.5	-306
133	VSSR	2354.5	-306
134	VSSR	2404.5	-306
135	DUM12	2454.5	-306
136	VPP	2504.5	-306
137	VREG1A	2554.5	-306
138	VREG1A	2604.5	-306
139	VREGP	2654.5	-306
140	VREGP	2704.5	-306
141	VREG_VREF	2754.5	-306
142	VREG_VREF	2804.5	-306
143	DUM13	2854.5	-306
144	DUM13	2904.5	-306
145	DUM14	2954.5	-306
146	DUM14	3004.5	-306
147	DUM15	3054.5	-306
148	VDDB	3104.5	-306
149	VDDB	3154.5	-306
150	VDDB	3204.5	-306

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad	X	Y
151	VDDB	3254.5	-306	201	GOUT<4>	4300	306	251	S<23>	2798	166
152	VDDB	3304.5	-306	202	GOUT<5>	4262	306	252	S<24>	2784	291
153	DUM15	3354.5	-306	203	GOUT<5>	4224	306	253	S<25>	2770	166
154	DUM16	3404.5	-306	204	GOUT<6>	4186	306	254	S<26>	2756	291
155	DUM16	3454.5	-306	205	GOUT<6>	4148	306	255	S<27>	2742	166
156	DUM17	3504.5	-306	206	GOUT<7>	4110	306	256	S<28>	2728	291
157	DUM17	3554.5	-306	207	GOUT<7>	4072	306	257	S<29>	2714	166
158	DUM17	3604.5	-306	208	GOUT<8>	4034	306	258	S<30>	2700	291
159	DUM18	3654.5	-306	209	GOUT<8>	3996	306	259	S<31>	2686	166
160	DUM18	3704.5	-306	210	GOUT<9>	3958	306	260	S<32>	2672	291
161	DUM19	3754.5	-306	211	GOUT<9>	3920	306	261	S<33>	2658	166
162	DUM19	3804.5	-306	212	GOUT<10>	3882	306	262	S<34>	2644	291
163	VSSB	3854.5	-306	213	GOUT<10>	3844	306	263	S<35>	2630	166
164	VSSB	3904.5	-306	214	GOUT<11>	3806	306	264	S<36>	2616	291
165	VSSB	3954.5	-306	215	GOUT<11>	3768	306	265	S<37>	2602	166
166	VSSB	4004.5	-306	216	GOUT<12>	3730	306	266	S<38>	2588	291
167	VSSB	4054.5	-306	217	GOUT<12>	3692	306	267	S<39>	2574	166
168	VREGN	4104.5	-306	218	GOUT<13>	3654	306	268	S<40>	2560	291
169	VREGN	4154.5	-306	219	GOUT<13>	3616	306	269	S<41>	2546	166
170	VREGN	4204.5	-306	220	GOUT<14>	3578	306	270	S<42>	2532	291
171	AVEE	4254.5	-306	221	GOUT<14>	3540	306	271	S<43>	2518	166
172	AVEE	4304.5	-306	222	GOUT<15>	3502	306	272	S<44>	2504	291
173	AVEE	4354.5	-306	223	GOUT<15>	3464	306	273	S<45>	2490	166
174	VREE	4404.5	-306	224	GOUT<16>	3426	306	274	S<46>	2476	291
175	VREE	4454.5	-306	225	GOUT<16>	3388	306	275	S<47>	2462	166
176	VREE	4504.5	-306	226	DUM23	3350	306	276	S<48>	2448	291
177	DUM20	4554.5	-306	227	DUM24	3134	166	277	S<49>	2434	166
178	DUM20	4604.5	-306	228	DUM25	3120	291	278	S<50>	2420	291
179	DUM20	4654.5	-306	229	S<1>	3106	166	279	S<51>	2406	166
180	VCOM	4704.5	-306	230	S<2>	3092	291	280	S<52>	2392	291
181	VCOM	4754.5	-306	231	S<3>	3078	166	281	S<53>	2378	166
182	VCOM	4804.5	-306	232	S<4>	3064	291	282	S<54>	2364	291
183	VCOM	4854.5	-306	233	S<5>	3050	166	283	S<55>	2350	166
184	VCOM	4904.5	-306	234	S<6>	3036	291	284	S<56>	2336	291
185	DUM21	4908	306	235	S<7>	3022	166	285	S<57>	2322	166
186	DUM22	4870	306	236	S<8>	3008	291	286	S<58>	2308	291
187	DUM22	4832	306	237	S<9>	2994	166	287	S<59>	2294	166
188	DUM22	4794	306	238	S<10>	2980	291	288	S<60>	2280	291
189	DUM22	4756	306	239	S<11>	2966	166	289	S<61>	2266	166
190	VGL	4718	306	240	S<12>	2952	291	290	S<62>	2252	291
191	VGL	4680	306	241	S<13>	2938	166	291	S<63>	2238	166
192	VGL	4642	306	242	S<14>	2924	291	292	S<64>	2224	291
193	VGL	4604	306	243	S<15>	2910	166	293	S<65>	2210	166
194	GOUT<1>	4566	306	244	S<16>	2896	291	294	S<66>	2196	291
195	GOUT<1>	4528	306	245	S<17>	2882	166	295	S<67>	2182	166
196	GOUT<2>	4490	306	246	S<18>	2868	291	296	S<68>	2168	291
197	GOUT<2>	4452	306	247	S<19>	2854	166	297	S<69>	2154	166
198	GOUT<3>	4414	306	248	S<20>	2840	291	298	S<70>	2140	291
199	GOUT<3>	4376	306	249	S<21>	2826	166	299	S<71>	2126	166
200	GOUT<4>	4338	306	250	S<22>	2812	291	300	S<72>	2112	291

No.	Pad name	X	Y	No.	Pad	X	Y	No.	Pad name	X	Y
301	S<73>	2098	166	351	S<123>	1398	166	401	S<173>	698	166
302	S<74>	2084	291	352	S<124>	1384	291	402	S<174>	684	291
303	S<75>	2070	166	353	S<125>	1370	166	403	S<175>	670	166
304	S<76>	2056	291	354	S<126>	1356	291	404	S<176>	656	291
305	S<77>	2042	166	355	S<127>	1342	166	405	S<177>	642	166
306	S<78>	2028	291	356	S<128>	1328	291	406	S<178>	628	291
307	S<79>	2014	166	357	S<129>	1314	166	407	S<179>	614	166
308	S<80>	2000	291	358	S<130>	1300	291	408	S<180>	600	291
309	S<81>	1986	166	359	S<131>	1286	166	409	DUM26	586	166
310	S<82>	1972	291	360	S<132>	1272	291	410	DUM27	572	291
311	S<83>	1958	166	361	S<133>	1258	166	411	DUM28	-572	291
312	S<84>	1944	291	362	S<134>	1244	291	412	DUM29	-586	166
313	S<85>	1930	166	363	S<135>	1230	166	413	S<181>	-600	291
314	S<86>	1916	291	364	S<136>	1216	291	414	S<182>	-614	166
315	S<87>	1902	166	365	S<137>	1202	166	415	S<183>	-628	291
316	S<88>	1888	291	366	S<138>	1188	291	416	S<184>	-642	166
317	S<89>	1874	166	367	S<139>	1174	166	417	S<185>	-656	291
318	S<90>	1860	291	368	S<140>	1160	291	418	S<186>	-670	166
319	S<91>	1846	166	369	S<141>	1146	166	419	S<187>	-684	291
320	S<92>	1832	291	370	S<142>	1132	291	420	S<188>	-698	166
321	S<93>	1818	166	371	S<143>	1118	166	421	S<189>	-712	291
322	S<94>	1804	291	372	S<144>	1104	291	422	S<190>	-726	166
323	S<95>	1790	166	373	S<145>	1090	166	423	S<191>	-740	291
324	S<96>	1776	291	374	S<146>	1076	291	424	S<192>	-754	166
325	S<97>	1762	166	375	S<147>	1062	166	425	S<193>	-768	291
326	S<98>	1748	291	376	S<148>	1048	291	426	S<194>	-782	166
327	S<99>	1734	166	377	S<149>	1034	166	427	S<195>	-796	291
328	S<100>	1720	291	378	S<150>	1020	291	428	S<196>	-810	166
329	S<101>	1706	166	379	S<151>	1006	166	429	S<197>	-824	291
330	S<102>	1692	291	380	S<152>	992	291	430	S<198>	-838	166
331	S<103>	1678	166	381	S<153>	978	166	431	S<199>	-852	291
332	S<104>	1664	291	382	S<154>	964	291	432	S<200>	-866	166
333	S<105>	1650	166	383	S<155>	950	166	433	S<201>	-880	291
334	S<106>	1636	291	384	S<156>	936	291	434	S<202>	-894	166
335	S<107>	1622	166	385	S<157>	922	166	435	S<203>	-908	291
336	S<108>	1608	291	386	S<158>	908	291	436	S<204>	-922	166
337	S<109>	1594	166	387	S<159>	894	166	437	S<205>	-936	291
338	S<110>	1580	291	388	S<160>	880	291	438	S<206>	-950	166
339	S<111>	1566	166	389	S<161>	866	166	439	S<207>	-964	291
340	S<112>	1552	291	390	S<162>	852	291	440	S<208>	-978	166
341	S<113>	1538	166	391	S<163>	838	166	441	S<209>	-992	291
342	S<114>	1524	291	392	S<164>	824	291	442	S<210>	-1006	166
343	S<115>	1510	166	393	S<165>	810	166	443	S<211>	-1020	291
344	S<116>	1496	291	394	S<166>	796	291	444	S<212>	-1034	166
345	S<117>	1482	166	395	S<167>	782	166	445	S<213>	-1048	291
346	S<118>	1468	291	396	S<168>	768	291	446	S<214>	-1062	166
347	S<119>	1454	166	397	S<169>	754	166	447	S<215>	-1076	291
348	S<120>	1440	291	398	S<170>	740	291	448	S<216>	-1090	166
349	S<121>	1426	166	399	S<171>	726	166	449	S<217>	-1104	291
350	S<122>	1412	291	400	S<172>	712	291	450	S<218>	-1118	166

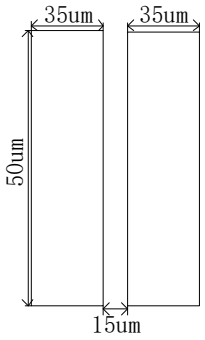
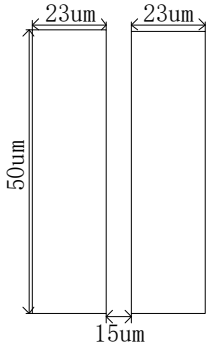
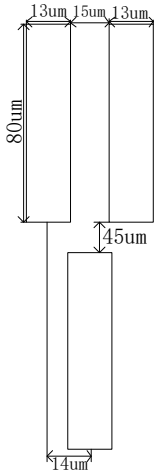
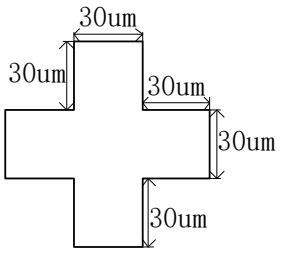
No.	Pad name	X	Y
451	S<219>	-1132	291
452	S<220>	-1146	166
453	S<221>	-1160	291
454	S<222>	-1174	166
455	S<223>	-1188	291
456	S<224>	-1202	166
457	S<225>	-1216	291
458	S<226>	-1230	166
459	S<227>	-1244	291
460	S<228>	-1258	166
461	S<229>	-1272	291
462	S<230>	-1286	166
463	S<231>	-1300	291
464	S<232>	-1314	166
465	S<233>	-1328	291
466	S<234>	-1342	166
467	S<235>	-1356	291
468	S<236>	-1370	166
469	S<237>	-1384	291
470	S<238>	-1398	166
471	S<239>	-1412	291
472	S<240>	-1426	166
473	S<241>	-1440	291
474	S<242>	-1454	166
475	S<243>	-1468	291
476	S<244>	-1482	166
477	S<245>	-1496	291
478	S<246>	-1510	166
479	S<247>	-1524	291
480	S<248>	-1538	166
481	S<249>	-1552	291
482	S<250>	-1566	166
483	S<251>	-1580	291
484	S<252>	-1594	166
485	S<253>	-1608	291
486	S<254>	-1622	166
487	S<255>	-1636	291
488	S<256>	-1650	166
489	S<257>	-1664	291
490	S<258>	-1678	166
491	S<259>	-1692	291
492	S<260>	-1706	166
493	S<261>	-1720	291
494	S<262>	-1734	166
495	S<263>	-1748	291
496	S<264>	-1762	166
497	S<265>	-1776	291
498	S<266>	-1790	166
499	S<267>	-1804	291
500	S<268>	-1818	166

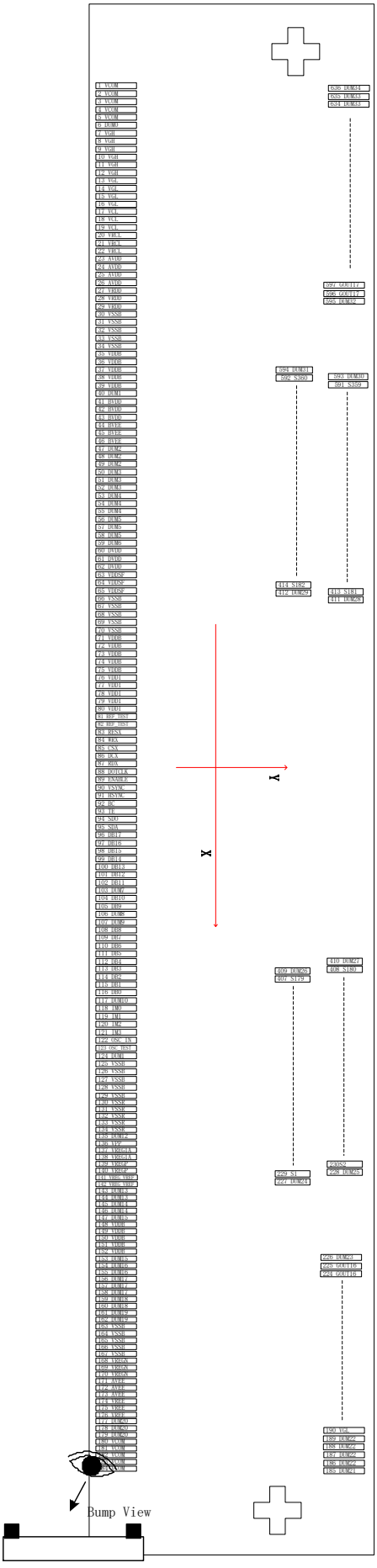
No.	Pad	X	Y
501	S<269>	-1832	291
502	S<270>	-1846	166
503	S<271>	-1860	291
504	S<272>	-1874	166
505	S<273>	-1888	291
506	S<274>	-1902	166
507	S<275>	-1916	291
508	S<276>	-1930	166
509	S<277>	-1944	291
510	S<278>	-1958	166
511	S<279>	-1972	291
512	S<280>	-1986	166
513	S<281>	-2000	291
514	S<282>	-2014	166
515	S<283>	-2028	291
516	S<284>	-2042	166
517	S<285>	-2056	291
518	S<286>	-2070	166
519	S<287>	-2084	291
520	S<288>	-2098	166
521	S<289>	-2112	291
522	S<290>	-2126	166
523	S<291>	-2140	291
524	S<292>	-2154	166
525	S<293>	-2168	291
526	S<294>	-2182	166
527	S<295>	-2196	291
528	S<296>	-2210	166
529	S<297>	-2224	291
530	S<298>	-2238	166
531	S<299>	-2252	291
532	S<300>	-2266	166
533	S<301>	-2280	291
534	S<302>	-2294	166
535	S<303>	-2308	291
536	S<304>	-2322	166
537	S<305>	-2336	291
538	S<306>	-2350	166
539	S<307>	-2364	291
540	S<308>	-2378	166
541	S<309>	-2392	291
542	S<310>	-2406	166
543	S<311>	-2420	291
544	S<312>	-2434	166
545	S<313>	-2448	291
546	S<314>	-2462	166
547	S<315>	-2476	291
548	S<316>	-2490	166
549	S<317>	-2504	291
550	S<318>	-2518	166

No.	Pad name	X	Y
551	S<319>	-2532	291
552	S<320>	-2546	166
553	S<321>	-2560	291
554	S<322>	-2574	166
555	S<323>	-2588	291
556	S<324>	-2602	166
557	S<325>	-2616	291
558	S<326>	-2630	166
559	S<327>	-2644	291
560	S<328>	-2658	166
561	S<329>	-2672	291
562	S<330>	-2686	166
563	S<331>	-2700	291
564	S<332>	-2714	166
565	S<333>	-2728	291
566	S<334>	-2742	166
567	S<335>	-2756	291
568	S<336>	-2770	166
569	S<337>	-2784	291
570	S<338>	-2798	166
571	S<339>	-2812	291
572	S<340>	-2826	166
573	S<341>	-2840	291
574	S<342>	-2854	166
575	S<343>	-2868	291
576	S<344>	-2882	166
577	S<345>	-2896	291
578	S<346>	-2910	166
579	S<347>	-2924	291
580	S<348>	-2938	166
581	S<349>	-2952	291
582	S<350>	-2966	166
583	S<351>	-2980	291
584	S<352>	-2994	166
585	S<353>	-3008	291
586	S<354>	-3022	166
587	S<355>	-3036	291
588	S<356>	-3050	166
589	S<357>	-3064	291
590	S<358>	-3078	166
591	S<359>	-3092	291
592	S<360>	-3106	166
593	DUM30	-3120	291
594	DUM31	-3134	166
595	DUM32	-3350	306
596	GOUT<17>	-3388	306
597	GOUT<17>	-3426	306
598	GOUT<18>	-3464	306
599	GOUT<18>	-3502	306
600	GOUT<19>	-3540	306

No.	Pad name	X	Y
601	GOUT<19>	-3578	306
602	GOUT<20>	-3616	306
603	GOUT<20>	-3654	306
604	GOUT<21>	-3692	306
605	GOUT<21>	-3730	306
606	GOUT<22>	-3768	306
607	GOUT<22>	-3806	306
608	GOUT<23>	-3844	306
609	GOUT<23>	-3882	306
610	GOUT<24>	-3920	306
611	GOUT<24>	-3958	306
612	GOUT<25>	-3996	306
613	GOUT<25>	-4034	306
614	GOUT<26>	-4072	306
615	GOUT<26>	-4110	306
616	GOUT<27>	-4148	306
617	GOUT<27>	-4186	306
618	GOUT<28>	-4224	306
619	GOUT<28>	-4262	306
620	GOUT<29>	-4300	306
621	GOUT<29>	-4338	306
622	GOUT<30>	-4376	306
623	GOUT<30>	-4414	306
624	GOUT<31>	-4452	306
625	GOUT<31>	-4490	306
626	GOUT<32>	-4528	306
627	GOUT<32>	-4566	306
628	VGL	-4604	306
629	VGL	-4642	306
630	VGL	-4680	306
631	VGL	-4718	306
632	DUM33	-4756	306
633	DUM33	-4794	306
634	DUM33	-4832	306
635	DUM33	-4870	306
636	DUM34	-4908	306

Name	X-axis	Y-axis
left mark	-5000	230
right mark	5000	230

Chip Size(include scribe line):750umx10800um	
Chip thickness: 300um	
Bump height: 9um	
Input Pads 1~80：35um X 50um pitch：50um 81~94：38um X 50um pitch：60um 95~116：50um X 50um pitch：72um 117~184 ： 35um X 50um pitch：50um	 pad 1~80
Gout Pads 185~226,595~636	
Source Pads 227~594	
Mark The left is the same with the right	



4. Interface setting

4.1. MCU interfaces

GC9A01 provides the 8-/9-/12-/16-/18-bit parallel system interface for 8080-I /8080- II series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [3:0] and the bit formal per pixel color order is selected by DBI [2:0] 3-bits of 3Ah register.

4.1.1. MCU interface selection

The selection of interface is done by setting external pins IM [3:0] as shown in the following table.

Table 6

IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
					Register/Content	GRAM
0	1	0	0	8080 MCU 8-bit bus interface I	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX
0	1	1	0	8080 MCU 16-bit bus interface I	D[7:0]	D[15:0],WRX,RDX,CSX,D/CX
0	1	0	1	8080 MCU 9-bit bus interface I	D[7:0]	D[8:0],WRX,RDX,CSX,D/CX
0	1	1	1	8080 MCU 18-bit bus interface I	D[7:0]	D[17:0],WRX,RDX,CSX,D/CX
1	1	0	1	3-wire 9-bit data serial interface I	SCL,SDA,CSX	
				2 data line serial interface I	SCL,SDA,CSX,DCX	
1	1	1	1	4-wire 8-bit data serial interface I	SCL,SDA,D/CX,CSX	
0	0	1	0	8080 MCU 16-bit bus interface II	D[8:1]	D[17:10],D[8:1],WRX,RDX,CSX,D/CX
0	0	0	0	8080 MCU 8-bit bus interface II	D[17:10]	D[17:10],WRX,RDX,CSX,D/CX
0	0	1	1	8080 MCU 18-bit bus interface II	D[8:1]	D[17:0],WRX,RDX,CSX,D/CX
0	0	0	1	8080 MCU 9-bit bus interface II	D[17:10]	D[17:9],WRX,RDX,CSX,D/CX
1	0	0	1	3-wire 9-bit data serial interface II	SCL,SDA,CSX,SDO	
1	0	1	1	4-wire 8-bit data serial interface II	SCL,SDA,D/CX,CSX,SDO	

4.1.2. 8080-I Series Parallel Interface

GC9A01 can be accessed via 8-/9-/12-/16-/18-bit MCU 8080-I series parallel interface. The chip select CSX (active low) is used to enable or disable GC9A01 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

GC9A01 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D[17:0] bits are commands.

The 8080-I series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-I Interface selection is done when IM3 pin is low state (VSSR level). Interface bus width can be selected by IM [2:0] bits.
The selection of 8080-I series parallel interface is shown as the table in the following.

Table 7

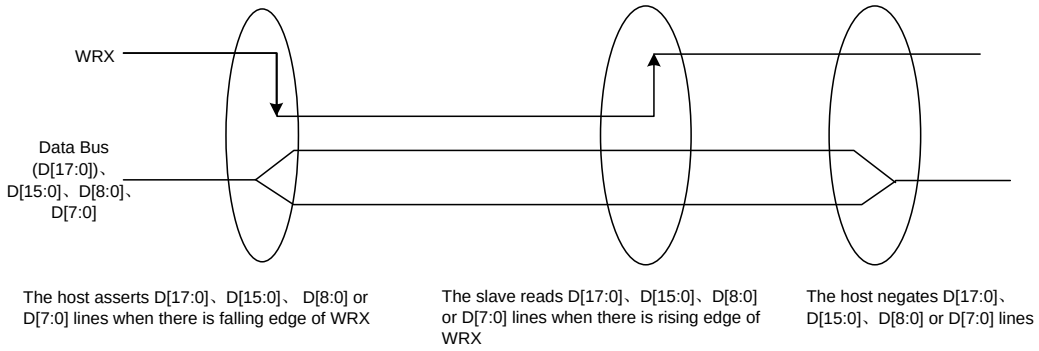
IM3	IM2	IM1	IM0	MCU-Interface	CSX	WRX	RDX	D/CX	Function
0	1	0	0	8080 MCU 8-bit bus interface I	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	1	1	0	8080 MCU 16-bit bus interface I	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	1	0	1	8080 MCU 9-bit bus interface I	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	1	1	1	8080 MCU 18-bit bus interface I	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.

4.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is SRAM data or command's parameter.

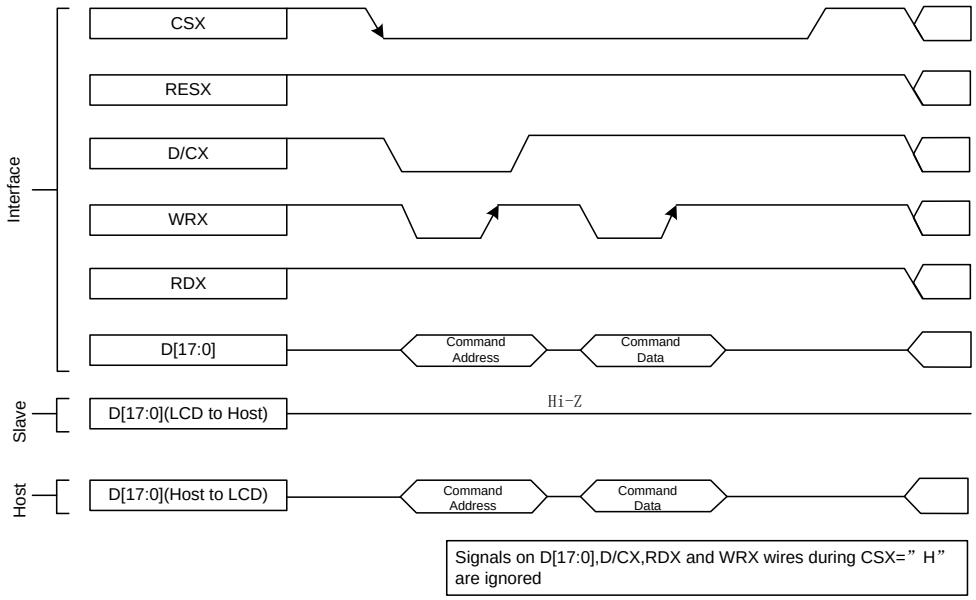
The following figure shows a write cycle for the 8080-I MCU interface.

Figure 2.



Note: WRX is an unsynchronized signal (It can be stopped)

Figure 3.

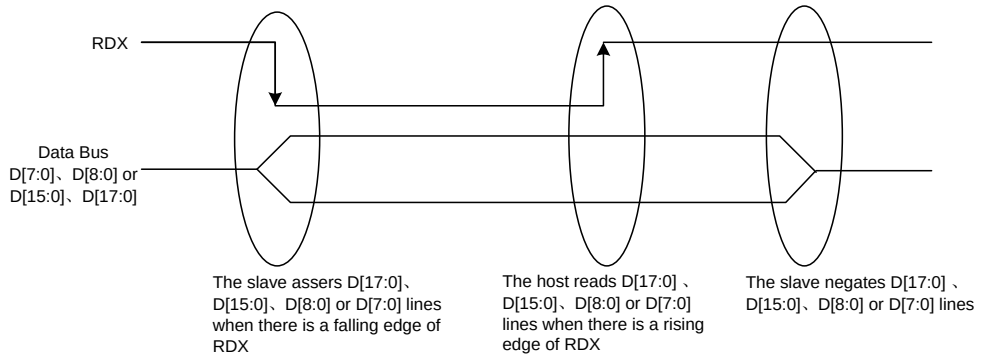


4.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle, while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

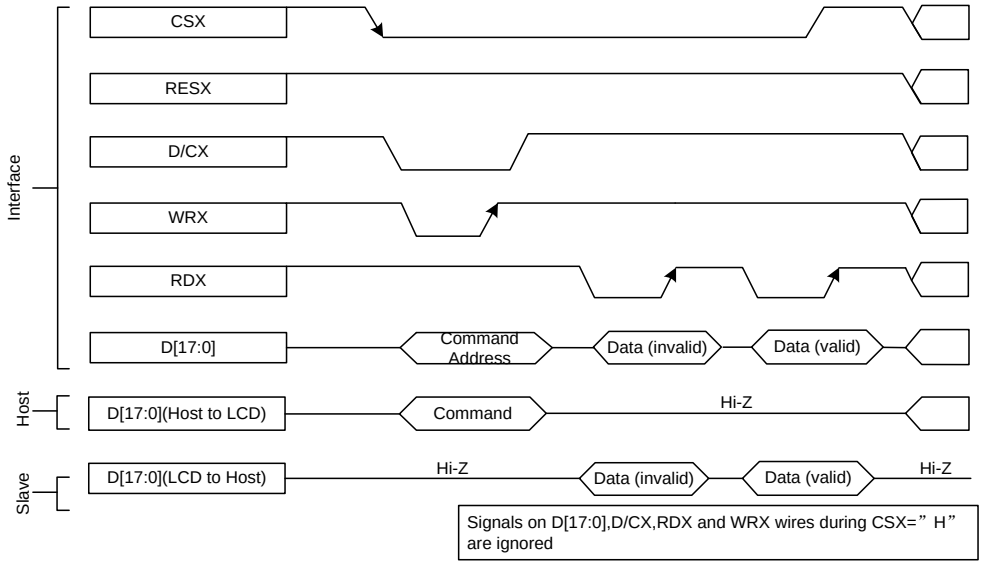
The following figure shows the read cycle for the 8080-I MCU interface.

Figure 4.



Note: RDX is an unsynchronized signal (It can be stopped).

Figure 5.



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

4.1.5. 8080-Ⅱ Series Parallel Interface

GC9A01 can be accessed via 8-/9-/16-/18-bit MCU 8080-Ⅱ series parallel interface. The chip select CSX (active low) is used to enable or disable GC9A01 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

GC9A01 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D[17:0] bits are commands.

The 8080-II series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-II Interface selection is done when IM3 pin is low state. Interface bus width can be selected by IM [2:0] bits.

The selection of 8080-II series parallel interface is shown as the table in the following.

Table 8

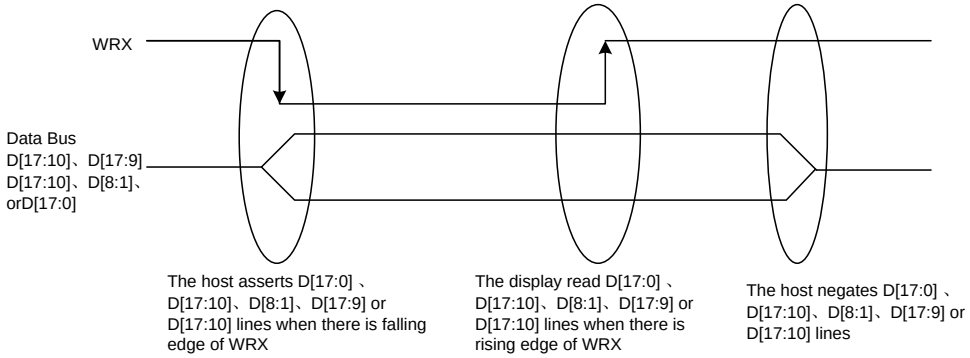
IM3	IM2	IM1	IM0	MCU-Interface	CSX	WRX	RDX	D/CX	Function
0	0	1	0	8080 MCU 16-bit bus interface II	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	0	0	8080 MCU 8-bit bus interface II	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	1	1	8080 MCU 18-bit bus interface II	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	0	1	8080 MCU 9-bit bus interface II	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.

4.1.6. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

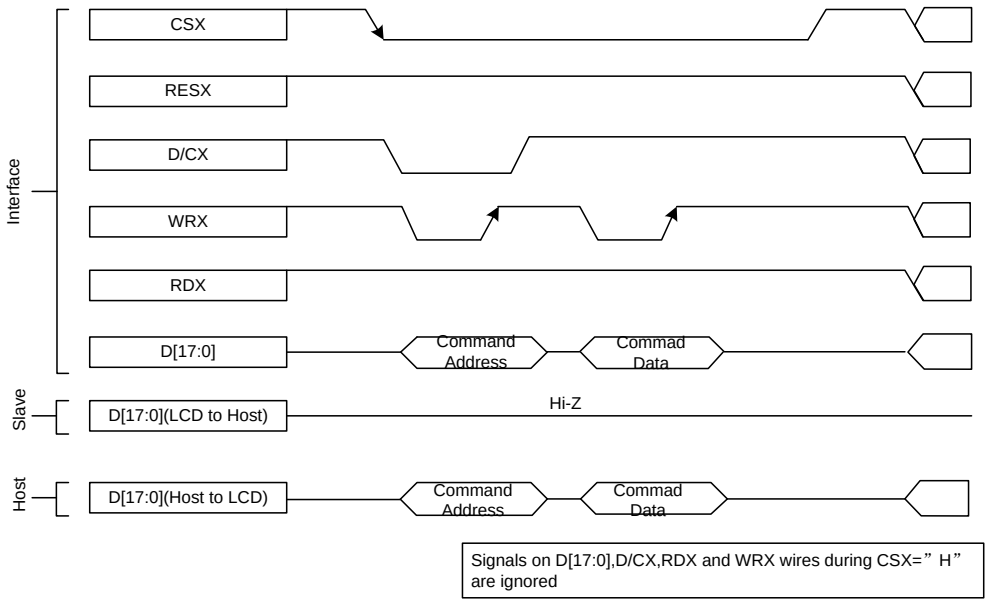
The following figure shows a write cycle for the 8080-II MCU interface.

Figure 6.



Note: WRX is an unsynchronized signal (It can be stopped)

Figure 7.

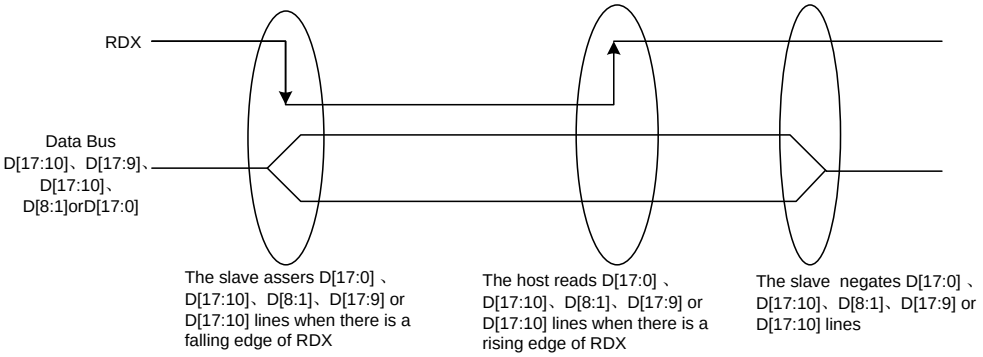


4.1.7. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

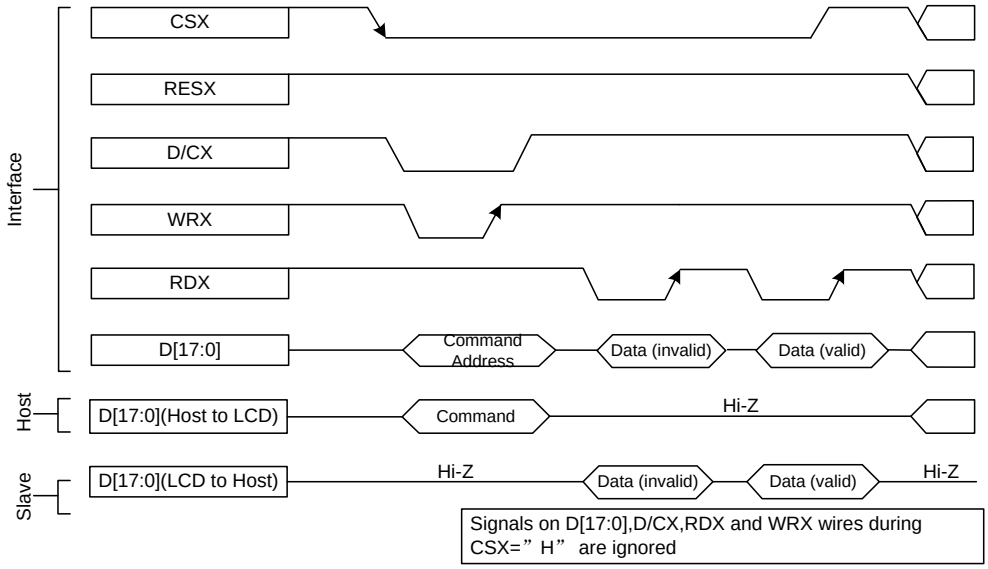
The following figure shows the read cycle for the 8080-II MCU interface.

Figure 8.



Note: RDX is an unsynchronized signal (It can be stopped).

Figure 9.



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

4.1.8. Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

Table 8.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	D/CX	SCL	Function
1	1	0	1	3-line serial interface	“L”	-	↑	Read/Write command, parameter or display data.
1	1	1	1	4-line serial interface	“L”	"H/L"	↑	Read/Write command, parameter or display data.
1	0	0	1	3-line serial interface	“L”	-	↑	Read/Write command, parameter or display data.
1	0	1	1	4-line serial interface	“L”	"H/L"	↑	Read/Write command, parameter or display data.

GC9A01 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and GC9A01. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO). The 4-line serial mode consists of the Data/ Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO) for data transmission. The data bus (D [17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

4.1.9. Write Cycle Sequence

The write mode of the interface means that host writes commands or data to GC9A01. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is “low”, the transmission byte is interpreted as a command byte. If the D/CX bit is “high”, the transmission byte is stored as the display data RAM(Memory write command),or command register as parameter.

Any instruction can be sent in any order to GC9A01 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

Figure 10.

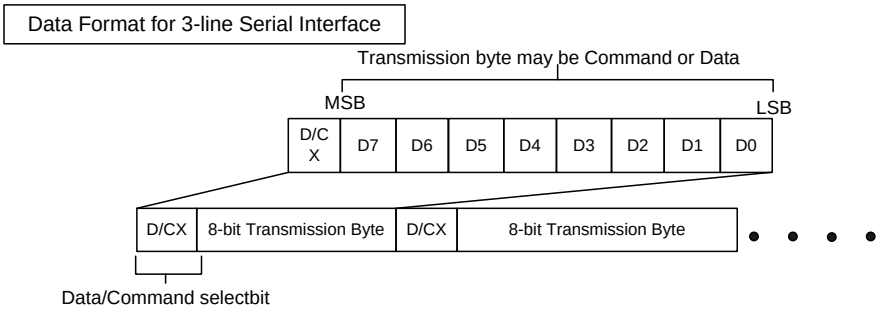
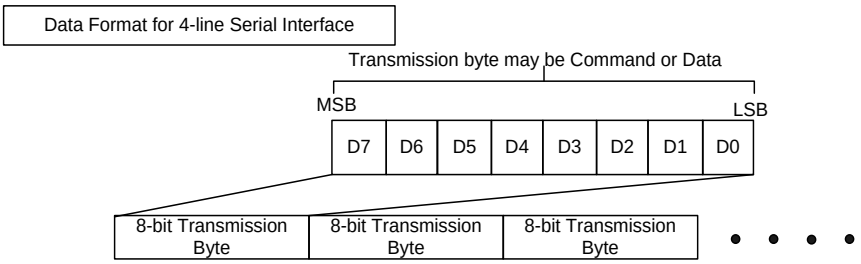


Figure11.



Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by GC9A01 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

Figure 12.

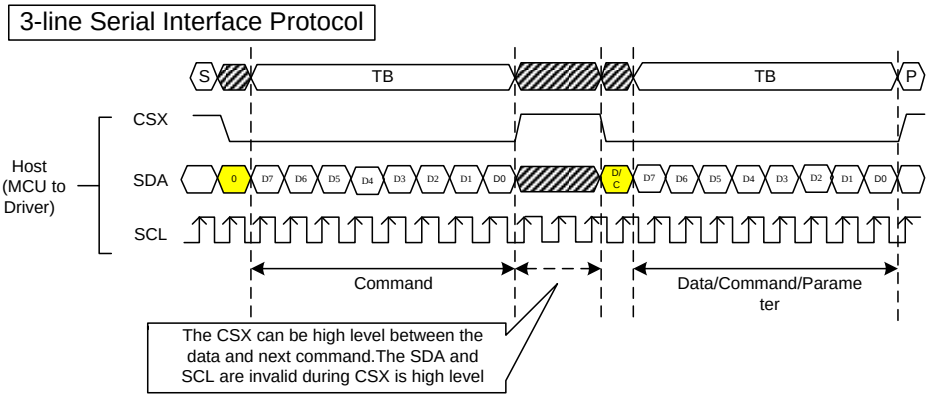
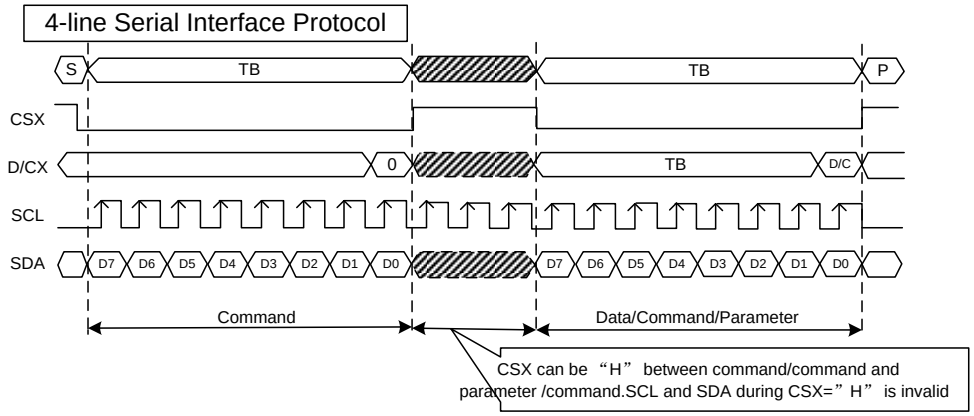


Figure 13.



4.1.10. Read Cycle Sequence

The read mode of interface means that the host reads register's parameter from GC9A01. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. GC9A01 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

Figure 14.

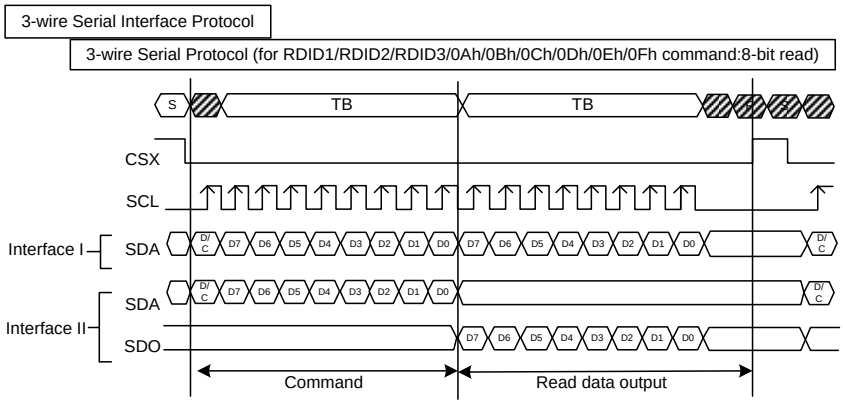


Figure 15.

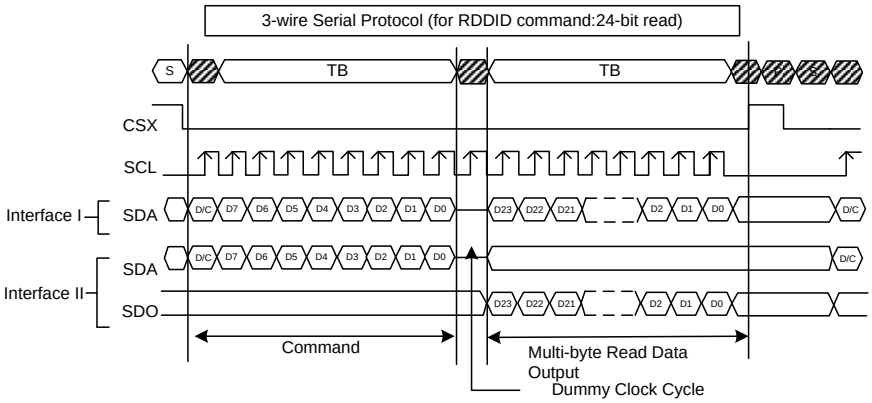


Figure 16.

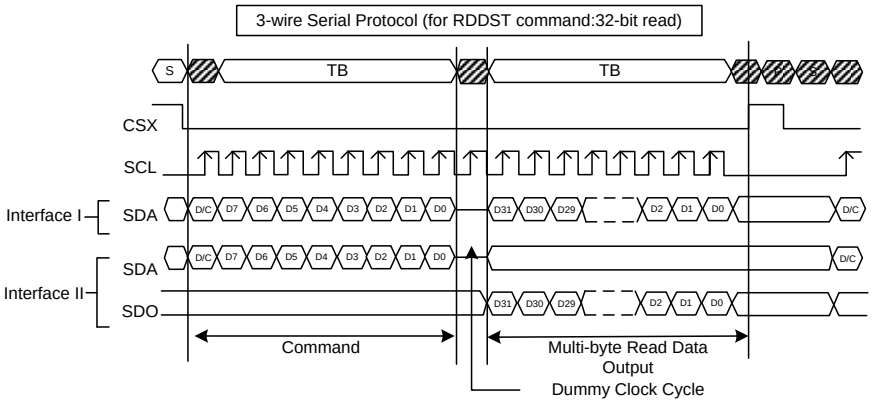


Figure 17.

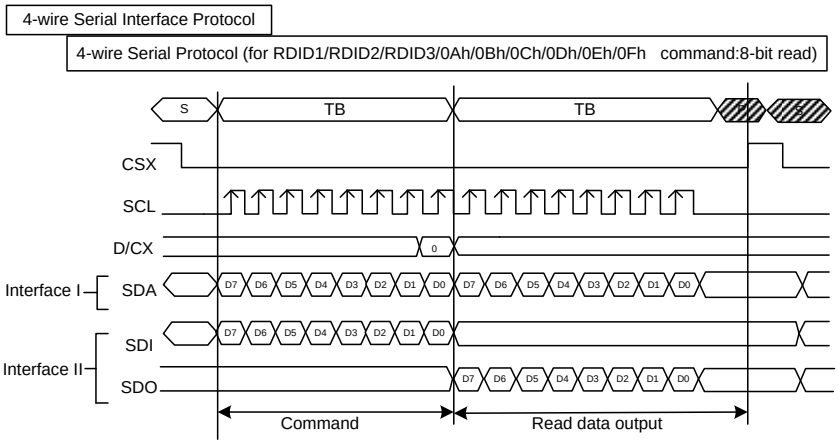


Figure 18.

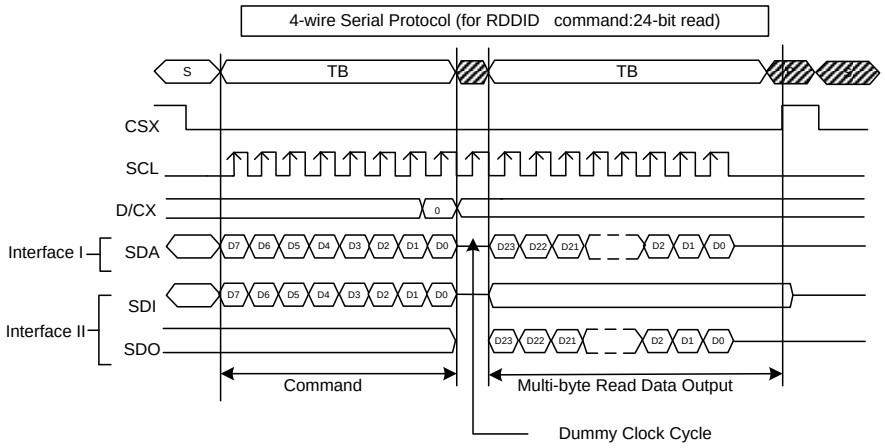
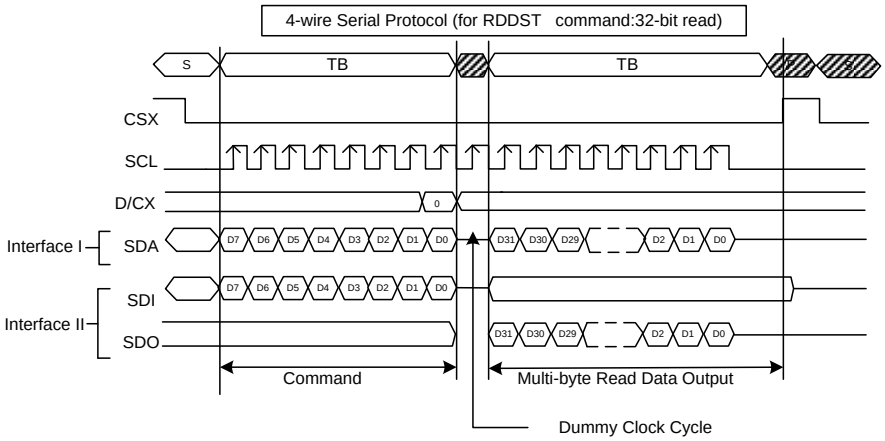


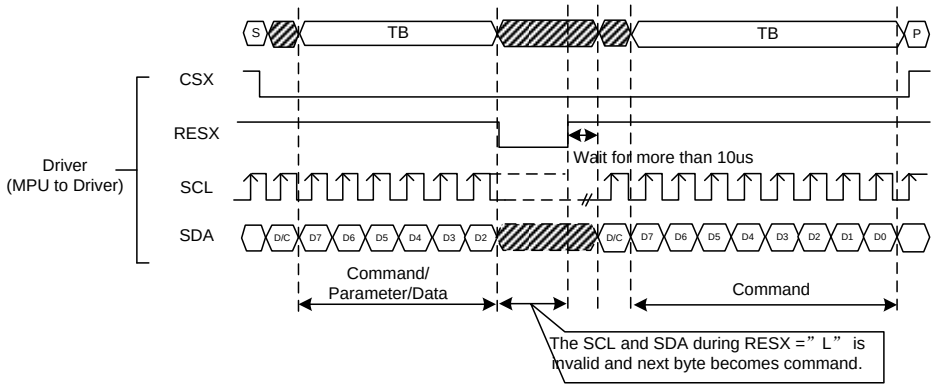
Figure 19.



4.1.11. Data Transfer Break and Recovery

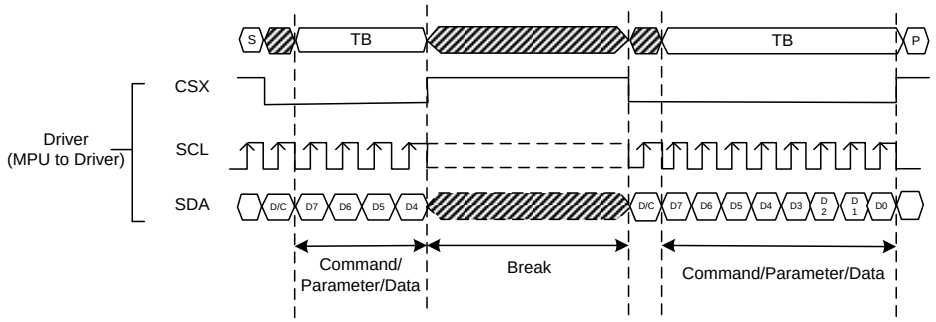
If there is a break in data transmission by RESX pulse, while transferring a command or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.

Figure 20.



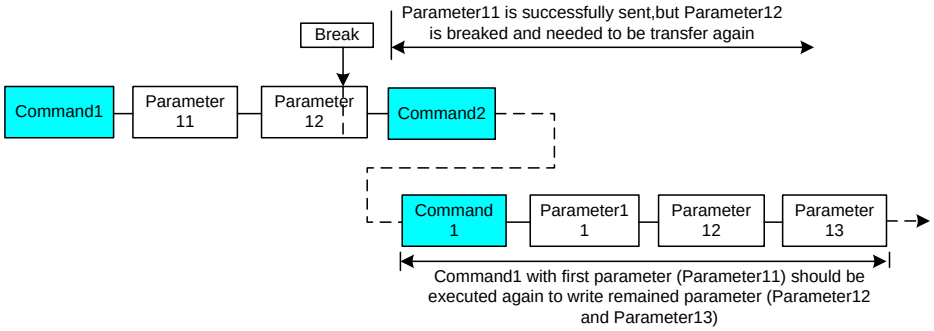
If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.

Figure 21.



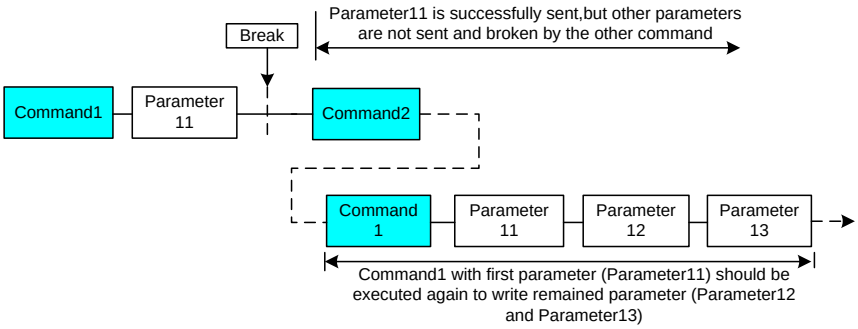
If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

Figure 22.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.

Figure 23.

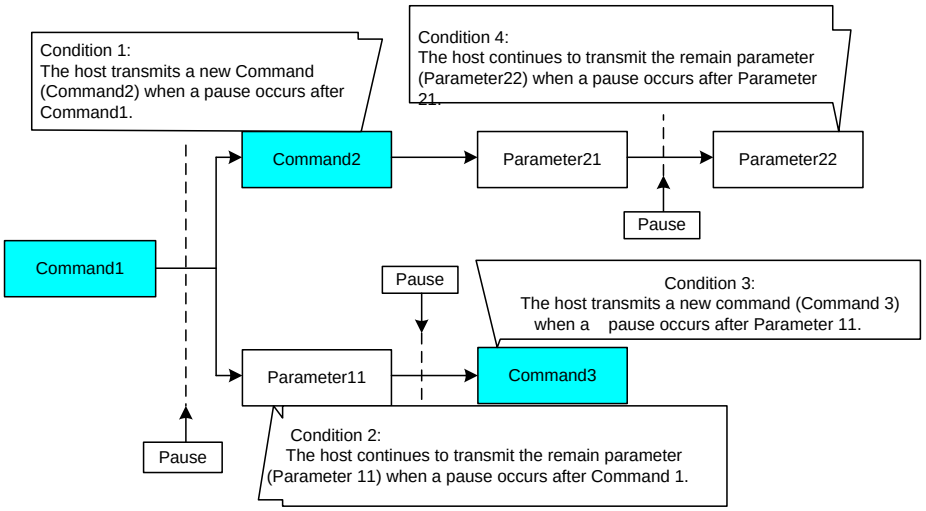


4.1.12. Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then GC9A01 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters(if appropriate) or a new command when the chip select pin is next enabled as shown below.

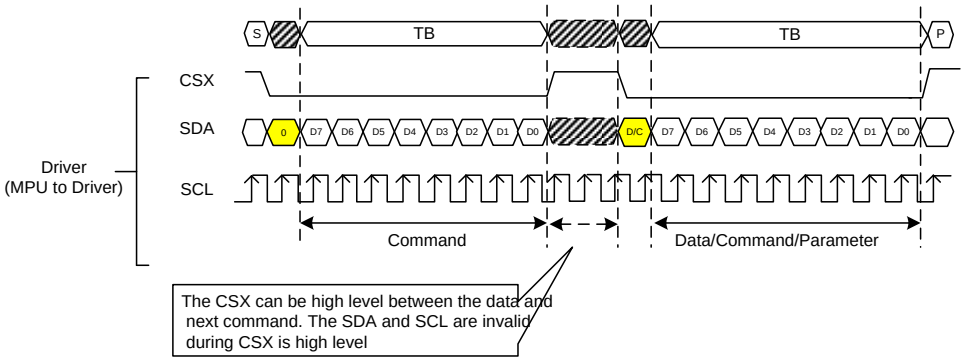
This applies to the following 4 conditions:
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

Figure 24.



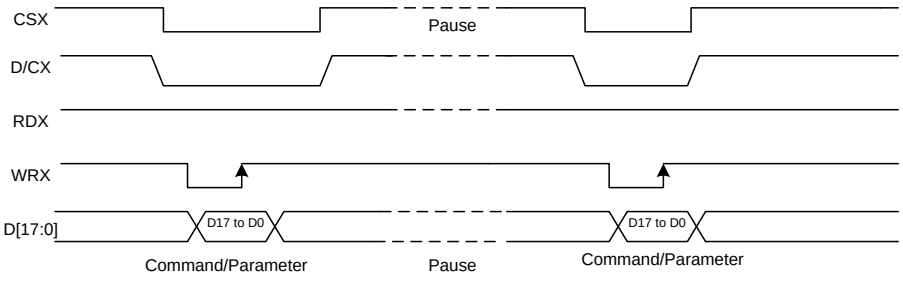
4.1.13. Serial Interface Pause (3_wire)

Figure 25.



4.1.14. Parallel Interface Pause

Figure 26.



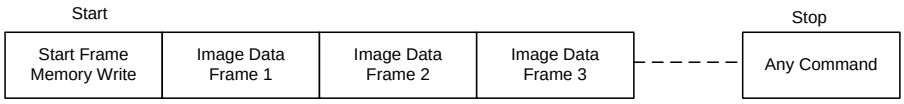
4.1.15. Data Transfer Mode

GC9A01 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

4.1.16. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.

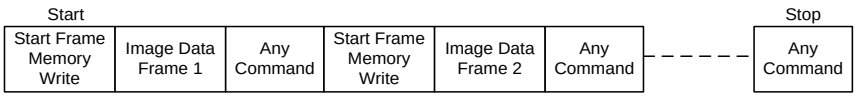
Figure 27.



4.1.17. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.

Figure 28.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.
Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

4.2. RGB Interface

4.2.1. RGB Interface Selection

GC9A01 has two kinds of RGB interface and these interfaces can be selected by RCM [1:0] bits. When RCM [1:0] bits are set to “10”, the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DE, D [17:0] pins; when RCM [1:0] bits are set to “11”, the SYNC mode is selected which utilizes which utilizes VSYNC, HSYNC,DOTCLK, D [17:0] pins. Using RGB interface must selection serial interface.
GC9A01 supports several pixel formats that can be selected by RIM bit of F6h command. The selection of a given interfaces is done by setting RCM [1:0] as show in the following table.

Table 9

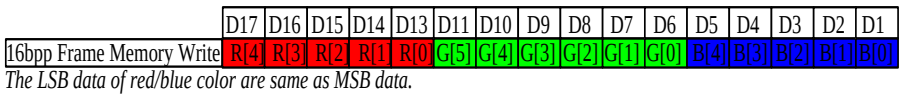
RCM[1:0]		RIM	DPI[1:0]			RGB interface Mode	RGB Mode	Used Pins
1	0	0	1	1	0	18-bit RGB interface (262K colors)	DE Mode Valid data is determined by the DE signal	VSYNC,HSYNC,DE,DOTCLK, D[17:0]
1	0	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC,HSYNC,DE,DOTCLK, D[17:13] & D[11:1]
1	0	1	-			6-bit RGB interface (262K colors)		VSYNC,HSYNC,DE,DOTCLK, D[5:0]
1	1	0	1	1	0	18-bit RGB interface (262K colors)	SYNC Mode In SYNC mode, DE signal is ignored;blanking porch is determined by B5h command	VSYNC,HSYNC,DOTCLK, D[17:0]
1	1	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC,HSYNC,DOTCLK, D[17:13] & D[11:1]
1	1	1	-			6-bit RGB interface (262K colors)		VSYNC,HSYNC,DOTCLK, D[5:0]

18-bit data bus interface (D[17:0] is used) , RIM=0

Figure 29.

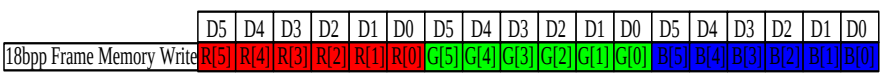
16-bit data bus interface (D[17:13] & D[11:1] is used) , DPI[2:0] = 101, and RIM=0

Figure 30.



6-bit data bus interface (D[5:0] is used) , RIM=1

Figure 31.



Pixel clock (DOTCLK) is running all the time without stopping and used to enter VSYNC, HSYNC, DE and

D[17:0] states when there is a rising edge of the DOTCLK. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

In DE mode, Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. D [17:0] are used to tell what is the information of the image that is transferred on the display (When DE= ’0’ (low) and there is a rising edge of DOTCLK). D [17:0] can be ‘0’ (low) or ‘1’ (high). These lines are read by a rising edge of the DOTCLK signal. In SYNC mode, the valid display data in inputted in pixel unit via D [17:0] according to HFP/HBP settings of HSYNC signal and VFP/VBP setting of VSYNC. In both RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.

Figure32.

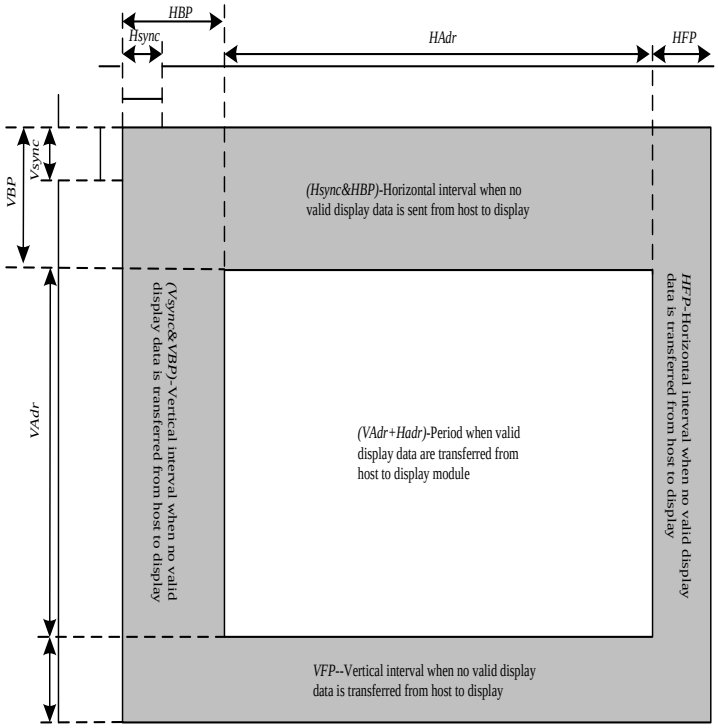


Table 10.

Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	240	-	Line
Vertical Front Porch	VFP		3	4	-	Line

Notes:

1. Vertical period (one frame) shall be equal to the sum of VBP + VAdr + VFP.

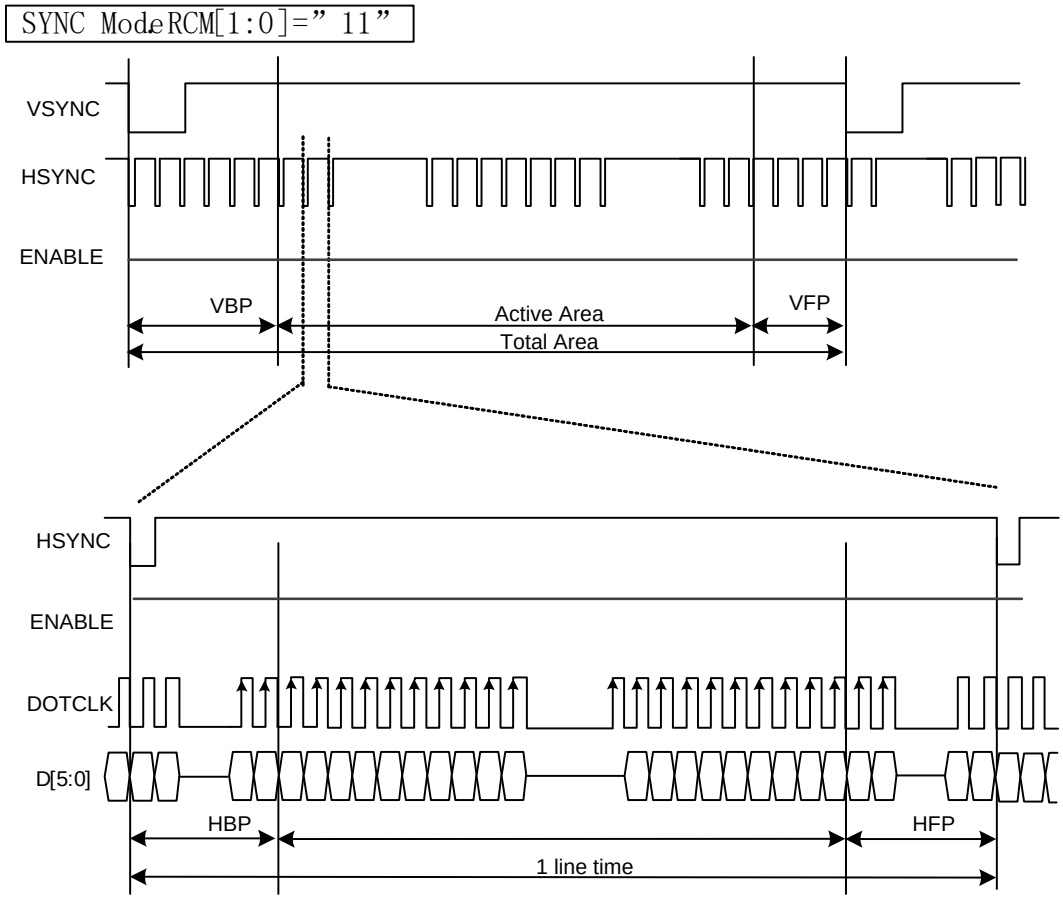
2. Horizontal period (one line) shall be equal to the sum of HBP + HAdr + HFP.

3. Control signals Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

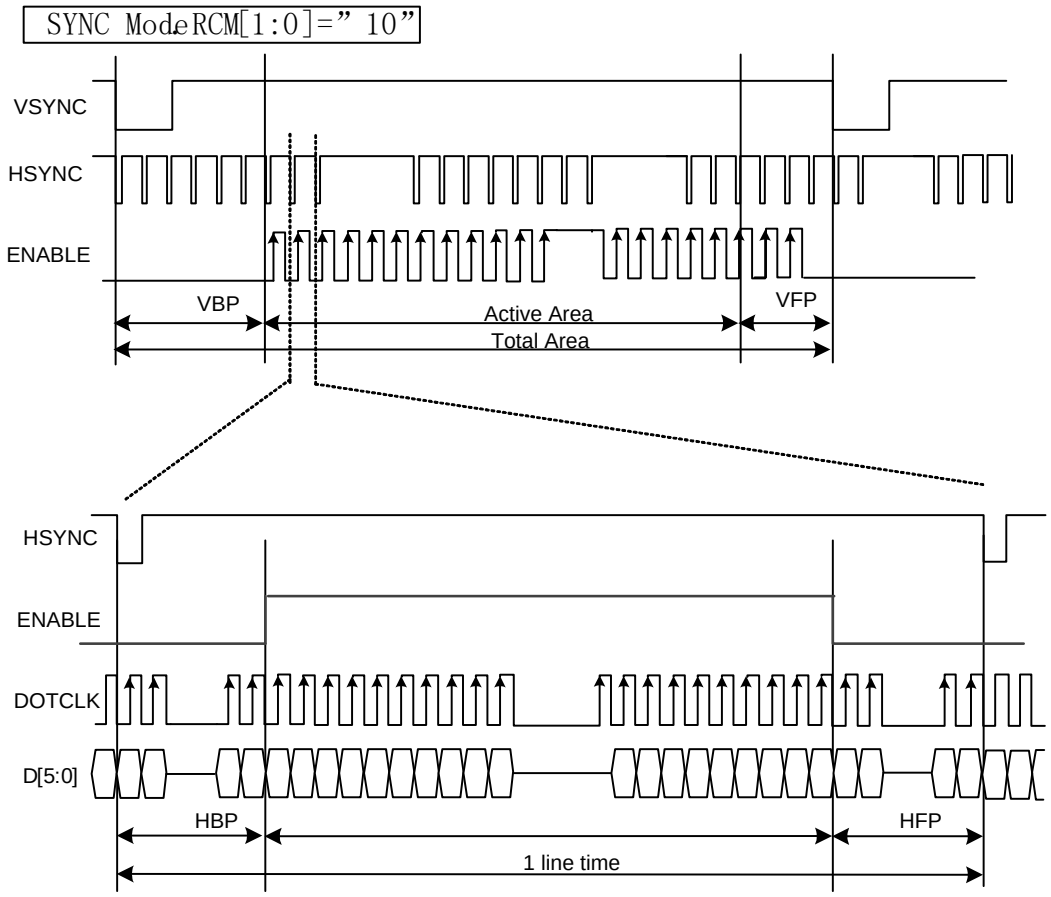
4.2.2. RGB Interface Timing

The timing chart of 18/16-bit RGB interface mode1 and mode 2 is shown as below.

Figure33.



Mode1 RGB SYNC mode



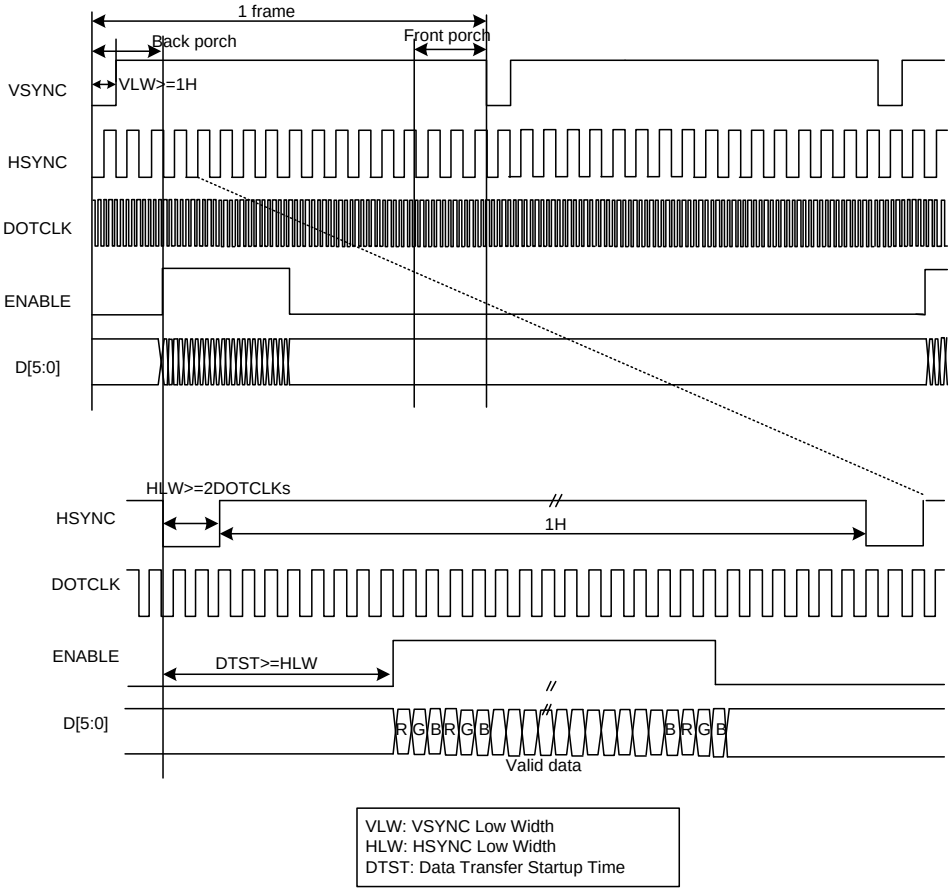
Mode2 RGB SYNC+DE mode

Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

The timing chart of 6-bit RGB interface mode is shown as below:

Figure34.



Note 1: 6-bit RGB interface mode only used in the DE interface.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

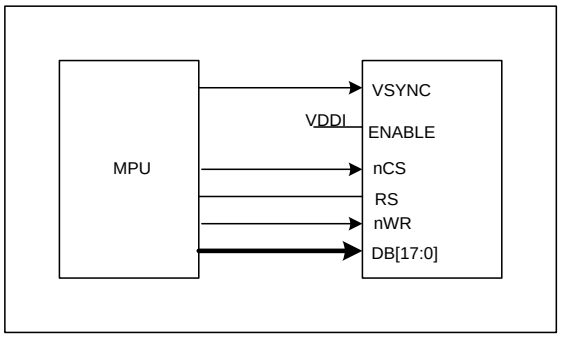
Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.

Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and DE to 3 multiples of DOTCLK.

4.3. VSYNC Interface

GC9A01 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the 8080-Ⅰ/8080-Ⅱ system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = “10” and RM = “0”.

Figure35.



Note 1:In the VSYNC mode,the pin ENABLE should connect to VDDI.

In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.

Figure36.

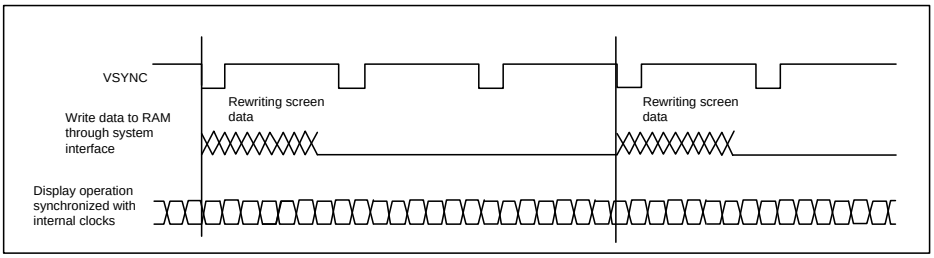
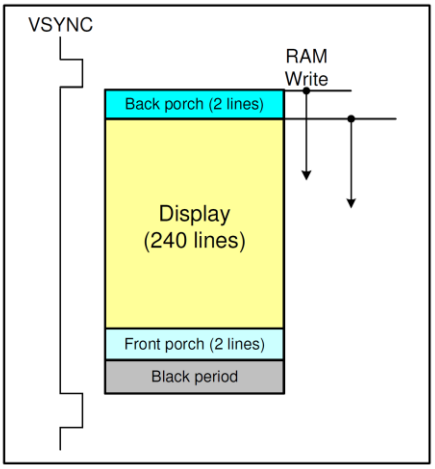


Figure37.



Notes in using the VSYNC interface

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into

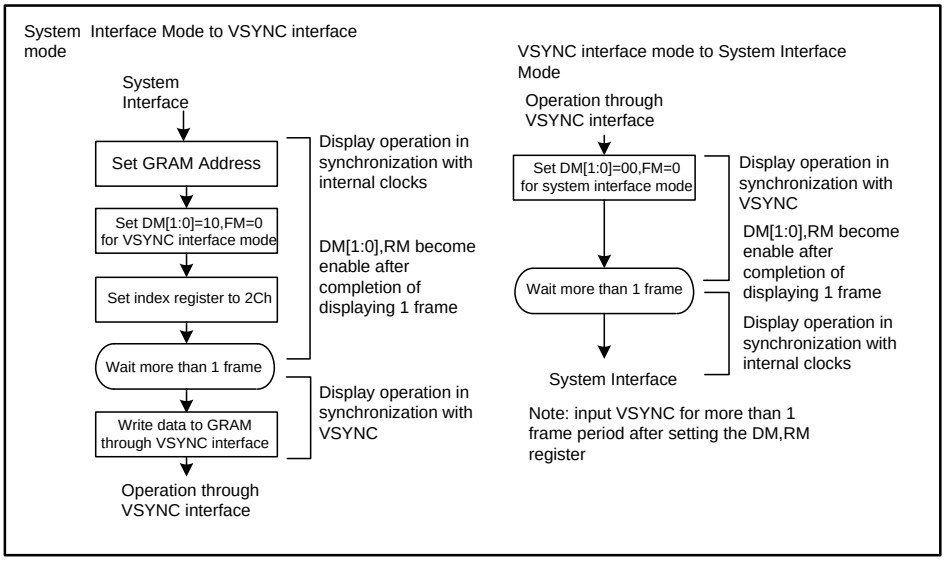
consideration.

2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.

3. When switching from the internal clock operation mode (DM[1:0] = “00”) to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.

4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.

Figure38.



4.4. Display Data RAM (DDRAM)

GC9A01 has an integrated 240x240x18-bit graphic type static RAM. This 129,600 -bytes memory allows storing a 240xRGBx240 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.

4.5. Display Data Format

GC9A01 supplies 18-/16-/9-/8-bit parallel MCU interface with 8080-Ⅰ/8080-Ⅱ series, 3-/4-line serial interface and 6-/16-18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters RCM[1:0].

4.5.1. 3-line Serial Interface

The 3-line/9-bit serial bus interface of GC9A01 can be used by setting external pin as IM [3:0] to “1101” for serial interface. The shown figure is the example of 3-line SPI interface.

Figure39.

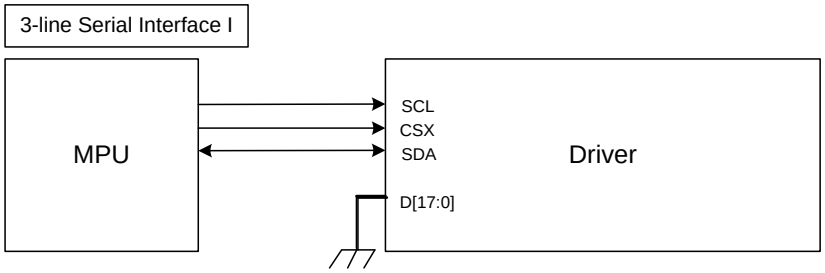
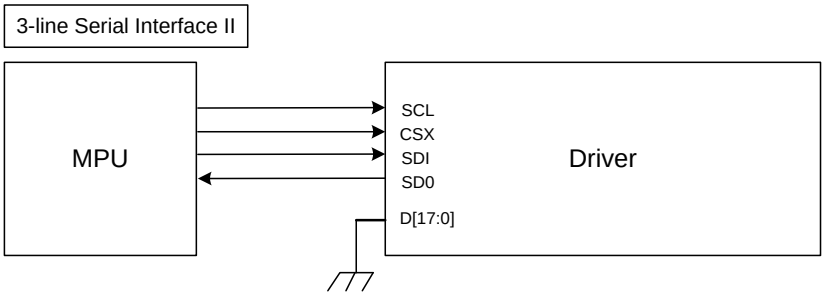


Figure40.



In 3-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

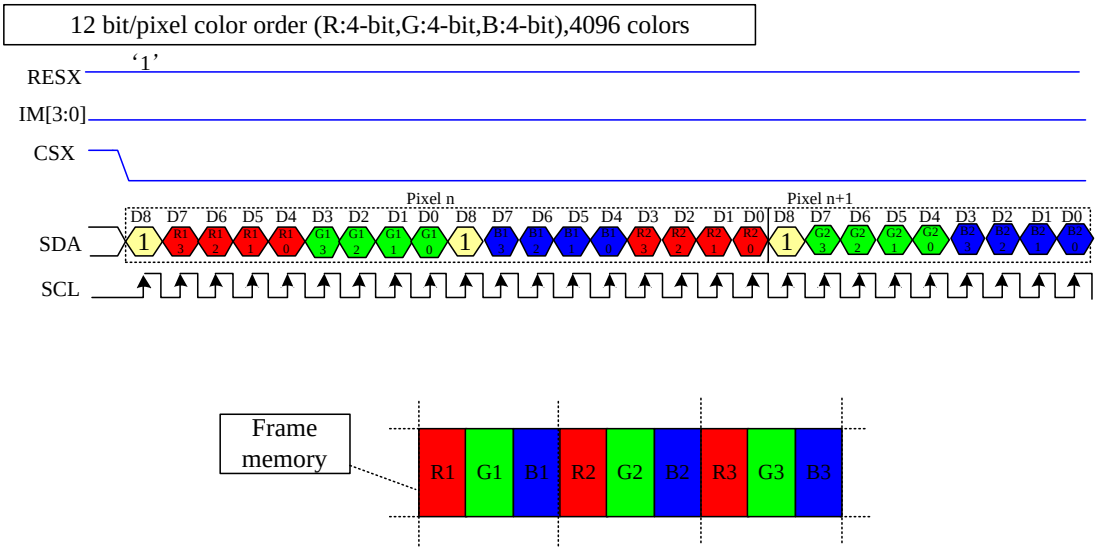
-4k colors, RGB 4, 4, 4 -bits input.

-65k colors, RGB 5, 6, 5 -bits input

-262k colors, RGB 6, 6, 6 -bits input.

1)4K-Colors:12-bit/pixel(RGB 4, 4, 4 -bits input).

Figure41.



Note 1: The pixel data with 12-bit color depth information.

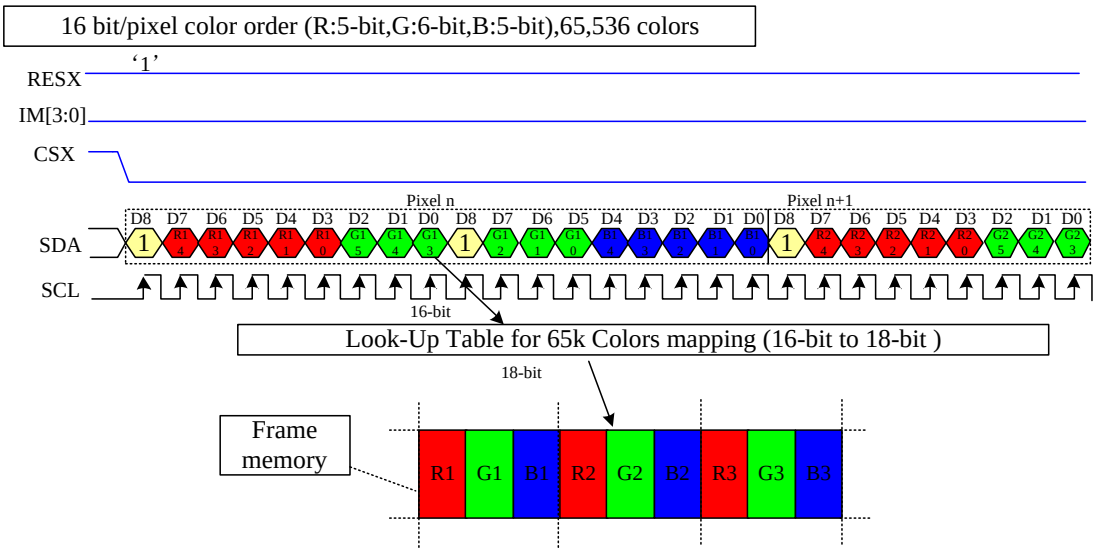
Note 2: The most significant bits are: Rx3, Gx3 and Bx3.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

2)65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

Figure41.



Note 1: The pixel data with 16-bit color depth information.

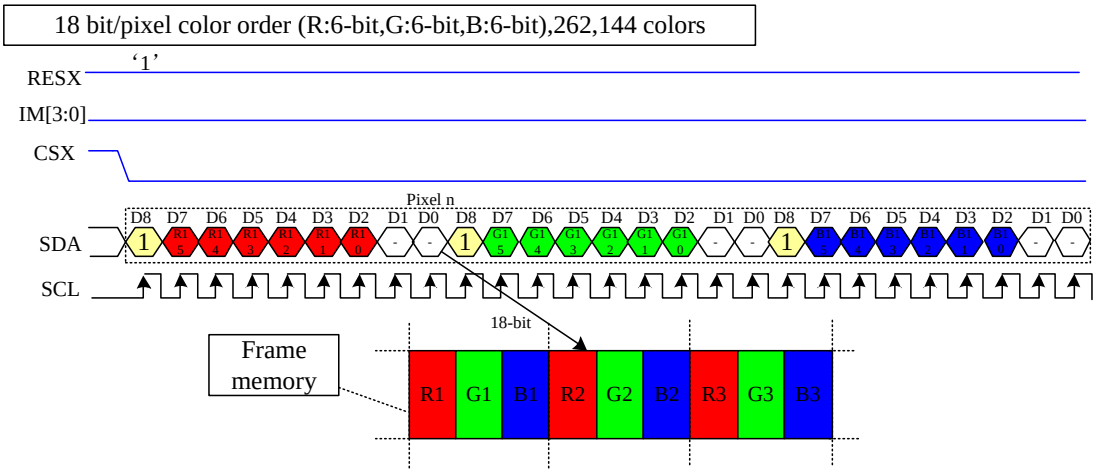
Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

3)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

Figure42.



Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care - Can be set "0" or "1".

4.5.2. 4-line Serial Interface

The 4-line/8-bit serial bus interface of GC9A01 can be used by setting external pin as IM [3:0] to “1111” for serial interface . The shown figure is the example of 4-line SPI interface.

Figure43.

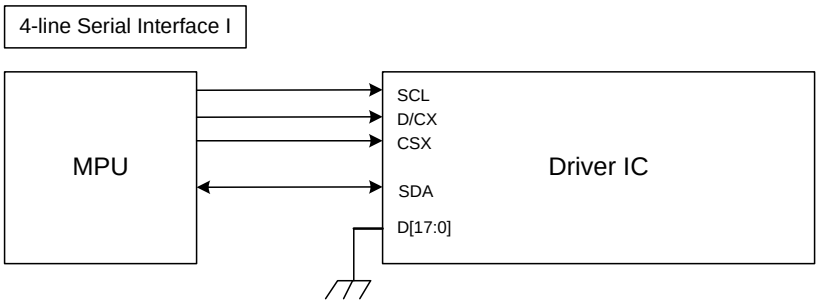
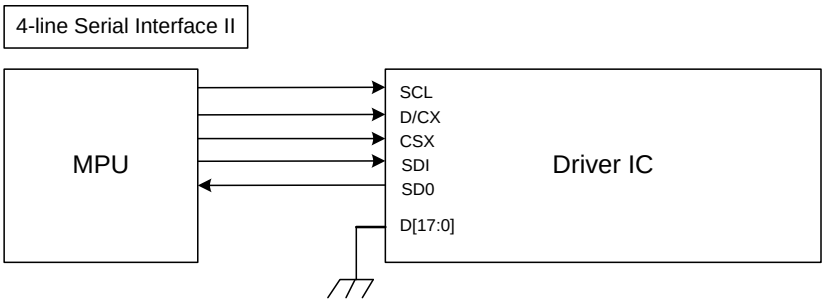


Figure44.



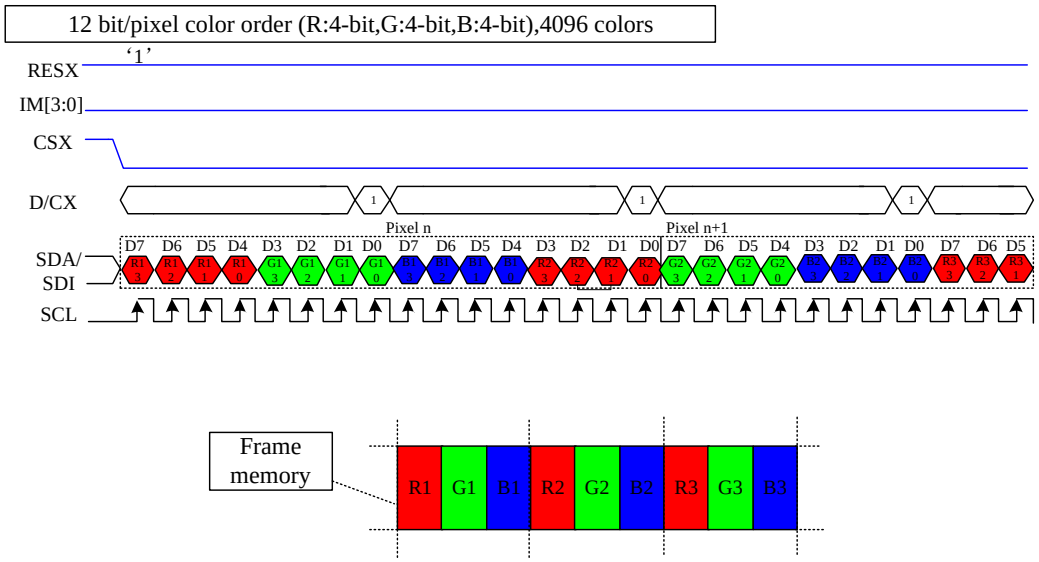
In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-4k colors, RGB 4, 4, 4 -bits input.

-65k colors, RGB 5, 6, 5 -bits input.

-262k colors, RGB 6, 6, 6 -bits input.

Figure44.



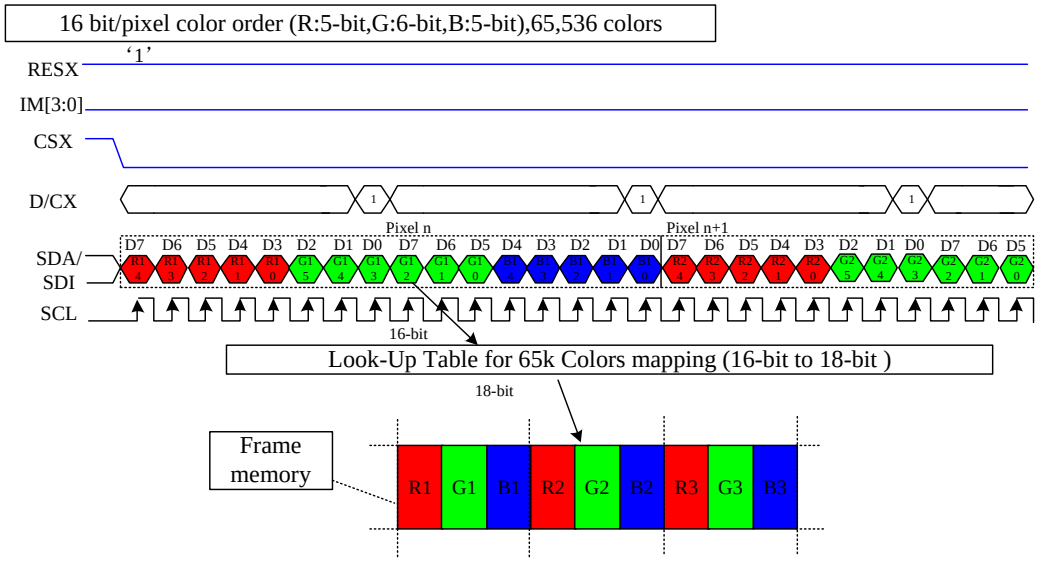
Note 1: The pixel data with 12-bit color depth information.

Note 2: The most significant bits are: Rx3, Gx3 and Bx3.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

Figure45.



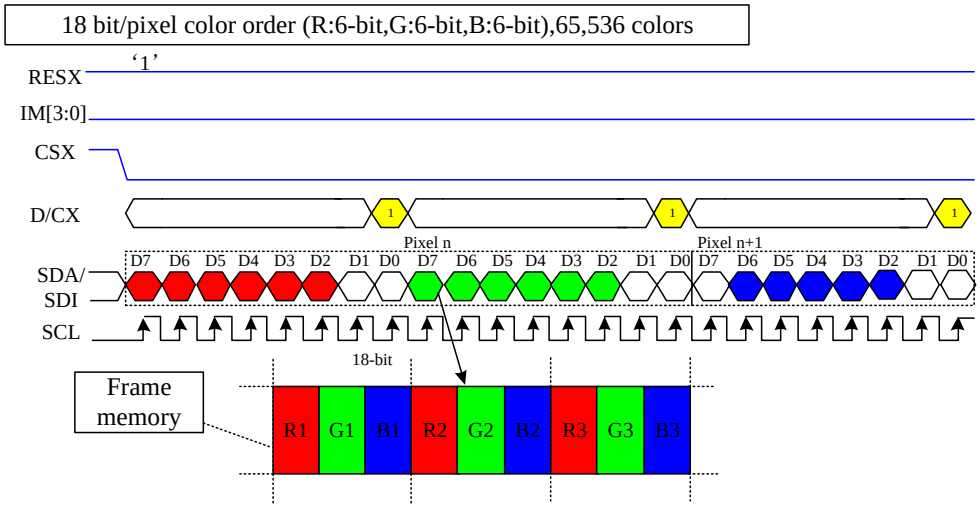
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

Figure46.



Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

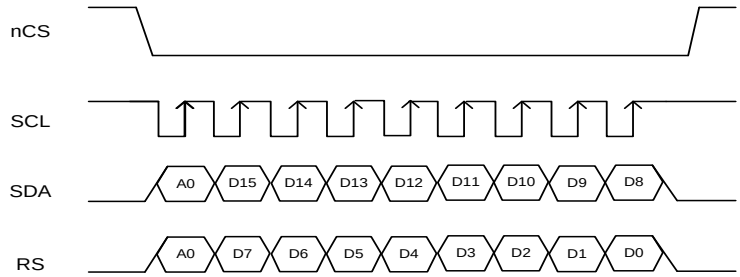
4.5.3. 2-data-line mode

This mode is active when 2data_en (E9h[3]) set to “1” in 3-wire. Only frame pixle data write transitions are sent in 2-data-line mode, register write/read is still sent in 3-wire.

The chip-select nCS (active low) enables and disables the serial interface. SCL is the serial data clock. SDA and DCX are serial data lines.

Serial data must be input to SDA in the sequence A0, D15 to D10 and DCX in the sequence A0, D7 to D0. The GC9A01 reads the data at the rising edge of SCL signal. The first bit of serial data A0 is data/command flag. It must be set to "1", D15 to D0 bits are display RAM data.

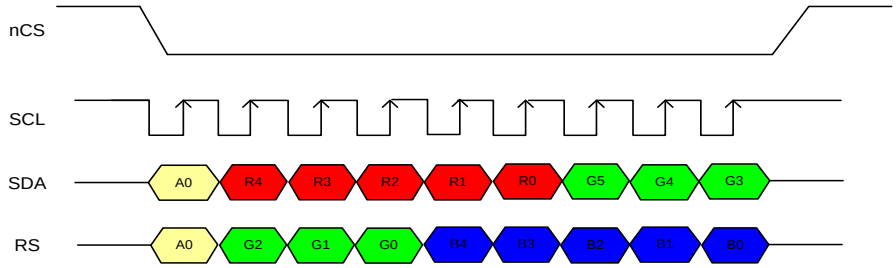
Figure47.



Five data formats are supported in 2-data-line mode, which is indicated by 2data_mdt (E9h[2:0]) .

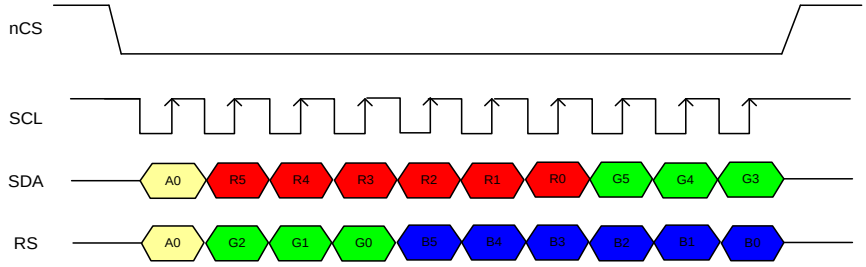
1)RGB565 1pixel/transition(65K color,2data_mdt[2:0]=’000’)

Figure48.



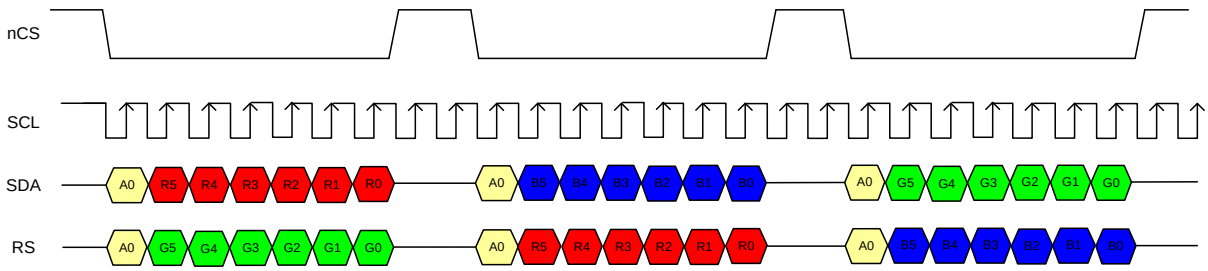
2)RGB666 1pixel/transition(262K color,2data_mdt[2:0]=’001’)

Figure49.



3)RGB666 2/3pixel/transition(262K color,2data_mdt[2:0]=’010’)

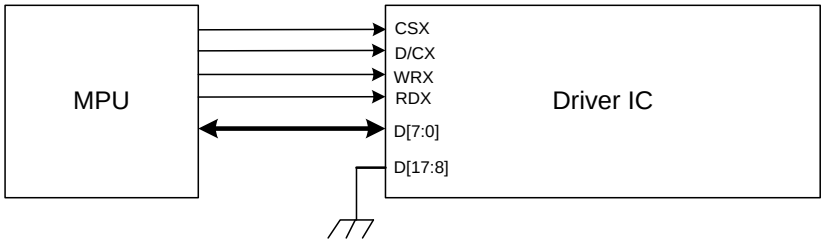
Figure50.


nCS
SCL
SDA
RS
A0 R5 R4 R3 R2 R1 R0
A0 B5 B4 B3 B2 B1 B0
A0 G5 G4 G3 G2 G1 G0
A0 G5 G4 G3 G2 G1 G0
A0 R5 R4 R3 R2 R1 R0
A0 B5 B4 B3 B2 B1 B0

4.5.4. 8-bit Parallel MCU Interface

The 8080-Ⅰsystem 8-bit parallel bus interface of GC9A01 can be used by setting external pin as IM [3:0] to“0100”.The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.

Figure53.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to “101”.

Table 11.

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D7	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

2) 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

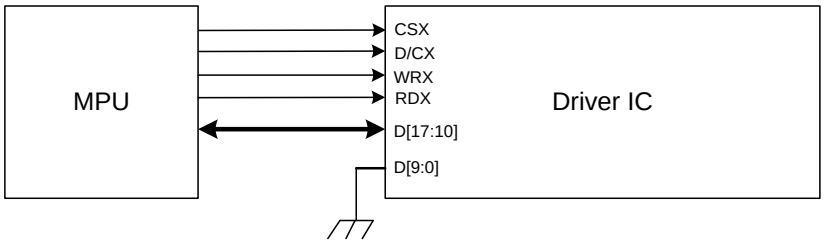
One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Table12.

Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D1	C1				…			
D0	C0				…			

The 8080-II system 8-bit parallel bus interface of GC9A01 can be used by settings as IM [3:0] =”0000”. The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.

Figure54.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to “101”.

Table13.

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D16	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D15	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D14	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D13	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D12	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D11	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D10	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

2) 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to“110”.

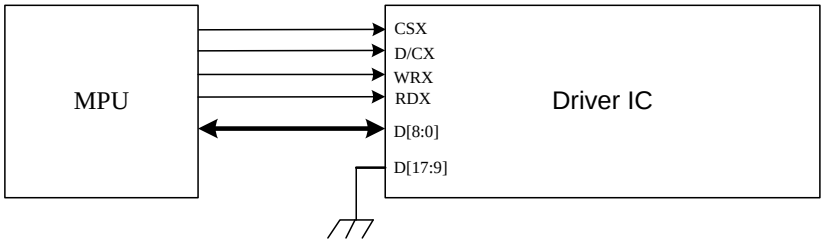
Table14.

Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D17	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D16	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D15	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D14	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D13	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D12	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D11	C1				…			
D10	C0				…			

4.5.5. 9-bit Parallel MCU Interface

The 8080-I system 9-bit parallel bus interface of GC9A01 can be selected by setting hardware pin IM [3:0] to "0101". The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.

Figure55.



1)262K-Colors,:18-bit/pixel(RGB 6, 6, 6 -bits input).

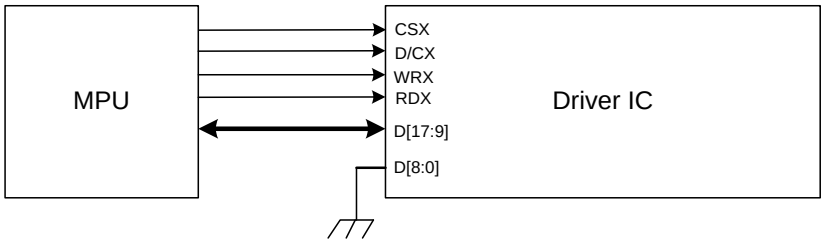
There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to "110".

Table15.

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D8		0R5	0G2	1R5	1G2	…	238R5	238G2	239R5	239G2
D7	C7	0R4	0G1	1R4	1G1	…	238R4	238G1	239R4	239G1
D6	C6	0R3	0G0	1R3	1G0	…	238R3	238G0	239R3	239G0
D5	C5	0R2	0B5	1R2	1B5	…	238R2	238B5	239R2	239B5
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

The 8080- Ⅱ system 9-bit parallel bus interface of GC9A01 can be selected by setting hardware pin IM [3:0] to “0001”. The following shown figure is the example of interface with 8080- MCU system interface.

Figure56.



1)262K-Colors,:18-bit/pixel(RGB 6, 6, 6 -bits input).

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to “110”.

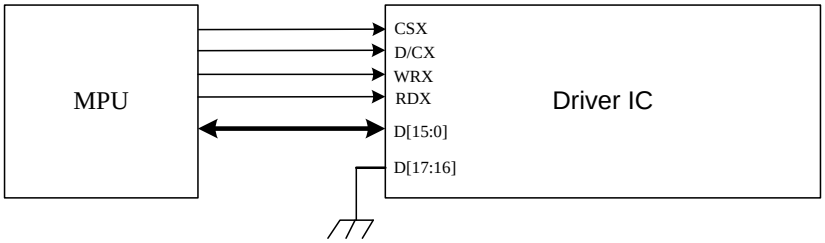
Table16.

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7	0R5	0G2	1R5	1G2	…	238R5	238G2	239R5	239G2
D16	C6	0R4	0G1	1R4	1G1	…	238R4	238G1	239R4	239G1
D15	C5	0R3	0G0	1R3	1G0	…	238R3	238G0	239R3	239G0
D14	C4	0R2	0B5	1R2	1B5	…	238R2	238B5	239R2	239B5
D13	C3	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D12	C2	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D11	C1	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D10	C0	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D9		0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

4.5.6. 16-bit Parallel MCU Interface

The 8080-Ⅰsystem 16-bit parallel bus interface of GC9A01 can be selected by setting hardware pin IM[3:0] to "0110".The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.

Figure57.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1)65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Table17.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8		0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "110".

1)MDT[1:0]="00"

Table18.

Count	0	1	2	3	…	358	359	360
D/CX	0	1	1	1	…	1	1	1
D15		0R5	0B5	1G5	…	238R5	238B5	239G5
D14		0R4	0B4	1G4	…	238R4	238B4	239G4
D13		0R3	0B3	1G3	…	238R3	238B3	239G3
D12		0R2	0B2	1G2	…	238R2	238B2	239G2
D11		0R1	0B1	1G1	…	238R1	238B1	239G1
D10		0R0	0B0	1G0	…	238R0	238B0	239G0
D9								
D8								
D7	C7	0G5	1R5	1B5	…	238G5	239R5	239B5
D6	C6	0G4	1R4	1B4	…	238G4	239R4	239B4
D5	C5	0G3	1R3	1B3	…	238G3	239R3	239B3
D4	C4	0G2	1R2	1B2	…	238G2	239R2	239B2
D3	C3	0G1	1R1	1B1	…	238G1	239R1	239B1
D2	C2	0G0	1R0	1B0	…	238G0	239R0	239B0
D1	C1							
D0	C0							

2)MDT[1:0]=“01”

Table19.

Count	0	1	2	3		…	477	478	479	480
D/CX	0	1	1	1		…	1	1	1	1
D15		0R5	0B5	1R5	1B5	…	238R5	238B5	239R5	239B5
D14		0R4	0B4	1R4	1B4	…	238R4	238B4	239R4	239B4
D13		0R3	0B3	1R3	1B3	…	238R3	238B3	239R3	239B3
D12		0R2	0B2	1R2	1B2	…	238R2	238B2	239R2	239B2
D11		0R1	0B1	1R1	1B1	…	238R1	238B1	239R1	239B1
D10		0R0	0B0	1R0	1B0	…	238R0	238B0	239R0	239B0
D9						…				
D8						…				
D7	C7	0G5		1G5		…	238G5		239G5	
D6	C6	0G4		1G4		…	238G4		239G4	
D5	C5	0G3		1G3		…	238G3		239G3	
D4	C4	0G2		1G2		…	238G2		239G2	
D3	C3	0G1		1G1		…	238G1		239G1	
D2	C2	0G0		1G0		…	238G0		239G0	
D1	C1					…				
D0	C0					…				

3)MDT[1:0]="10"

Table20.

Count	0	1	2	3		…	477	478	479	480
D/CX	0	1	1	1		…	1	1	1	1
D15		0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D14		0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0
D13		0R3		1R3		…	238R3		239R3	
D12		0R2		1R2		…	238R2		239R2	
D11		0R1		1R1		…	238R1		239R1	
D10		0R0		1R0		…	238R0		239R0	
D9		0G5		1G5		…	238G5		239G5	
D8		0G4		1G4		…	238G4		239G4	
D7	C7	0G3		1G3		…	238G3		239G3	
D6	C6	0G2		1G2		…	238G2		239G2	
D5	C5	0G1		1G1		…	238G1		239G1	
D4	C4	0G0		1G0		…	238G0		239G0	
D3	C3	0B5		1B5		…	238B5		239B5	
D2	C2	0B4		1B4		…	238B4		239B4	
D1	C1	0B3		1B3		…	238B3		239B3	
D0	C0	0B2		1B2		…	238B2		239B2	

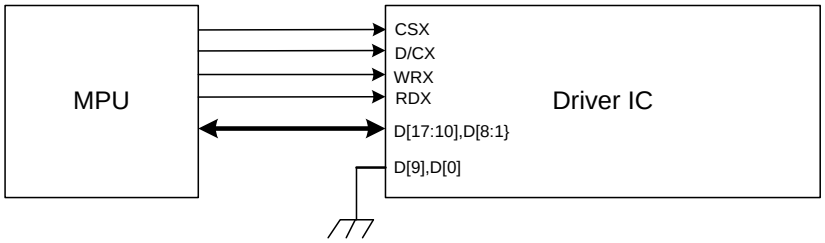
4)MDT[1:0]="11"

Table21.

Count	0	1	2	3		…	477	478	479	480
D/CX	0	1	1	1		…	1	1	1	1
D15			0R3		1R3	…		238R3		239R3
D14			0R2		1R2	…		238R2		239R2
D13			0R1		1R1	…		238R1		239R1
D12			0R0		1R0	…		238R0		239R0
D11			0G5		1G5	…		238G5		239G5
D10			0G4		1G4	…		238G4		239G4
D9			0G3		1G3	…		238G3		239G3
D8			0G2		1G2	…		238G2		239G2
D7	C7		0G1		1G1	…		238G1		239G1
D6	C6		0G0		1G0	…		238G0		239G0
D5	C5		0B5		1B5	…		238B5		239B5
D4	C4		0B4		1B4	…		238B4		239B4
D3	C3		0B3		1B3	…		238B3		239B3
D2	C2		0B2		1B2	…		238B2		239B2
D1	C1	0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D0	C0	0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0

The 8080-II system 16-bit parallel bus interface of GC9A01 can be selected by settings IM [3:0] ="0010". The following shown figure is the example of interface with 8080- MCU system interface.

Figure58.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “101”.

Table22.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17		0R4	1R4	2R4	…	237R4	238R4	239R4
D16		0R3	1R3	2R3	…	237R3	238R3	239R3
D15		0R2	1R2	2R2	…	237R2	238R2	239R2
D14		0R1	1R1	2R1	…	237R1	238R1	239R1
D13		0R0	1R0	2R0	…	237R0	238R0	239R0
D12		0G5	1G5	2G5	…	237G5	238G5	239G5
D11		0G4	1G4	2G4	…	237G4	238G4	239G4
D10		0G3	1G3	2G3	…	237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D4	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D3	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D2	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D1	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to “110”.

1)MDT[1:0]=00

Table23.

Count	0	1	2	3	…	358	359	360
D/CX	0	1	1	1	…	1	1	1
D17		0R5	0B5	1G5	…	238R5	238B5	239G5
D16		0R4	0B4	1G4	…	238R4	238B4	239G4
D15		0R3	0B3	1G3	…	238R3	238B3	239G3
D14		0R2	0B2	1G2	…	238R2	238B2	239G2

D13		0R1	0B1	1G1	…	238R1	238B1	239G1
D12		0R0	0B0	1G0	…	238R0	238B0	239G0
D11								
D10								
D8	C7	0G5	1R5	1B5	…	238G5	239R5	239B5
D7	C6	0G4	1R4	1B4	…	238G4	239R4	239B4
D6	C5	0G3	1R3	1B3	…	238G3	239R3	239B3
D5	C4	0G2	1R2	1B2	…	238G2	239R2	239B2
D4	C3	0G1	1R1	1B1	…	238G1	239R1	239B1
D3	C2	0G0	1R0	1B0	…	238G0	239R0	239B0
D2	C1							
D1	C0							

2)MDT[1:0]=01

Table24.

Count	0	1	2	3		…	477	478	479	480
D/CX	0	1	1	1		…	1	1	1	1
D17		0R5	0B5	1R5	1B5	…	238R5	238B5	239R5	239B5
D16		0R4	0B4	1R4	1B4	…	238R4	238B4	239R4	239B4
D15		0R3	0B3	1R3	1B3	…	238R3	238B3	239R3	239B3
D14		0R2	0B2	1R2	1B2	…	238R2	238B2	239R2	239B2
D13		0R1	0B1	1R1	1B1	…	238R1	238B1	239R1	239B1
D12		0R0	0B0	1R0	1B0	…	238R0	238B0	239R0	239B0
D11						…				
D10						…				
D8	C7	0G5		1G5		…	238G5		239G5	
D7	C6	0G4		1G4		…	238G4		239G4	
D6	C5	0G3		1G3		…	238G3		239G3	
D5	C4	0G2		1G2		…	238G2		239G2	
D4	C3	0G1		1G1		…	238G1		239G1	
D3	C2	0G0		1G0		…	238G0		239G0	
D2	C1					…				
D1	C0					…				

3)MDT[1:0]=10

Table25.

Count	0	1	2	3		…	477	478	479	480
D/CX	0	1	1	1		…	1	1	1	1
D17		0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D16		0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0
D15		0R3		1R3		…	238R3		239R3	
D14		0R2		1R2		…	238R2		239R2	
D13		0R1		1R1		…	238R1		239R1	
D12		0R0		1R0		…	238R0		239R0	
D11		0G5		1G5		…	238G5		239G5	
D10		0G4		1G4		…	238G4		239G4	
D8	C7	0G3		1G3		…	238G3		239G3	
D7	C6	0G2		1G2		…	238G2		239G2	
D6	C5	0G1		1G1		…	238G1		239G1	
D5	C4	0G0		1G0		…	238G0		239G0	
D4	C3	0B5		1B5		…	238B5		239B5	
D3	C2	0B4		1B4		…	238B4		239B4	
D2	C1	0B3		1B3		…	238B3		239B3	
D1	C0	0B2		1B2		…	238B2		239B2	

4)MDT[1:0]=11

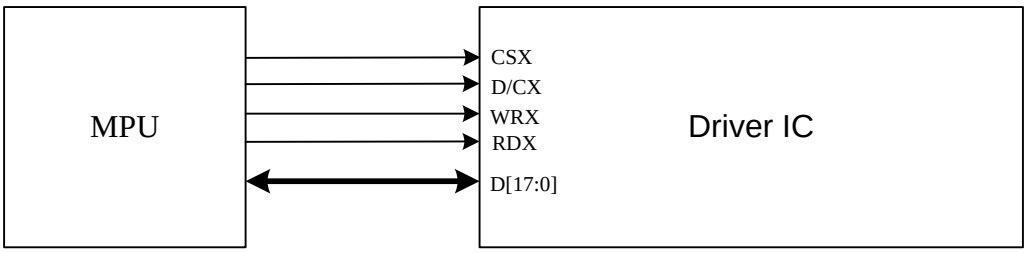
Table26.

Count	0	1	2	3		…	477	478	479	480
D/CX	0	1	1	1		…	1	1	1	1
D17			0R3		1R3	…		238R3		239R3
D16			0R2		1R2	…		238R2		239R2
D15			0R1		1R1	…		238R1		239R1
D14			0R0		1R0	…		238R0		239R0
D13			0G5		1G5	…		238G5		239G5
D12			0G4		1G4	…		238G4		239G4
D11			0G3		1G3	…		238G3		239G3
D10			0G2		1G2	…		238G2		239G2
D8	C7		0G1		1G1	…		238G1		239G1
D7	C6		0G0		1G0	…		238G0		239G0
D6	C5		0B5		1B5	…		238B5		239B5
D5	C4		0B4		1B4	…		238B4		239B4
D4	C3		0B3		1B3	…		238B3		239B3
D3	C2		0B2		1B2	…		238B2		239B2
D2	C1	0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D1	C0	0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0

4.5.7. 18-bit Parallel MCU Interface

The 8080-I system 18-bit parallel bus interface of GC9A01 can be selected by setting hardware pin IM[3:0] to "0111".The following shown figure is the example of interface with 8080-I MCU system interface.

Figure58.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Table27.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8		0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

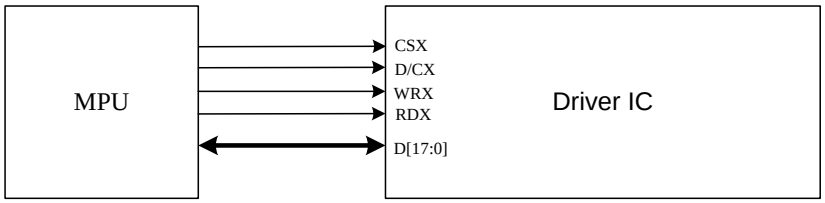
One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "110".

Table28.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17		0R5	1R5	2R5	…	237R5	238R5	239R5
D16		0R4	1R4	2R4	…	237R4	238R4	239R4
D15		0R3	1R3	2R3	…	237R3	238R3	239R3
D14		0R2	1R2	2R2	…	237R2	238R2	239R2
D13		0R1	1R1	2R1	…	237R1	238R1	239R1
D12		0R0	1R0	2R0	…	237R0	238R0	239R0
D11		0G5	1G5	2G5	…	237G5	238G5	239G5
D10		0G4	1G4	2G4	…	237G4	238G4	239G4
D9		0G3	1G3	2G3	…	237G3	238G3	239G3
D8		0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C7	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C6	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C5	0B5	1B5	2B5	…	237B5	238B5	239B5
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

The 8080-II system 18-bit parallel bus interface mode can be selected by settings IM [3:0] =”0011”. The following shown figure is the example of interface with 8080- MCU system interface.

Figure59.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1)65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “101”.

Table29.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8	C7	0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C6	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C5	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C4	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C3	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C2	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C1	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C0	0B1	1B1	2B1	…	237B1	238B1	239B1
D0		0B0	1B0	2B0	…	237B0	238B0	239B0

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Table30.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17		0R5	1R5	2R5	…	237R5	238R5	239R5
D16		0R4	1R4	2R4	…	237R4	238R4	239R4
D15		0R3	1R3	2R3	…	237R3	238R3	239R3
D14		0R2	1R2	2R2	…	237R2	238R2	239R2
D13		0R1	1R1	2R1	…	237R1	238R1	239R1
D12		0R0	1R0	2R0	…	237R0	238R0	239R0
D11		0G5	1G5	2G5	…	237G5	238G5	239G5
D10		0G4	1G4	2G4	…	237G4	238G4	239G4
D9		0G3	1G3	2G3	…	237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C4	0B5	1B5	2B5	…	237B5	238B5	239B5

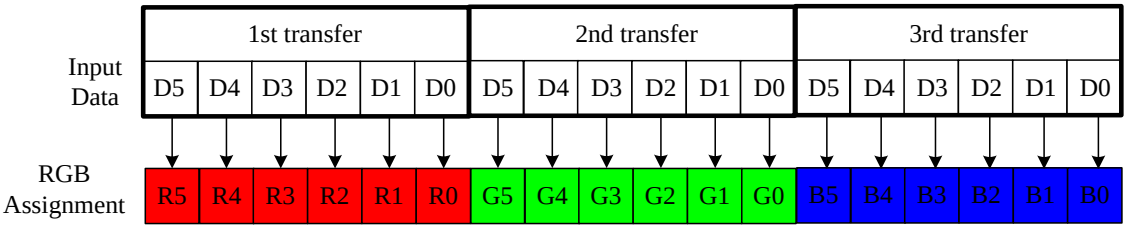
D4	**C3**	**0B4**	**1B4**	**2B4**	**…**	**237B4**	**238B4**	**239B4**
D3	**C2**	**0B3**	**1B3**	**2B3**	**…**	**237B3**	**238B3**	**239B3**
D2	**C1**	**0B2**	**1B2**	**2B2**	**…**	**237B2**	**238B2**	**239B2**
D1	**C0**	**0B1**	**1B1**	**2B1**	**…**	**237B1**	**238B1**	**239B1**
D0		**0B0**	**1B0**	**2B0**	**…**	**237B0**	**238B0**	**239B0**

4.5.8. 6-bit Parallel RGB Interface

The 6-bit RGB interface is selected by setting the RIM bit to “1”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (D [5:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. the valid display data is inputted in pixel unit via D [5:0] according to the VFP/VBP and HFP/HBP settings. Unused pins must be connected to GND to ensure normally operation. Registers can be set by the SPI system interface.

1)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

Figure60.



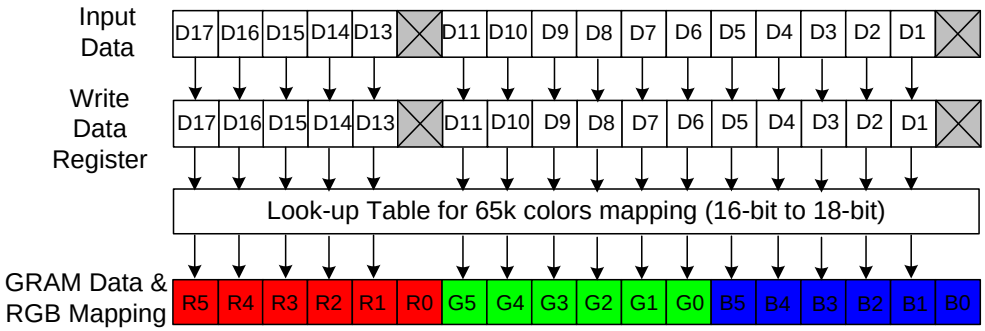
GC9A01 has data transfer counters to count the first, second, third data transfer in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK).Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.

4.5.9. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits to “101”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data is transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (D[17:13] & D[11:0]) according to the data enable signal (DE). The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D[17:13] & D[11:0] according to the VFP/VBP and HFP/HBP settings. The unused D12 and D0 pins must be connected to GND for ensure normally operation. Registers can be set by the SPI system interface.

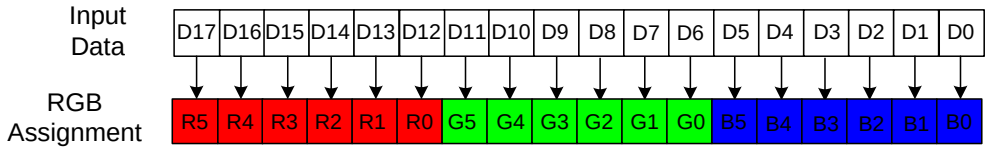
Figure62.



4.5.10. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits to “110”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (D [17:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D[17:0] according to the VFP/VBP and HFP/HBP settings. Registers can be set by the SPI system interface.

Figure63.



5. Function Description

5.1. Display data GRAM mapping

The display data RAM stores display dots and consists of 240x240x18 bits. There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

Every pixel (18-bit) data in GRAM is located by a (Page, Column) address (Y, X). By specifying the arbitrary window address **SC, EC** bits and **SP, EP** bits, it is possible to access the GRAM by setting RAMWR or RAMRD commands from start positions of the window address.

GRAM address for display panel position as shown in the following table

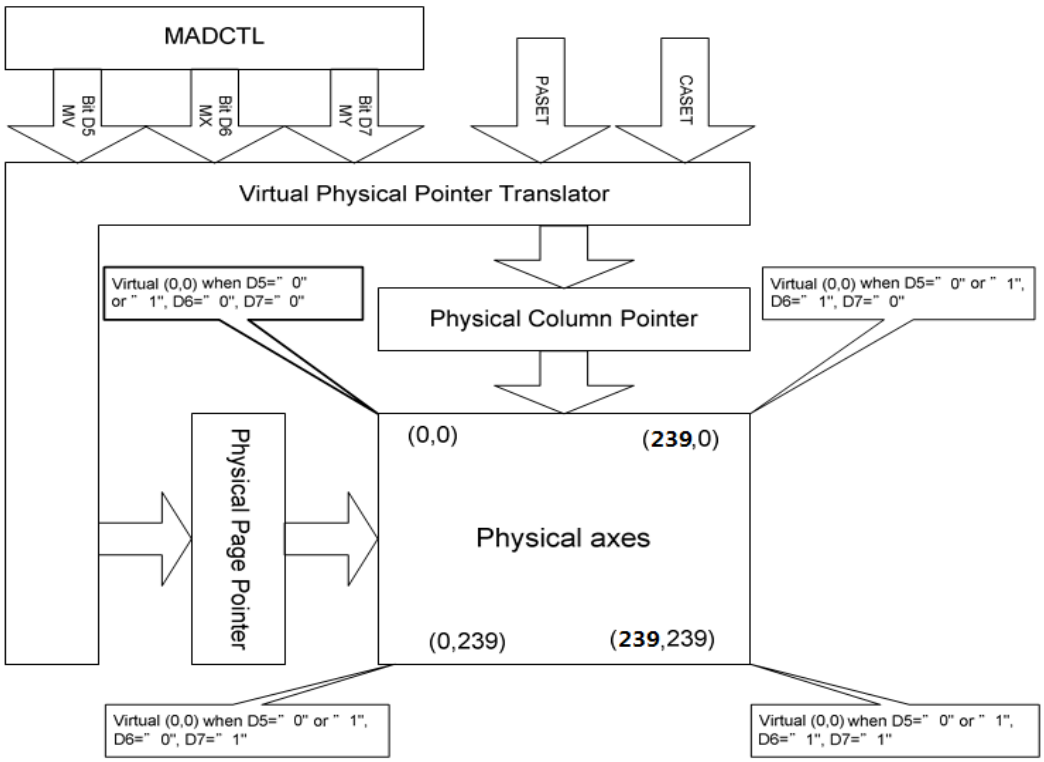
Table31.

(00,00)h	(00,01)h	…… …	(00, ED)h	(00, EE)h	(00,EF)h
(01,00)h	(01,01)h	…… …	(01, ED)h	(01, EE)h	(01, EF)h
(02,00)h	(02,01)h	…… …	(02, ED)h	(02, EE)h	(02, EF)h
(03,00)h	(03,01)h	…… …	(03, ED)h	(03, EE)h	(03, EF)h
. . .	. . .	. . .	. . .	. . .	. . .
(ED,00)h	(ED,01)h	…… …	(ED, ED)h	(ED, EE)h	(ED, EF)h
(EE,00)h	(EE,01)h	…… …	(EE, ED)h	(EE, EE)h	(EE, EF)h
(EF,00)h	(EF,01)h	…… …	(EF, ED)h	(EF, EE)h	(EF, EF)h

5.2. MCU to memory write/read direction

The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, Bits D5, D6, and D7 as described

below.

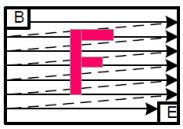
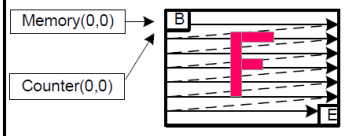
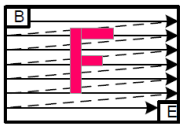
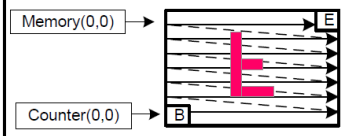
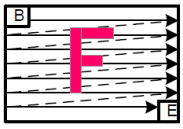
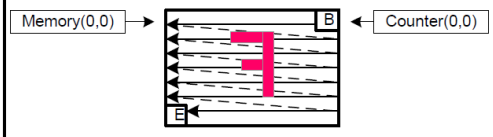
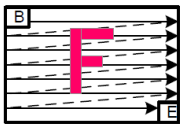
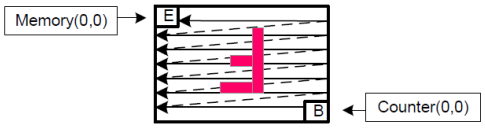
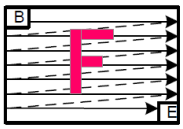
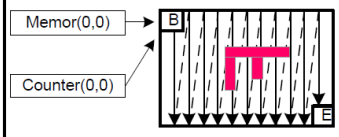
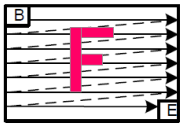
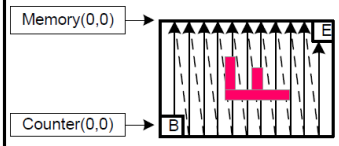
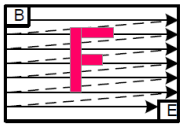
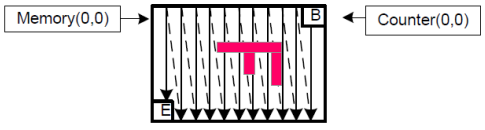
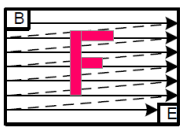
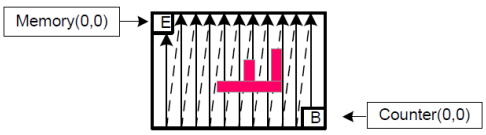


D5	D6	D7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (239-Physical Page Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (239-Physical Column Pointer)	Direct to (239-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (239-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (239-Physical Page Pointer)	Direct to (239-Physical Column Pointer)

Condition	Column Counter	Page counter
When RAMWR/RAMRD command is accepted	Return to “Start column”	Return to “Start Page”
Complete Pixel Read/Write action	Increment by 1	No change
The Column values is large than “End Column”	Return to “Start column”	Increment by 1
The Page counter is large than “End Page”	Return to “Start column”	Return to “Start Page”

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

Display Data Direction	MADCTR Parameter			Image in the Memory (MCU)	Image in the Driver (Frame Memory)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

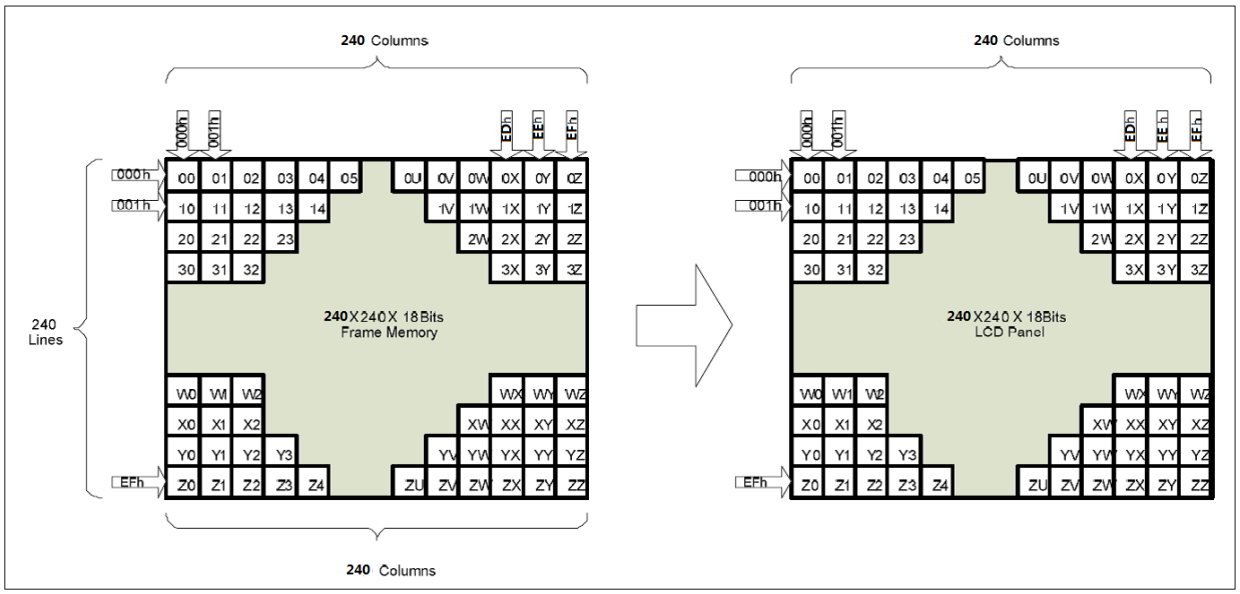
5.3. GRAM to display address mapping

By setting the **SS**, the relation between the source output channel and the GRAM address can be changed as reverse display. By setting the **GS** , the relation between the gate output channel and the GRAM address can be changed as reverse display. By setting the **BGR**, the relation between the source output channel and the <R>, <G>, <B> dot allocation can be reversed for different LCD color filter arrangement.

The following Tables show relations among the GRAM data allocation, the source output channel, and the R, G, B dot allocation.

GRAM X address and display panel position:

GC9A01 supports three kinds of display mode: one is Normal Display Mode, the other is Partial Display Mode, and Scrolling Display Mode.

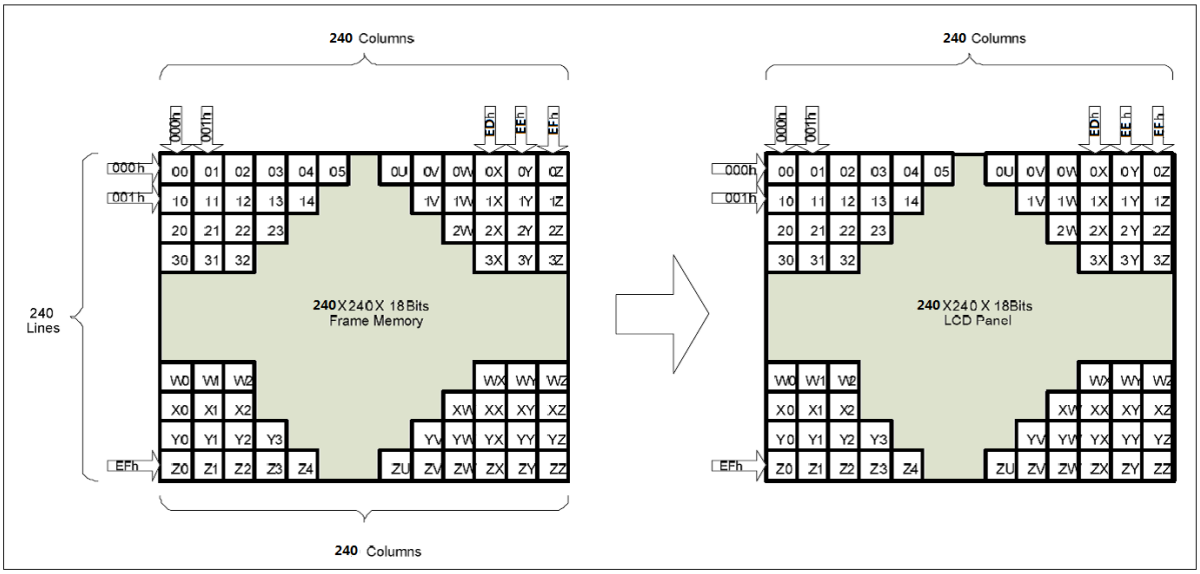


5.3.1. Normal display on or partial mode on, vertical scroll off

In this mode, content of the frame memory within an area where column pointer is 0000h to 00EFh and page pointer is 0000h to 00EFh is displayed.

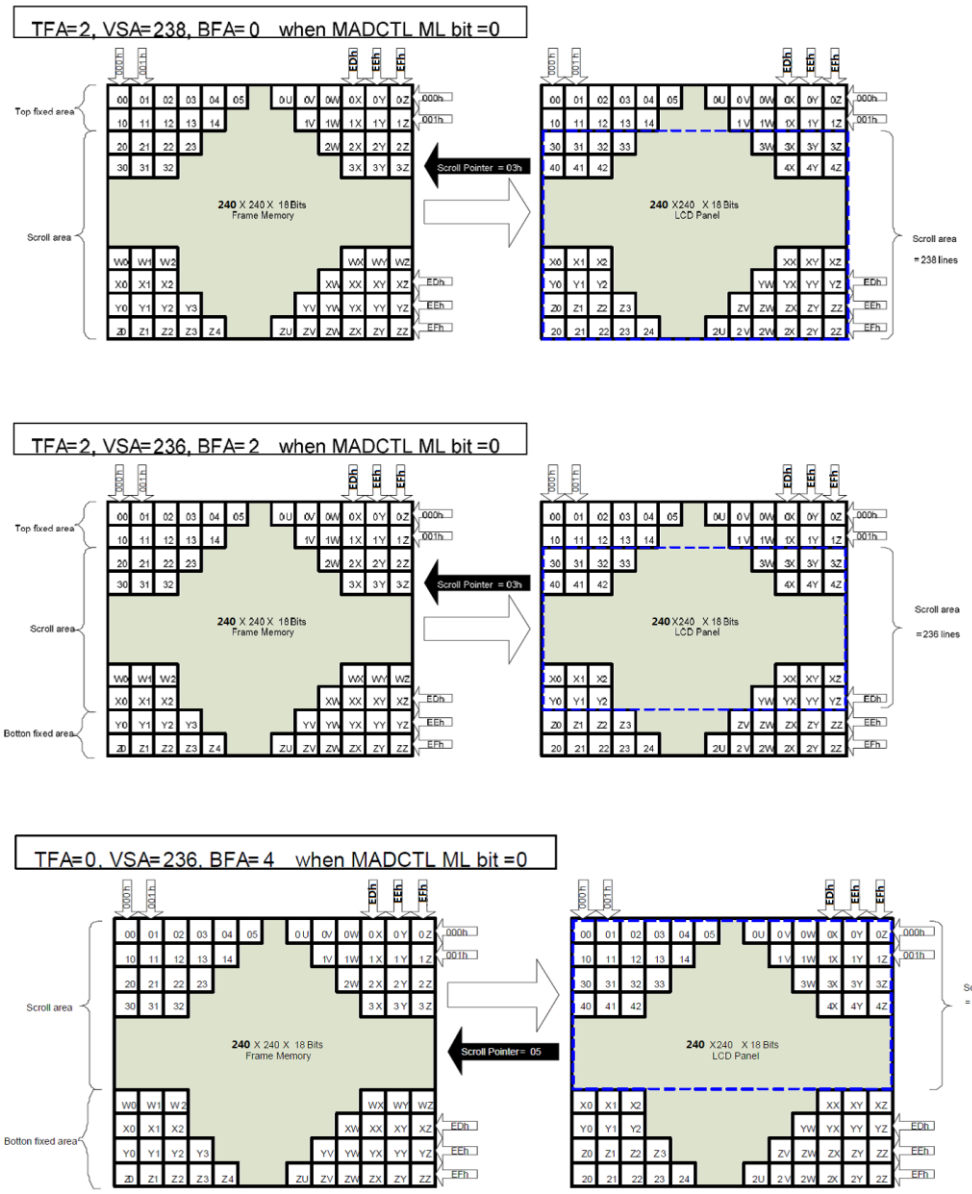
To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0)

Figure66.



5.3.2. Vertical scroll display mode

When setting R37h, the scrolling display mode is active, and the vertical scrolling display is specified by **TFA, VSA ,BFA** bits (R33h) and **VSP** bits (R37h).



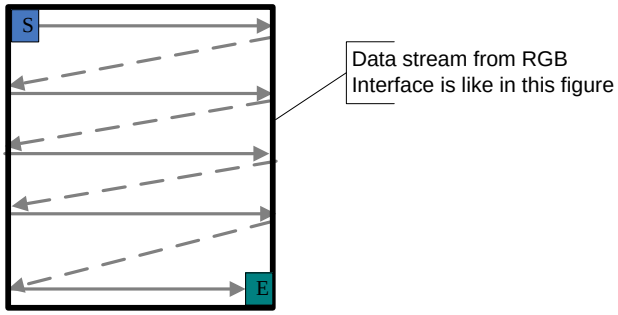
Note: When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) ≠ 240, Scrolling Mode is undefined.

5.3.3. Updating order on display active area in RGB interface mode

There is defined different kind of updating orders for display in RGB interface mode (**RCM [1:0]** =’1x’).

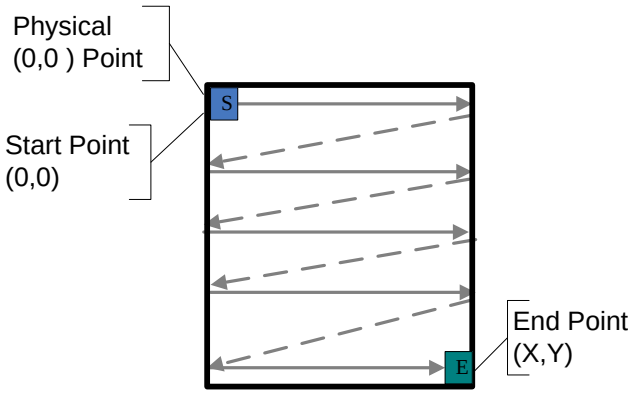
These updating are controlled by **MY** and **MX** bits. Data streaming direction from the host to the display is described in the following figure.

Figure74.



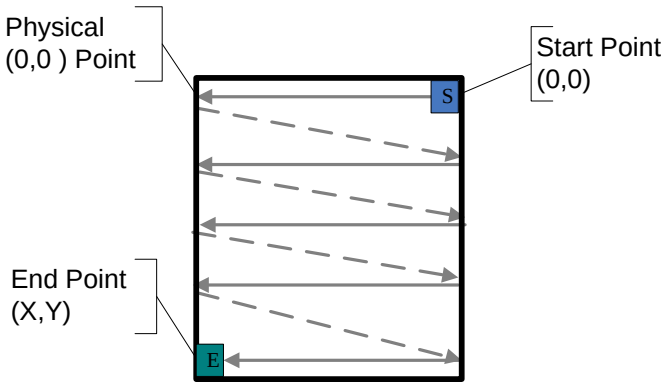
Updating order when MY = ‘0’ and MX = ‘0’

Figure75.



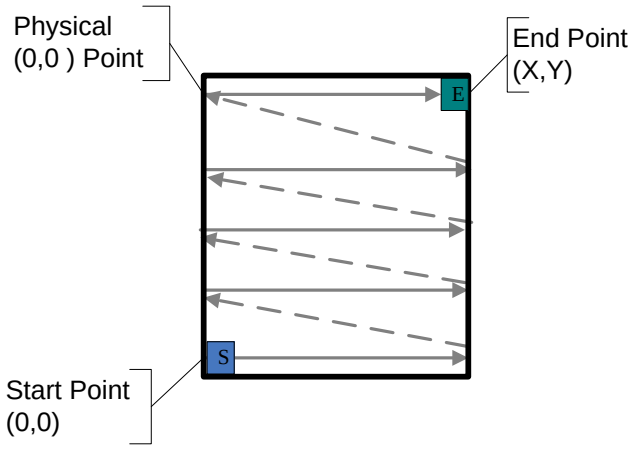
Updating order when MY = ‘0’ and MX = ‘1’

Figure76.



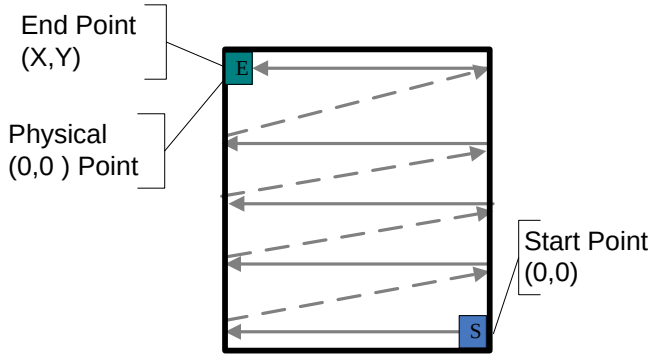
Updating order when MY = ‘1’ and MX = ‘0’

Figure77.



Updating order when MY = '1' and MX = '1'

Figure78.



Rules for updating order on display active area in RGB interface display mode:

Table37.

Condition	Horizontal Counter	Vertical Counter
An active VS signal is received	Return to 0	Return to 0
Single Pixel information of the active area is received	Increment by 1	No change
An active HS signal between two active area lines	Return to 0	Increment by 1
The Horizontal counter value is larger than X and the Vertical counter value is larger than Y	Return to 0 "Start Column"	Return to "Start Page"

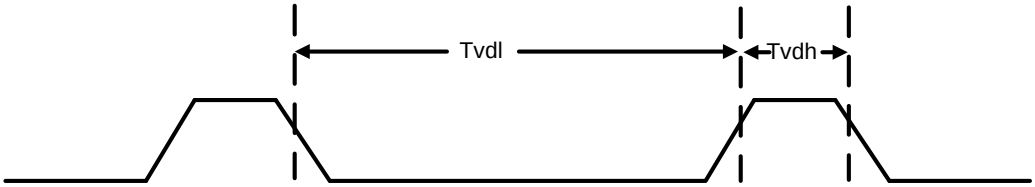
Note: Pixel order is RGB on the display.

5.4. Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

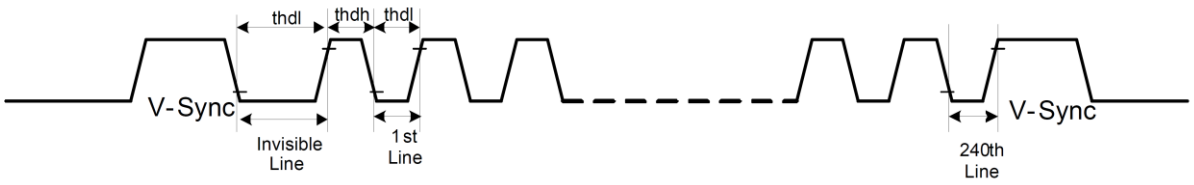
5.4.1. Tearing effect line modes

Mode 1, The Tearing Effect Output signal consists of V-Blanking Information only:
Figure79.



tVdh= The LCD display is not updated from the Frame Memory
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, The Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 240 H-sync pulses per field.
Figure80.

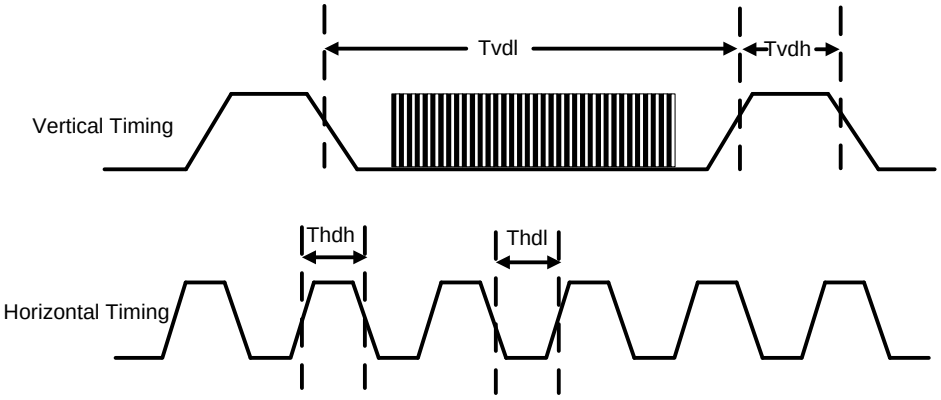


thdh= The LCD display is not updated from the Frame Memory
thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

5.4.2. Tearing effect line timing

The Tearing Effect signal is described below.

Figure81.



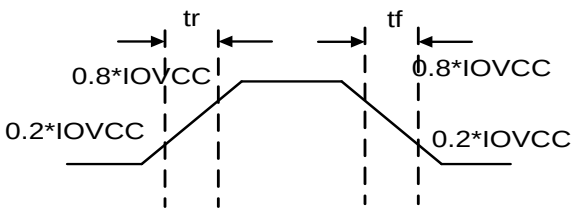
Idle Mode Off (Frame Rate = 20~90 Hz)

Table38.

Symbol	Parameter	Spec.			Description
		Min.	Max.	Unit	
tvdl	Vertical Timing Low Duration	TBD	-	ms	-
tvdh	Vertical Timing High Duration	1000	-	us	-
thdl	Horizontal Timing Low Duration	TBD	-	us	-
thdh	Horizontal Timing High Duration	TBD	500	us	-

Note: Idle Mode Off (Frame Rate = 20~90 Hz) ,The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

Figure82.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

5.5. Source driver

The GC9A01 contains a 360 channels of source driver (S1~S360) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 360 channels and generates corresponding
gray scale voltage output, which can realize a 262K colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

5.6. Gate driver

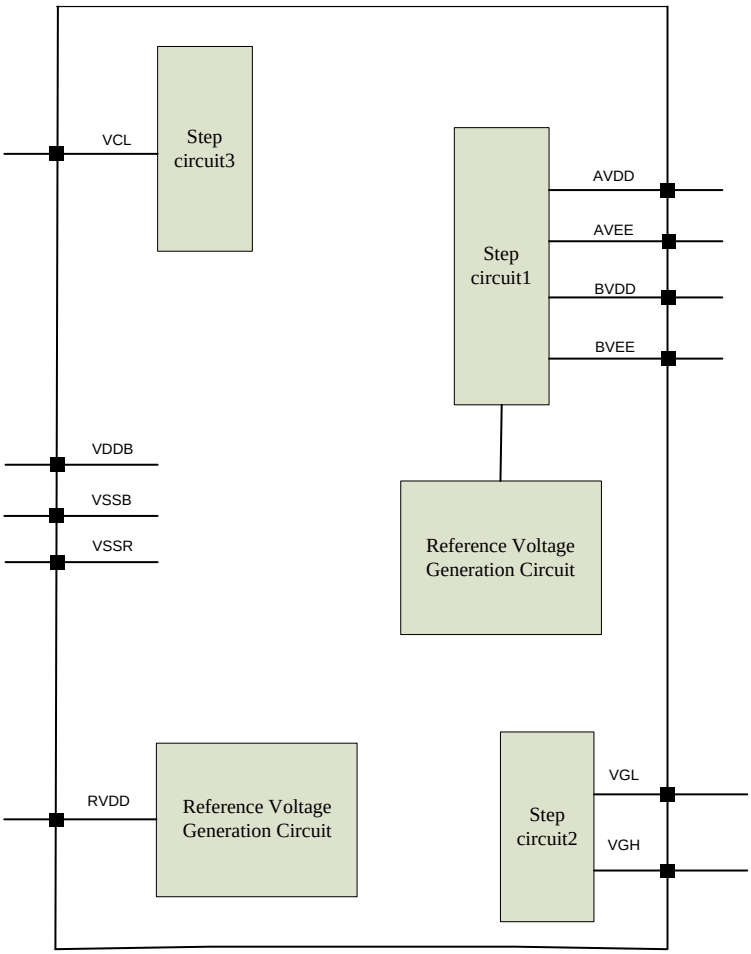
The GC9A01 contains a 32 gate channels of gate driver (G1~G32) which is usedfor driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

5.7. LCD power generation circuit

5.7.1. Power supply circuit

The power circuit of GC9A01 is used to generate supply voltages for LCD panel driving.

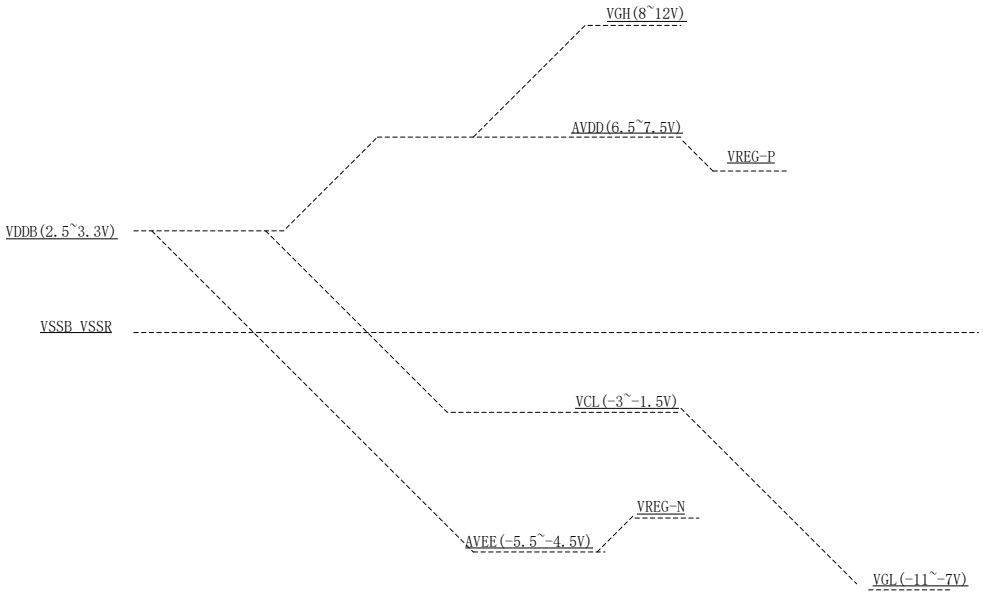
Figure83.



5.7.2. LCD power generation scheme

The boost voltage generated is shown as below.

Figure84.



LCD power generation scheme

5.8. Gamma Correction

GC9A01 incorporates the γ-correction function to display 262,144 colors for the LCD panel. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make GC9A01 available with liquid crystal panels of various characteristics.

Figure85.

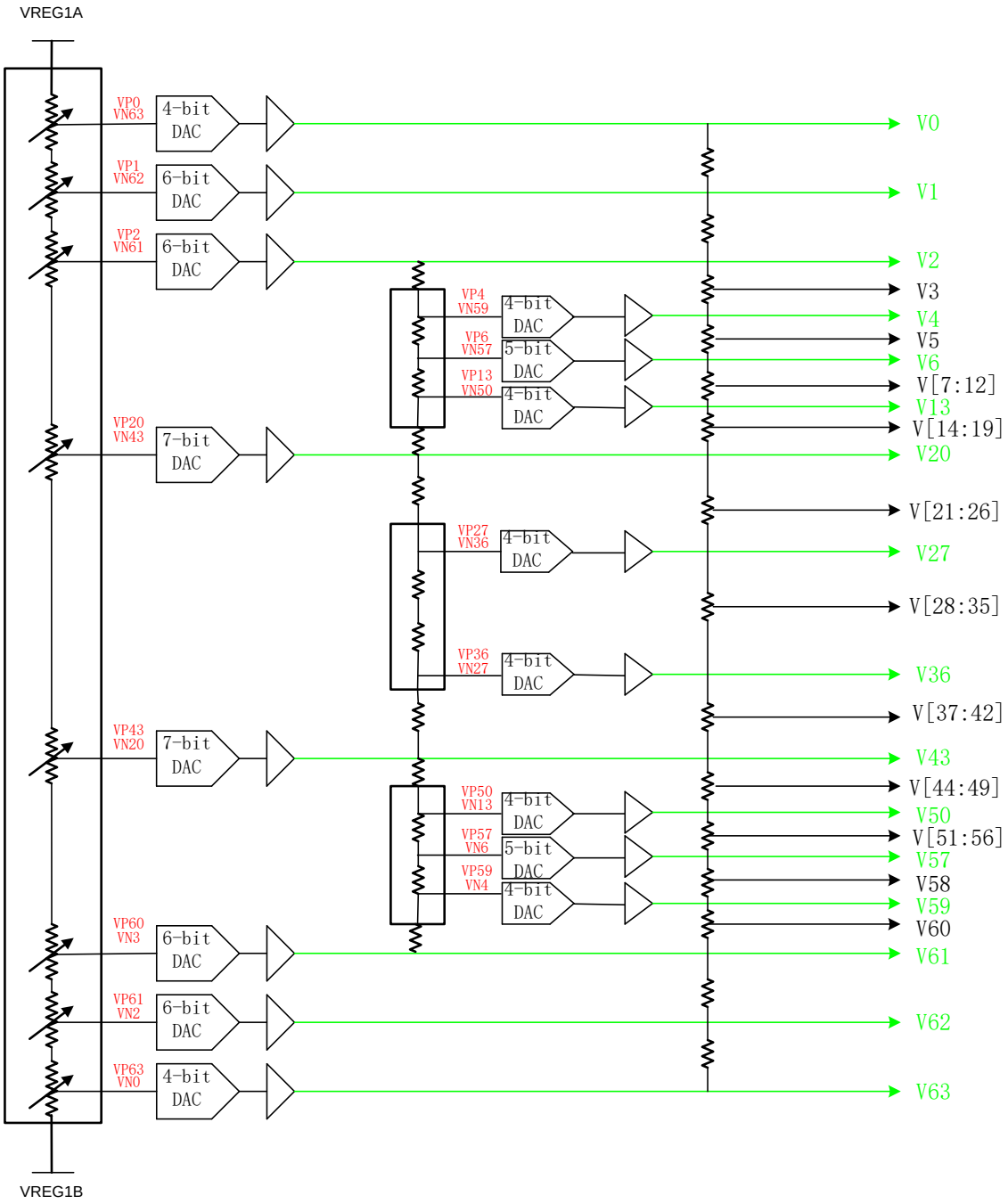
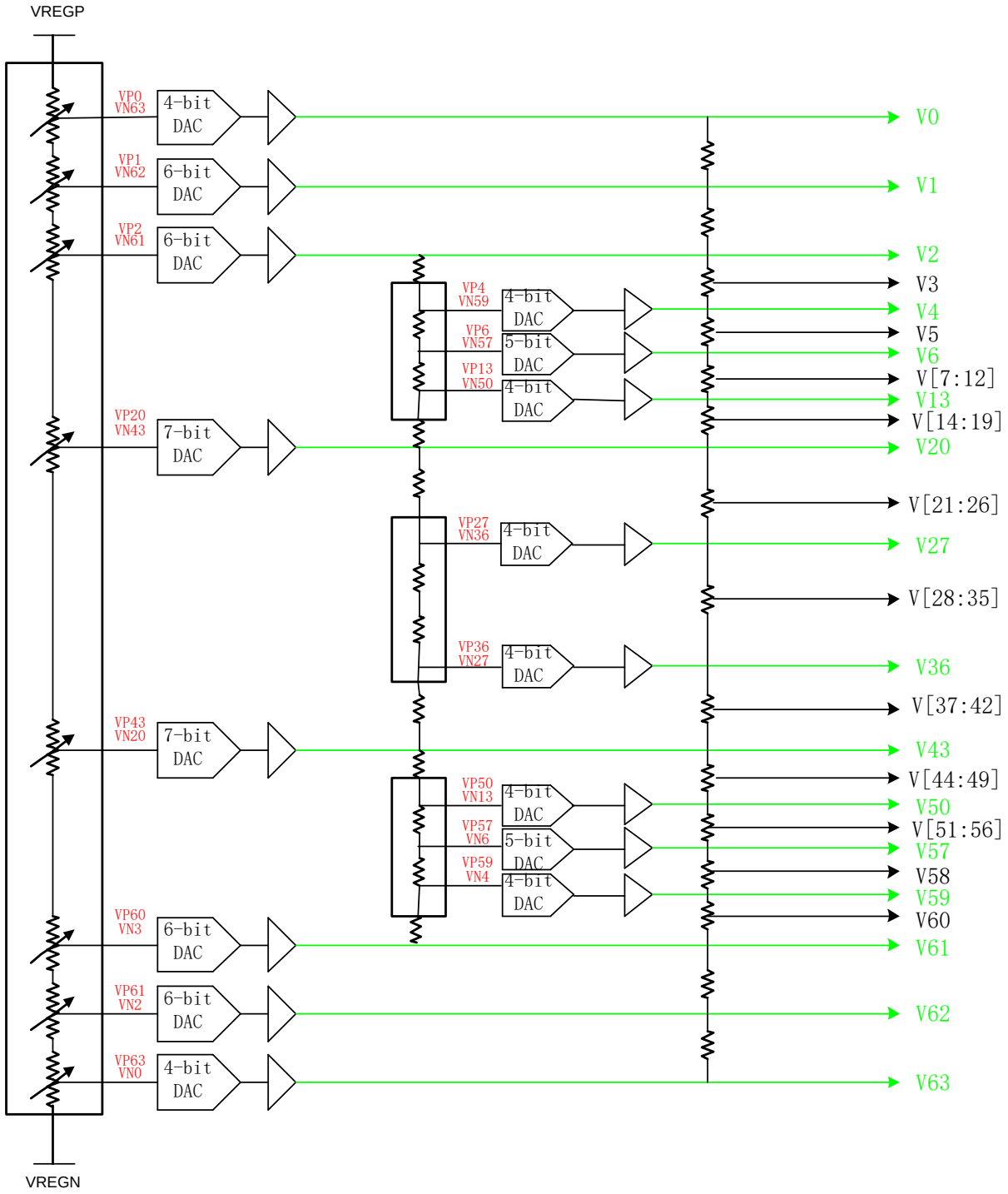
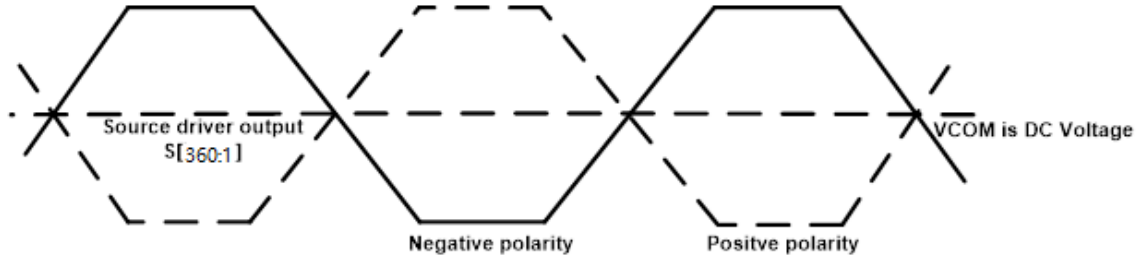


Figure86.



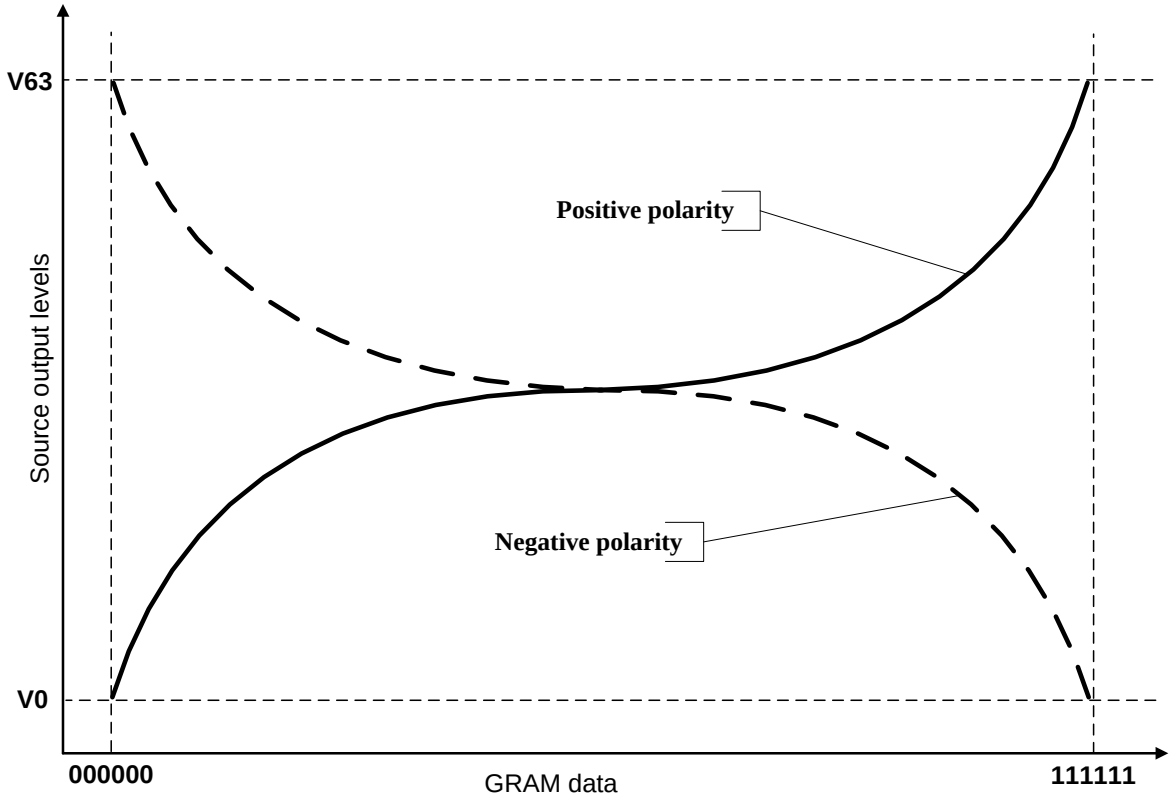
Grayscale Voltage Generation

Figure87.Dot inversion



Relationship between Source Output and VCOM

Figure88.



5.9. Power Level Definition

5.9.1. Power Levels

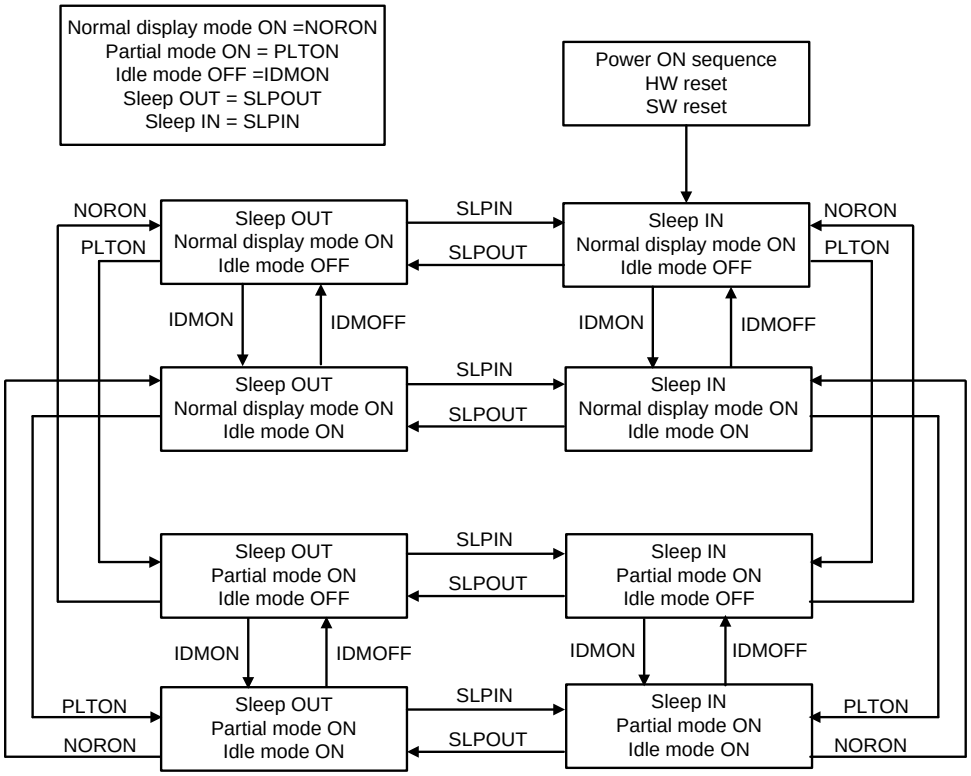
6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out.
   In this mode part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out.
   In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode.
   In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VDDB and VDDI are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

5.9.2. Power Flow Chart

Figure89.



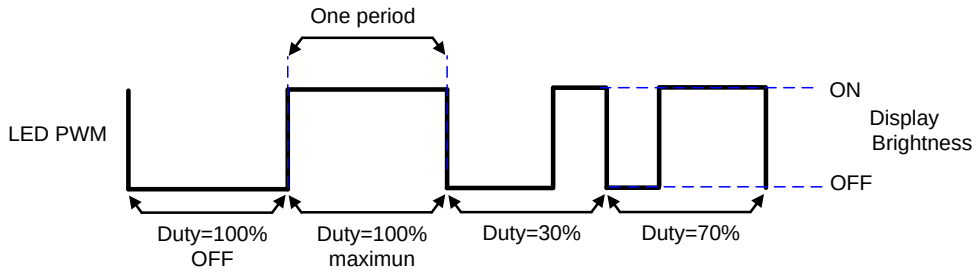
Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

5.10.3.Brightness control block

There is an external output signal from brightness block, LEDPWM to control the LED driver IC in order to control display brightness.
There are resister bits, DBV[7:0] of R51h, for display brightness of manual brightness setting. The LEDPWM duty is calculated as DBV[7:0]/255 x period (affected by OSC frequency).
For example: LEDPWM period = 3ms, and DBV[7:0] = '200DEC'. Then LEDPWM duty = 200 / 255=78.1%.
Correspond to the LEDPWM period = 3 ms, the high-level of LEDPWM (high effective) = 2.344ms, and the low-level of LEDPWM = 0.656ms.

Figure90.



LEDPWM output duty

5.10. Input/output pin state

5.10.1. Output pins

Table40.

Output or Bi-directional pins	After Power On	After Hardware Reset
DB17 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)
SDA	High-Z (Inactive)	High-Z (Inactive)
SDO	High-Z (Inactive)	High-Z (Inactive)
TE	Low	Low
LEDPWM	Low	Low

Characteristics of output pins

5.10.2. Input pins

Table41.

Input pins	During Power On Process	After Power On	After Hardware Reset	During Power Off Process
RESX	Input valid	Input valid	Input valid	Input valid
CSX	Input invalid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input invalid
SDA	Input invalid	Input valid	Input valid	Input invalid
VSYNC	Input invalid	Input valid	Input valid	Input invalid
HSYNC	Input invalid	Input valid	Input valid	Input invalid
DE	Input invalid	Input valid	Input valid	Input invalid
DOTCLK	Input invalid	Input valid	Input valid	Input invalid
D[17:0]	Input invalid	Input valid	Input valid	Input invalid
IM[3:0]	Input invalid	Input valid	Input valid	Input invalid

Characteristics of input pins

6. Command

6.1. Command List

Regulative Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Read Display Identification Information 2	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID_1[7:0]								00
	1	↑	1	XX	ID_2[7:0]								9A
	1	↑	1	XX	ID_3[7:0]								01
Read Display Status	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D[31:25]							X	00
	1	↑	1	XX	X	D[22:20]			D[19:16]				61
	1	↑	1	XX	X	X	X	X	X	D[10:8]			00
	1	↑	1	XX	D[7:5]			X	X	X	X	X	00
Enter Sleep Mode	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Sleep OUT	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
Partial Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	0	12h
Normal Display Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	1	13h
Display Inversion OFF	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Display Inversion ON	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Display OFF	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Display ON	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
Column Address Set	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
	1	1	↑	XX	SC[15:8]								00
	1	1	↑	XX	SC[7:0]								00
	1	1	↑	XX	EC[15:8]								01
	1	1	↑	XX	EC[7:0]								3Fh
Page Address Set	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
	1	1	↑	XX	SP[15:8]								00
	1	1	↑	XX	SP[7:0]								00
	1	1	↑	XX	EP[15:8]								00h

	1	1	↑	XX	EP[7:0]								EFh
Memory Write	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
	1	1	↑	D[17:0]									XX
Partial Area	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
	1	1	↑	XX	SR[15:8]								00
	1	1	↑	XX	SR[7:0]								00
	1	1	↑	XX	ER[15:8]								00
	1	1	↑	XX	ER[7:0]								EF
Vertical Scrolling Definition	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
	1	1	↑	XX	TFA[15:8]								00
	1	1	↑	XX	TFA[7:0]								00
	1	1	↑	XX	VSA[15:8]								00
	1	1	↑	XX	VSA[7:0]								F0
Tearing Effect Line OFF	0	1	↑	XX	0	0	1	1	0	1	0	0	34h
Tearing Effect Line ON	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
	1	1	↑	XX	X	X	X	X	X	X	X	M	00
Memory Access Control	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	X	X	00
Vertical Scrolling Start Address	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
	1	1	↑	XX	VSP[15:8]								00
	1	1	↑	XX	VSP[7:0]								00
Idle Mode OFF	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
Idle Mode ON	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Pixel Format Set	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
	1	1	↑	XX	X	DPI[2:0]			X	DBI[2:0]			66
Write Memory Continue	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch
	1	1	↑	D[17:0]									XX
Set Tear Scanline	0	1	↑	XX	0	1	0	0	0	1	0	0	44h
	1	1	↑	XX	X	X	X	X	X	X	X	STS[8]	00
	1	1	↑	XX	STS[7:0]								00
Get Scanline	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	X	X	GTS [8]	00
	1	↑	1	XX	GTS[7:0]								00
Write Display Brightness	0	1	↑	XX	0	1	0	1	0	0	0	1	51h
	1	↑	1	XX	DBV[7:0]								00
Write CTRL Display	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
	1	1	↑	XX	X	X	BCTRL	X	DD	BL	X	X	00
Read ID1	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh

	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								00
Read ID2	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								9A
Read ID3	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								01

Extended Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RGB Interface Signal Control	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
	1	1	↑	XX	X	RCM[1:0]		X	VSPL	HSPL	DPL	EPL	01
Blanking Porch Control	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
	1	1	↑	XX	0	0	0	0	VFP[3:0]				08
	1	1	↑	XX	0	VBP[6:0]							02
	1	1	↑	XX	0	0	0	HBP[4:0]					14
Display Function Control	0	1	1	XX	1	0	1	1	0	1	1	0	B6
	1	1	1	XX	X	X	X	X	X	X	X	X	00
	1	1	1	XX	X	GS	SS	SM	X	X	X	X	00
	1	1	1	XX	X	X	NL[5:0]						1D
TE Control	0	1	↑	XX	1	0	1	1	1	0	1	0	BAh
	1	1	↑	XX	te_pol	te_width[6:0]							00
Interface Control	0	1	↑	XX	1	1	1	1	0	1	1	0	F6h
	1	1	↑	XX	1	1	0	0	DM[1:0]		RM	RIM	C0

Inter Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Power Criterion Control	0	1	↑	XX	1	1	0	0	0	0	0	1	C1h
	1	1	↑	XX	0	0	0	0	0	0	vcire	0	00
DVDD voltage Control	0	1	↑	XX	1	0	1	0	0	1	1	1	A7h
	1	1	↑	XX	0	1	0	0	vdd_ad[3:0]				48
Vreg1a voltage Control	0	1	↑	XX	1	1	0	0	0	0	1	1	C3h
	1	1	↑	XX	0	vreg1_vbp_d[6:0]							3C
Vreg1b voltage Control	0	1	↑	XX	1	1	0	0	0	1	0	0	C4h
	1	1	↑	XX	0	vreg1_vbn_d[6:0]							3C
Vreg2a voltage Control	0	1	↑	XX	1	1	0	0	1	0	0	1	C9h
	1	1	↑	XX	0	0	vrh[5:0]						28
Frame Rate	0	1	↑	XX	1	0	1	0	1	0	0	0	E8

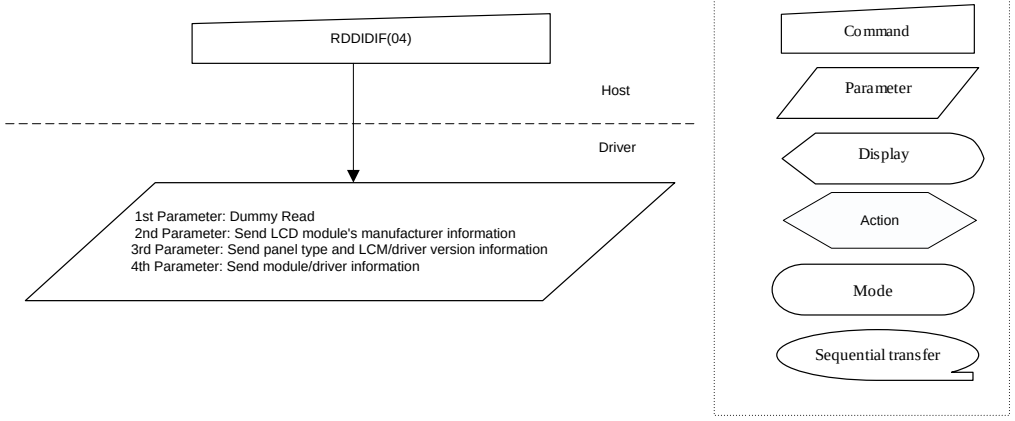
													h
	1	1	↑	XX	0	DINV[2:0]			RTN1[3:0]				11
	1	1	↑	XX	RTN2[7:0]								40
SPI 2data control	0	1	↑	XX	1	1	1	0	1	0	0	1	E9 h
	1	1	↑	XX					2data_ en	2data_mdt			00
Charge Pump Frequent Control	0	1	↑	XX	1	1	1	0	1	1	0	0	EC h
	1	1	↑	XX		avdd_clk_ad[2: 0]				avee_clk_ad[2:0]			33
	1	1	↑	XX						vcl_clk_ad[2:0]			02
	1	1	↑	XX	vgh_clk_ad[3:0]				vgl_clk_ad[3:0]				88
Inner register enable 1	0	1	↑	XX	1	1	1	1	1	1	1	0	FE h
Inner register enable 2	0	1	↑	XX	1	1	1	0	1	1	1	1	EF h
SET_GAM MA1	0	1	↑	XX	1	1	1	1	0	0	0	0	F0h
	1	1	↑	XX	dig2gam_ dig2j0_n[1:0]	dig2gam_vr1_n[5:0]							80
	1	1	↑	XX	dig2gam_ dig2j1_n[1:0]	dig2gam_vr2_n[5:0]							03
	1	1	↑	XX	0	0	0	dig2gam_vr4_n[4:0]					08
	1	1	↑	XX	0	0	0	dig2gam_vr6_n[4:0]					06
	1	1	↑	XX	dig2gam_vr0_n[3:0]				dig2gam_vr13_n[3:0]				05
	1	1	↑	XX	0	dig2gam_vr20_n[6:0]							2B
SET_GAM MA2	0	1	↑	XX	1	1	1	1	0	0	0	1	F1h
	1	1	↑	XX	0	dig2gam_vr43_n[6:0]							41
	1	1	↑	XX	dig2gam_vr27_n [2:0]			dig2gam_vr57_n[4:0]					97
	1	1	↑	XX	dig2gam_vr36_n [2:0]			dig2gam_vr59_n[4:0]					98
	1	1	↑	XX	0	0	dig2gam_vr61_n[5:0]						13
	1	1	↑	XX	0	0	dig2gam_vr62_n[5:0]						17
	1	1	↑	XX	dig2gam_vr50_n[3:0]				dig2gam_vr63_n[3:0]				CD
SET_GAM MA3	0	1	↑	XX	1	1	1	1	0	0	1	0	F2h
	1	1	↑	XX	dig2gam_ dig2j0_p[1:0]	dig2gam_vr1_p[5:0]							40

	1	1	↑	XX	dig2gam_dig2j1_p[1:0]		dig2gam_vr2_p[5:0]							03
	1	1	↑	XX	0	0	0	dig2gam_vr4_p[4:0]						08
	1	1	↑	XX	0	0	0	dig2gam_vr6_p[4:0]						0B
	1	1	↑	XX	dig2gam_vr0_p[3:0]				dig2gam_vr13_p[3:0]					08
	1	1	↑	XX	0	dig2gam_vr20_p[6:0]								2E
SET_GAMMA4	0	1	↑	XX	1	1	1	1	0	0	1	1		F3h
	1	1	↑	XX	0	dig2gam_vr43_p[6:0]								3F
	1	1	↑	XX	dig2gam_vr27_p[2:0]			dig2gam_vr57_p[4:0]						98
	1	1	↑	XX	dig2gam_vr36_p[2:0]			dig2gam_vr59_p[4:0]						B4
	1	1	↑	XX	0	0	dig2gam_vr61_p[5:0]							14
	1	1	↑	XX	0	0	dig2gam_vr62_p[5:0]							18
	1	1	↑	XX	dig2gam_vr50_p[3:0]				dig2gam_vr63_p[3:0]					CD

6.2. Description of Level 1 Command

6.2.1. Read display identification information (04h)

<table>
<tr><td>04h</td><td colspan="13">Read display identification information 2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>04h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID_1[7:0]</td><td>00</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID_2[7:0]</td><td>9A</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID_3[7:0]</td><td>01</td></tr>
<tr><td>Description</td><td colspan="13">This read byte returns 24 bits display identification information.
The 1st parameter is dummy data.
The 2nd parameter (ID2_1 [7:0]): LCD module’s manufacturer ID.
The 3rd parameter (ID2_2 [7:0]): LCD module/driver version ID.
The 4th parameter (ID2_3 [7:0]): LCD module/driver ID.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>24’h009A01</td></tr><tr><td>SW Reset</td><td>24’h009A01</td></tr><tr><td>HW Reset</td><td>24’h009A01</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"></td></tr>
</table>


RDDIDIF(04)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send LCD module's manufacturer information
3rd Parameter: Send panel type and LCM/driver version information
4th Parameter: Send module/driver information
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.2. Read Display Status (09h)

09h	Read Display Status												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D[31:25]							X	00
3rd Parameter	1	↑	1	XX	0	D[22:20]			D[19:16]				61
4th Parameter	1	↑	1	XX	0	0	0	0	0	D[10:8]			00
5th Parameter	1	↑	1	XX	D[7:5]			0	0	0	0	0	00

Description

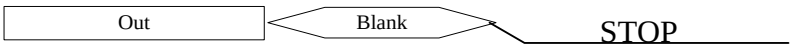
This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Status
D31	Booster voltage status	O	Booster OFF
		1	Booster ON
D30	Row address order	O	Top to Bottom (When MADCTL B7='0')
		1	Bottom to Top (When MADCTL B7='1')
D29	Column address order	O	Left to Right (When MADCTL B6='0').
		1	Right to Left (When MADCTL B6='1').
D28	Row/column exchange	O	Normal Mode (When MADCTL B5='0').
		1	Reverse Mode (When MADCTL B5='1').
D27	Vertical refresh	O	LCD Refresh Top to BoUom (When MADCTL B4='0')
		1	LCD Refresh BoUom to Top (When MADCTL B4='1').
D26	RGB/BGR order	O	RGB (When MADCTL B3='0')
		1	BGR (When MADCTL B3='1')
D25	Horizontal refresh order	O	LCD Refresh Left to Right (When MADCTL B2='0')
		1	LCD Refresh Right to Left (When MADCTL B2='1')
D24	Not used	O	-
D23	Not used	O	-
D22	Interface color pixel format definition	101	16-bit/pixel
D21		110	18-bit/pixel
D20			

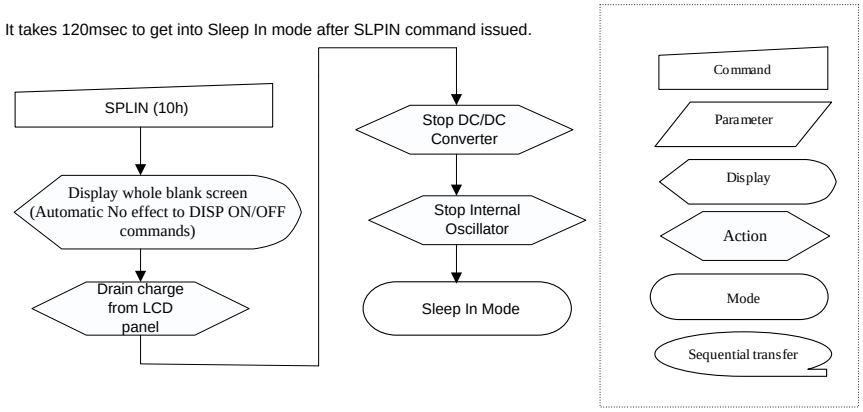
		D19	Idle mode ON/OFF	O	Idle Mode OFF
				1	Idle Mode ON
		D18	Partial mode ON/OFF	O	Partial Mode OFF
				1	Partial Mode ON
		D17	Sleep IN/OUT	O	Sleep IN Mode
				1	Sleep OUT Mode
		D16	Display normal mode ON/OFF	O	Display Normal Mode OFF.
				1	Display Normal Mode ON.
		D15	Vertical scrolling status	O	Scroll OFF
		D14	Not used	O	-
		D13	Inversion status	O	Not defined
		D12	All pixel ON	O	Not defined
		D11	All pixel OFF	O	Not defined
		D10	Display ON/OFF	O	
				1	Display is ON
		D9	Tearing effect line ON/OFF	O	Tearing Effect Line OFF
				1	Tearing Effect ON
		D5	Tearing effect line mode	0	Mode 1, V-Blanking only
				1	Mode 2, both H-Blanking and V-Blanking
		D4	Not used	O	-
		D3	Not used	O	-
		D2	Not used	O	-
		D1	Not used	O	-
		D0	Not used	O	-
Restriction					
Register Availability					

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

6.2.3. Enter Sleep Mode (10h)

<table>
<tr><td>10h</td><td colspan="13">Enter Sleep Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>10h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped
 

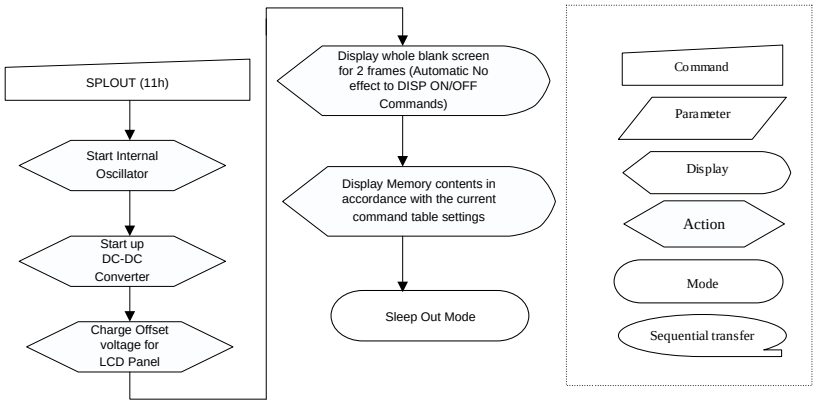
MCU interface and memory are still working and the memory keeps its contents.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr><tr><td>SW Reset</td><td>Sleep IN Mode</td></tr><tr><td>HW Reset</td><td>Sleep IN Mode</td></tr></table></td></tr>
</table>

Flow Chart	

It takes 120msec to get into Sleep In mode after SLPIN command issued.
SPLIN (10h)
Display whole blank screen (Automatic No effect to DISP ON/OFF commands)
Drain charge from LCD panel
Stop DC/DC Converter
Stop Internal Oscillator
Sleep In Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.4. Sleep Out Mode (11h)

<table>
<tr><td>11h</td><td colspan="13">Sleep Out Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>11h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns off sleep mode.
the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits stabilize. The display module loads all display supplier’s factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr><tr><td>SW Reset</td><td>Sleep IN Mode</td></tr><tr><td>HW Reset</td><td>Sleep IN Mode</td></tr></table></td></tr>
</table>

Flow Chart	 SPLOUT (11h) Start Internal Oscillator Start up DC-DC Converter Charge Offset voltage for LCD Panel Display whole blank screen for 2 frames (Automatic No effect to DISP ON/OFF Commands) Display Memory contents in accordance with the current command table settings Sleep Out Mode Command Parameter Display Action Mode Sequential transfer

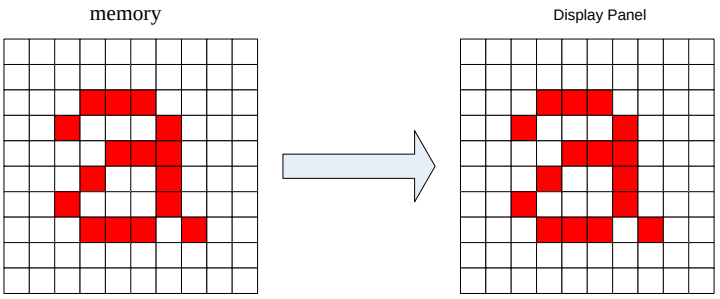
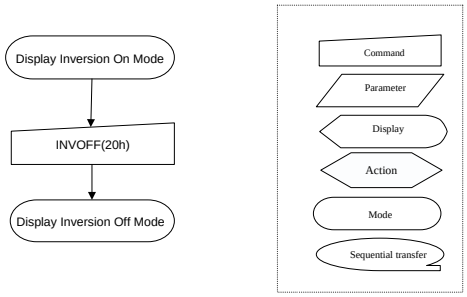
6.2.5. Partial Mode ON (12h)

<table>
<tr><td>12h</td><td colspan="13">Partial Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

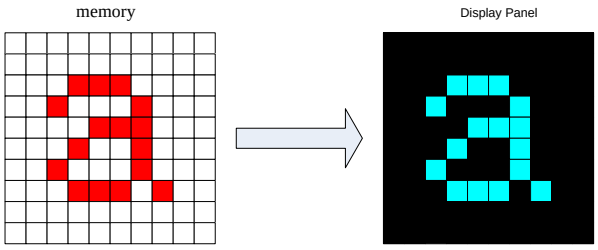
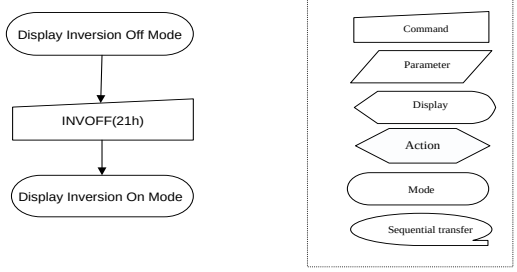
6.2.6. Normal Display Mode ON (13h)

<table>
<tr><td>13h</td><td colspan="13">Normal Display Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command returns the display to normal mode.
Normal display mode on means Partial mode off.
Exit from NORON by the Partial mode On command (12h)
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

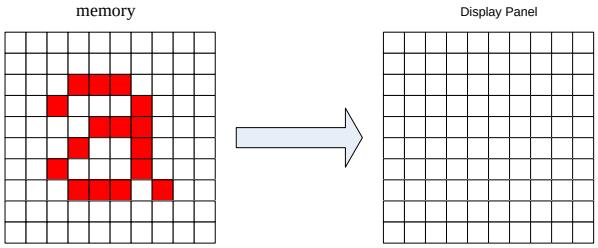
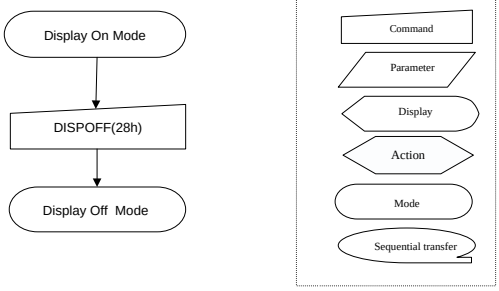
6.2.7. Display Inversion OFF (20h)

<table>
<tr><td>20h</td><td colspan="13">Display Inversion OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>20h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from display inversion mode.
This command makes no change of the content of frame memory.
This command doesn’t change any other status.
 
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module already is inversion OFF mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion OFF</td></tr><tr><td>SW Reset</td><td>Display Inversion OFF</td></tr><tr><td>HW Reset</td><td>Display Inversion OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">  </td></tr>
</table>

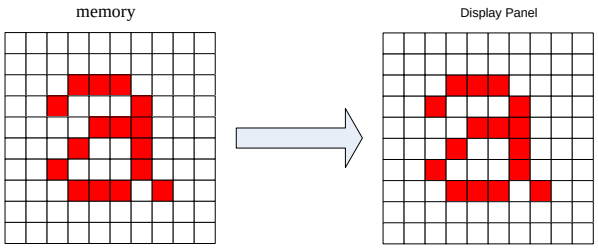
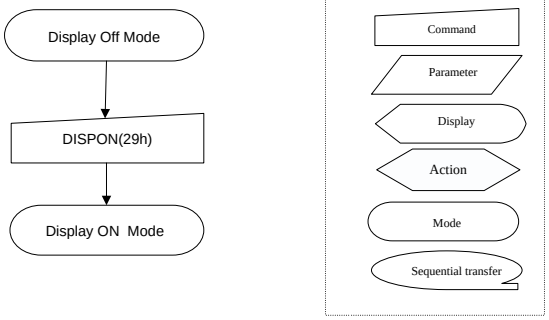
6.2.8. Display Inversion ON (21h)

<table>
<tr><td>21h</td><td colspan="13">Display Inversion ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>21h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to enter into display inversion mode.
This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display.
This command doesn’t change any other status.
To exit Display inversion mode, the Display inversion OFF command (20h) should be written..
 
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module already is inversion ON mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion OFF</td></tr><tr><td>SW Reset</td><td>Display Inversion OFF</td></tr><tr><td>HW Reset</td><td>Display Inversion OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">  </td></tr>
</table>

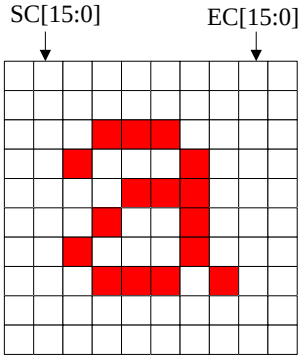
6.2.9. Display OFF (28h)

<table>
<tr><td>28h</td><td colspan="13">Display OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>28h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.
This command makes no change of contents of frame memory.
This command does not change any other status.
There will be no abnormal visible effect on the display.
 
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in display off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display OFF</td></tr><tr><td>SW Reset</td><td>Display OFF</td></tr><tr><td>HW Reset</td><td>Display OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">  </td></tr>
</table>

6.2.10. Display ON (29h)

<table>
<tr><td>29h</td><td colspan="13">Display ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>29h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.
This command makes no change of contents of frame memory.
This command does not change any other status.
 
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in display on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display OFF</td></tr><tr><td>SW Reset</td><td>Display OFF</td></tr><tr><td>HW Reset</td><td>Display OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">  </td></tr>
</table>

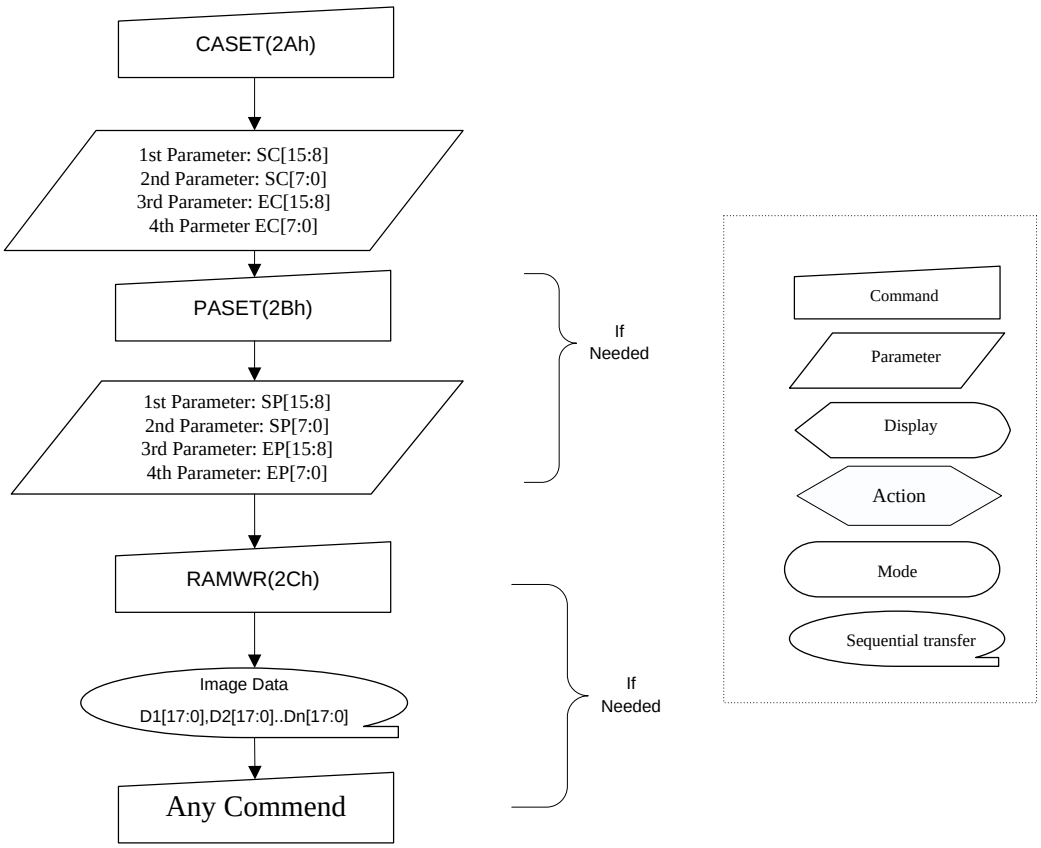
6.2.11. Column Address Set (2Ah)

<table>
<tr><td>2Ah</td><td colspan="13">Column Address Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>2Ah</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SC15</td><td>SC14</td><td>SC13</td><td>SC12</td><td>SC11</td><td>SC10</td><td>SC9</td><td>SC8</td><td rowspan="2">Note1</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SC7</td><td>SC6</td><td>SC5</td><td>SC4</td><td>SC3</td><td>SC2</td><td>SC1</td><td>SC0</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EC15</td><td>EC14</td><td>EC13</td><td>EC12</td><td>EC11</td><td>EC10</td><td>EC9</td><td>EC8</td><td rowspan="2">Note1</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EC7</td><td>EC6</td><td>EC5</td><td>EC4</td><td>EC3</td><td>EC2</td><td>EC1</td><td>EC0</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command comes. Each value
represents one column line in the Frame Memory..
 

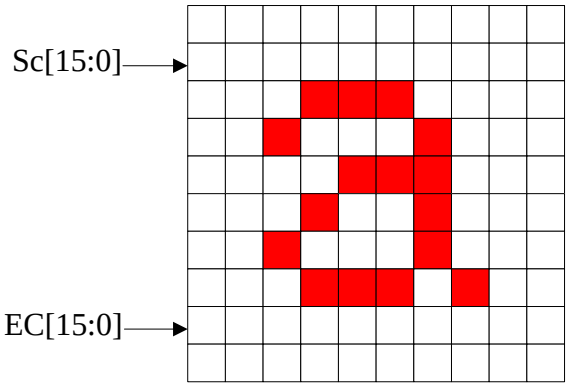
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">SC [15:0] always must be equal to or less than EC [15:0].
Note 1: When SC [15:0] or EC [15:0] is greater than 013Fh (When MADCTL’s B5 = 0) or 00EFh (When MADCTL’s B5 = 1), data of out of range will be ignored</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th colspan="2">Default Value</th></tr><tr><td>Power On Sequence</td><td>SC [15:0]=0000h</td><td>EC [15:0]=013Fh</td></tr></table></td></tr>
</table>

SW Reset	SC [15:0]=0000h	If MADCTL's B5 = 0: EC [15:0]=013Fh
		If MADCTL's B5 = 1: EC [15:0]=00EFh
HW Reset	SC [15:0]=0000h	EC [15:0]=00EFh

Flow Chart



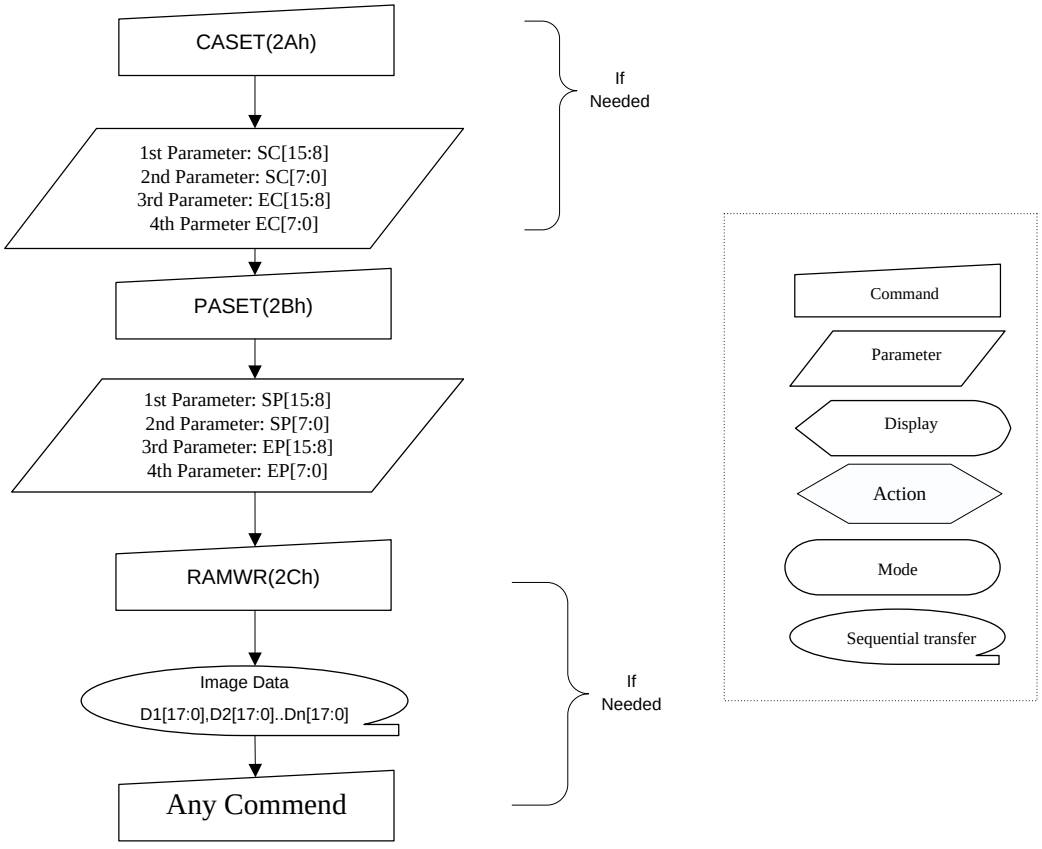
6.2.12. Row Address Set (2Bh)

<table>
<tr><td>2Bh</td><td colspan="13">Row Address Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>2Bh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SP15</td><td>SP14</td><td>SP13</td><td>SP12</td><td>SP11</td><td>SP10</td><td>SP9</td><td>SP8</td><td rowspan="2">Note1</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SP7</td><td>SP6</td><td>SP5</td><td>SP4</td><td>SP3</td><td>SP2</td><td>SP1</td><td>SP0</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EP15</td><td>EP14</td><td>EP13</td><td>EP12</td><td>EP11</td><td>EP10</td><td>EP9</td><td>EP8</td><td rowspan="2">Note1</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EP7</td><td>EP6</td><td>EP5</td><td>EP4</td><td>EP3</td><td>EP2</td><td>EP1</td><td>EP0</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to define area of frame memory where MCU can access. This command makes no change on the
other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each value
represents one Page line in the Frame Memory.
 

X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">SP [15:0] always must be equal to or less than EP [15:0]
Note 1: When SP [15:0] or EP [15:0] is greater than 00EFh (When MADCTL’s B5 = 0) or 013Fh (When MADCTL’s B5 = 1), data of out of range will be ignored.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"></td></tr>
</table>

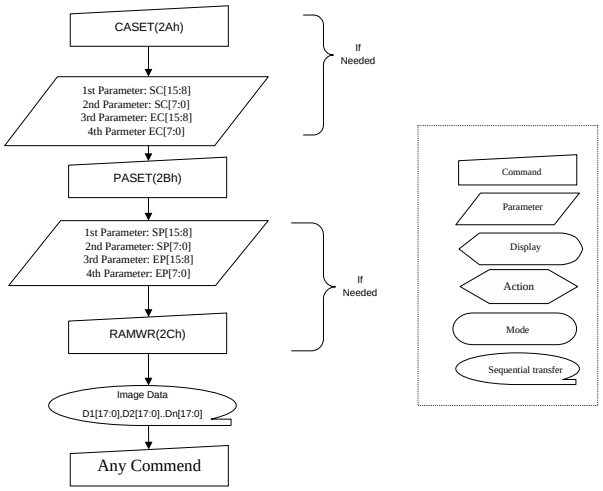
Status	Default Value	
Power On Sequence	SP [15:0]=0000h	EP [15:0]=00EFh
SW Reset	SP [15:0]=0000h	If MADCTL's B5 = 0: EP [15:0]=00EFh
		If MADCTL's B5 = 1: EP [15:0]=013Fh
HW Reset	SP [15:0]=0000h	EP [15:0]=00EFh

Flow Chart

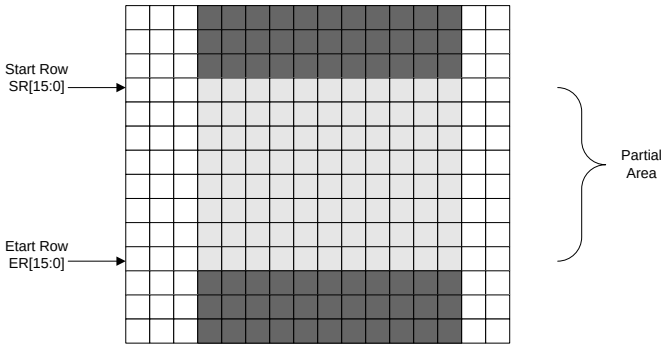
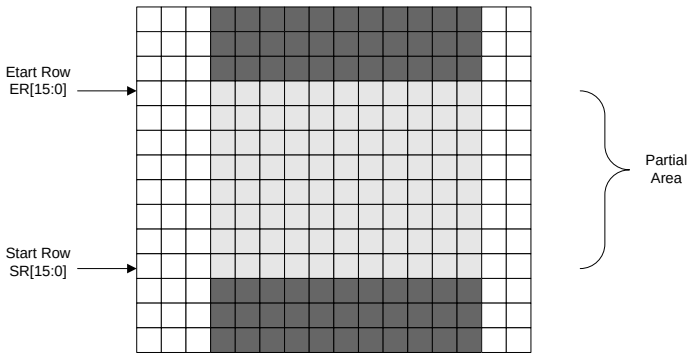


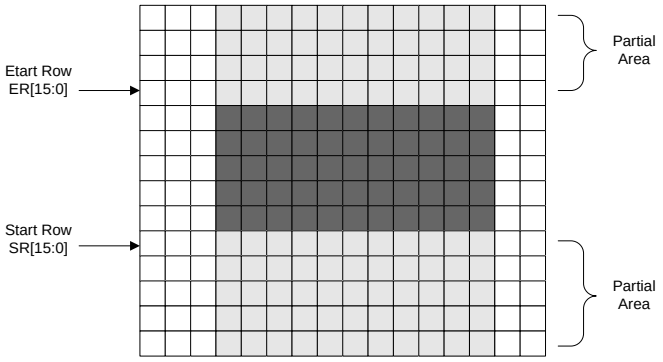
6.2.13. Memory Write (2Ch)

<table>
<tr><td>2Ch</td><td colspan="13">Memory Write</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>2Ch</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="9">D1 [17:0]</td><td>XX</td></tr>
<tr><td>:</td><td>1</td><td>1</td><td>↑</td><td colspan="9">Dx [17:0]</td><td>XX</td></tr>
<tr><td>Nth Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="9">Dn [17:0]</td><td>XX</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver
status. When this command is accepted, the column register and the page register are reset to the Start Column/Start
Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting.) Then D [17:0] isstored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write. X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">In all color modes, there is no restriction on length of parameters.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>SW Reset</td><td rowspan="2">Contents of memory is not cleared</td></tr><tr><td>HW Reset</td></tr></table></td></tr>
</table>

Flow Chart	 CASET(2Ah) 1st Parameter: SC[15:8] 2nd Parameter: SC[7:0] 3rd Parameter: EC[15:8] 4th Parmeter EC[7:0] If Needed PASET(2Bh) 1st Parameter: SP[15:8] 2nd Parameter: SP[7:0] 3rd Parameter: EP[15:8] 4th Parameter: EP[7:0] If Needed RAMWR(2Ch) Image Data D1[17:0],D2[17:0]..Dn[17:0] Any Commend Command Parameter Display Action Mode Sequential transfer

6.2.14. Partial Area (30h)

30h	Partial Area												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
1st Parameter	1	1	↑	XX	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00
2nd Parameter	1	1	↑	XX	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
3rd Parameter	1	1	↑	XX	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	00
4th Parameter	1	1	↑	XX	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	EF
Description	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row>Start Row when MADCTL B4=0:-  If End Row>Start Row when MADCTL B4=1:-  If End Row<Start Row when MADCTL B4=0:-												



If End Row = Start Row then the Partial Area will be one row deep.

X = Don't care.

Restriction	SR [15…0] and ER [15…0] cannot be 0000h nor exceed 013Fh.

Register Availability

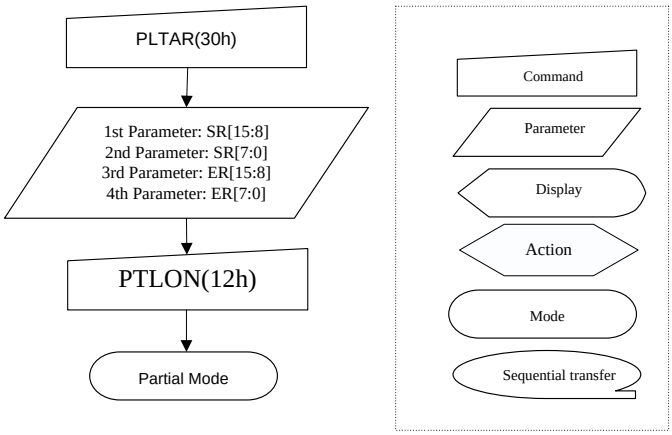
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

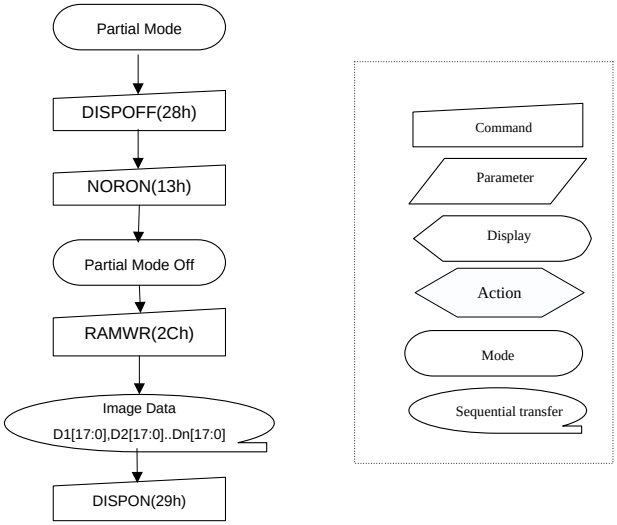
Status	Default Value	
	SR [15:0]	ER [15:0]
Power On Sequence	16'h0000h	16'h00EFh
SW Reset	16'h0000h	16'h00EF h
HW Reset	16'h0000h	16'h00EF h

Flow Chart

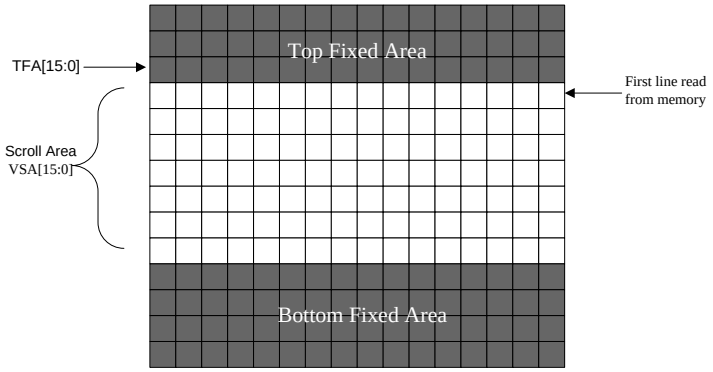
1. To Enter Partial Mode

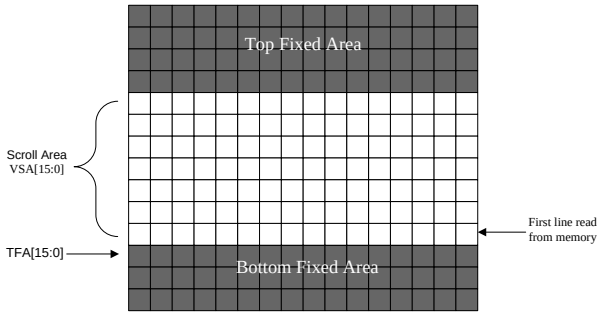


2. To Leave Partial Mode



6.2.15. Vertical Scrolling Definition (33h)

33h	Vertical Scrolling Definition												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
1st Parameter	1	1	↑	XX	TFA [15:8]								00
2nd Parameter	1	1	↑	XX	TFA [7:0]								00
3rd Parameter	1	1	↑	XX	VSA [15:8]								00
4th Parameter	1	1	↑	XX	VSA [7:0]								F0
Description	This command defines the Vertical Scrolling Area of the display. When MADCTL B4=0 The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display). The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.  When MADCTL B4=1 The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.												



X = Don’t care.

Restriction

Register Availability

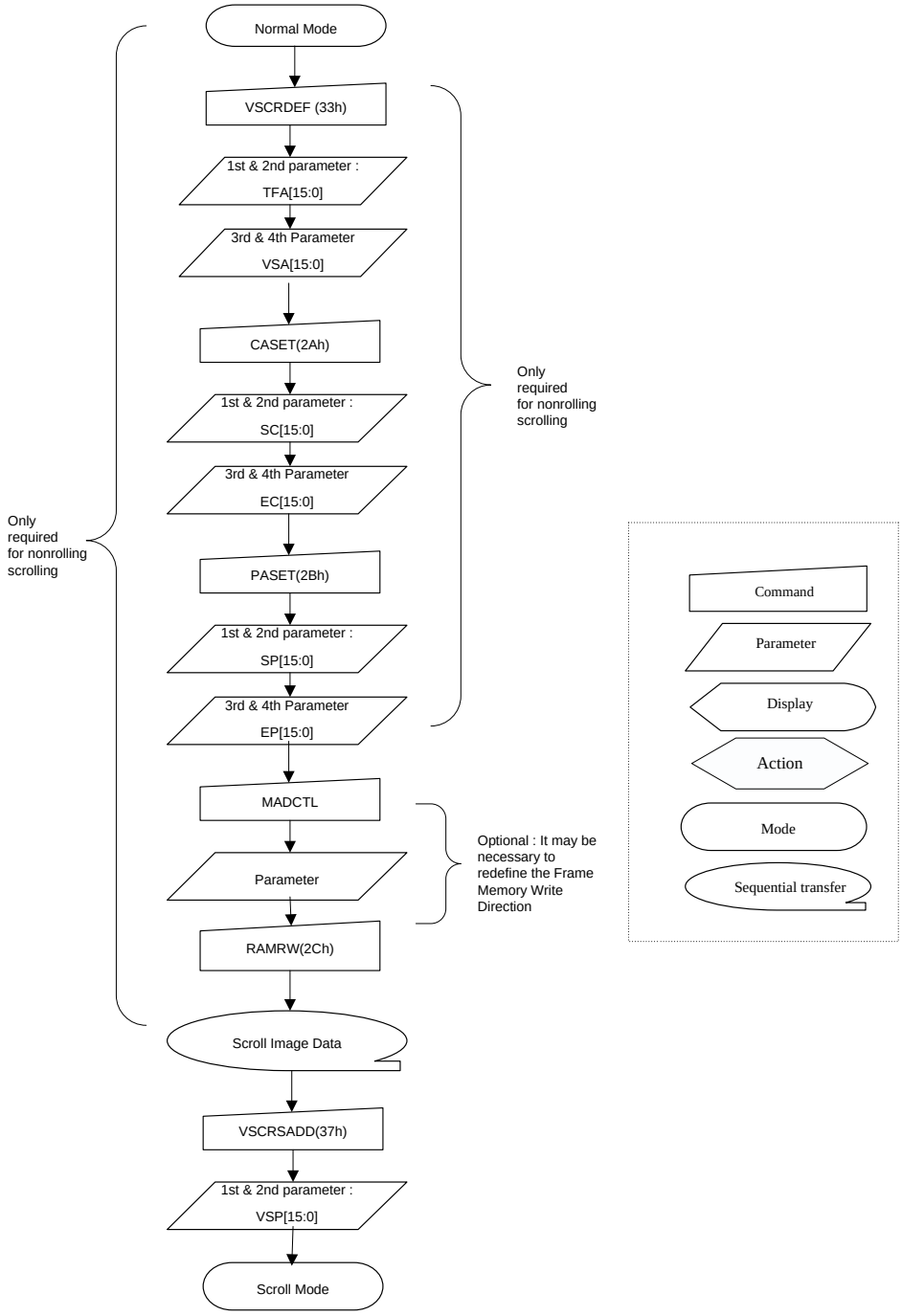
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	TFA [15:0]	VSA [15:0]
Power On Sequence	16’h0000h	16’h00F0h
SW Reset	16’h0000h	16’h00F 0h
HW Reset	16’h0000h	16’h00F 0h

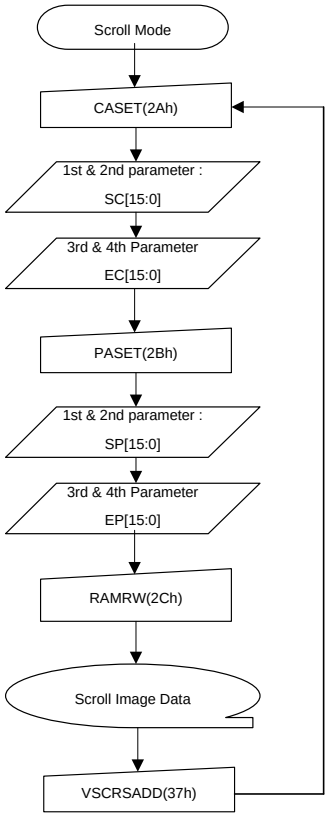
Flow Chart

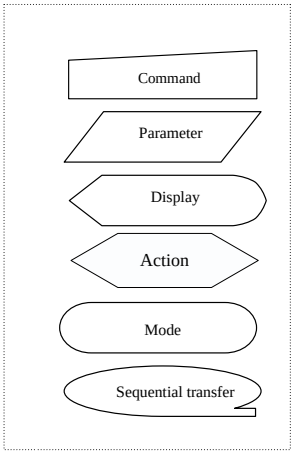
1. To enter Vertical Scroll Mode :



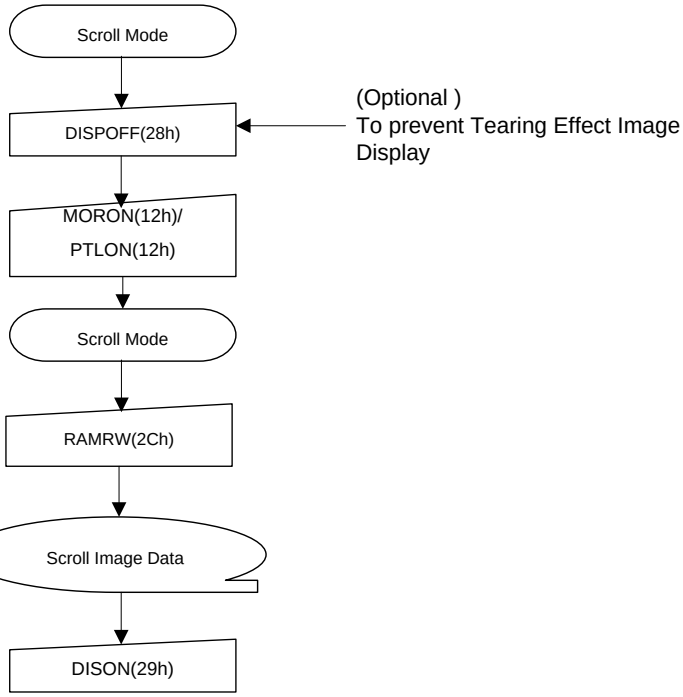
Note : The Frame Memory Window size ,must be defined correctly otherwise undesirable image will be displayed.

2.Continuous Scroll :



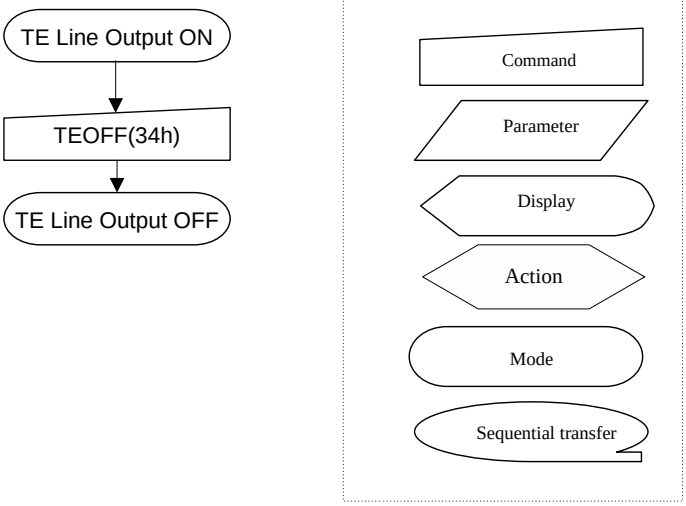


3.To Leave Vertical Scroll Mode:



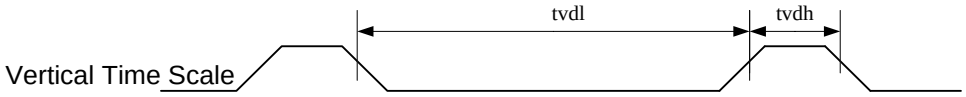
Note: Scroll Mode can be left by both the Normal Display Mode ON (13h) and Partial Mode ON (12h) commands.

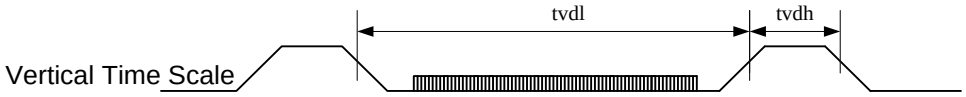
6.2.16. Tearing Effect Line OFF (34h)

<table>
<tr><td>34h</td><td colspan="13">Tearing Effect Line OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>34h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already OFF.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

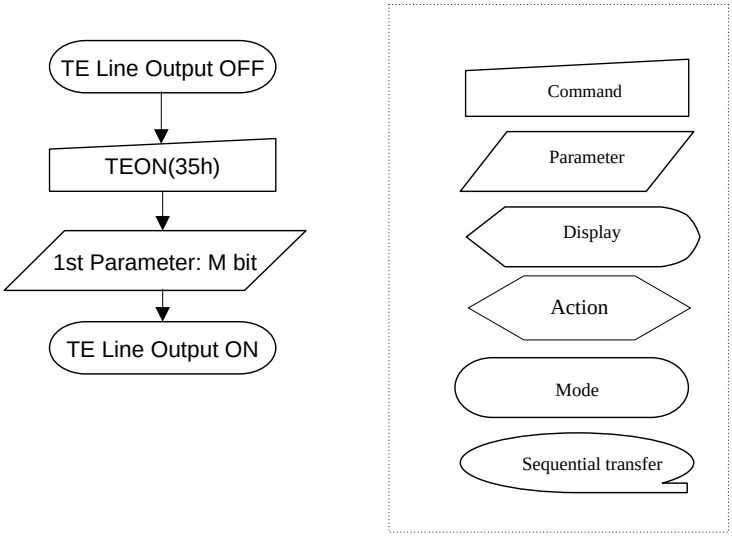
6.2.17. Tearing Effect Line ON (35h)

<table>
<tr><td>35h</td><td colspan="13">Tearing Effect Line ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>35h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>M</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by
changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

When M=0:
The Tearing Effect Output line consists of V-Blanking information only:
 

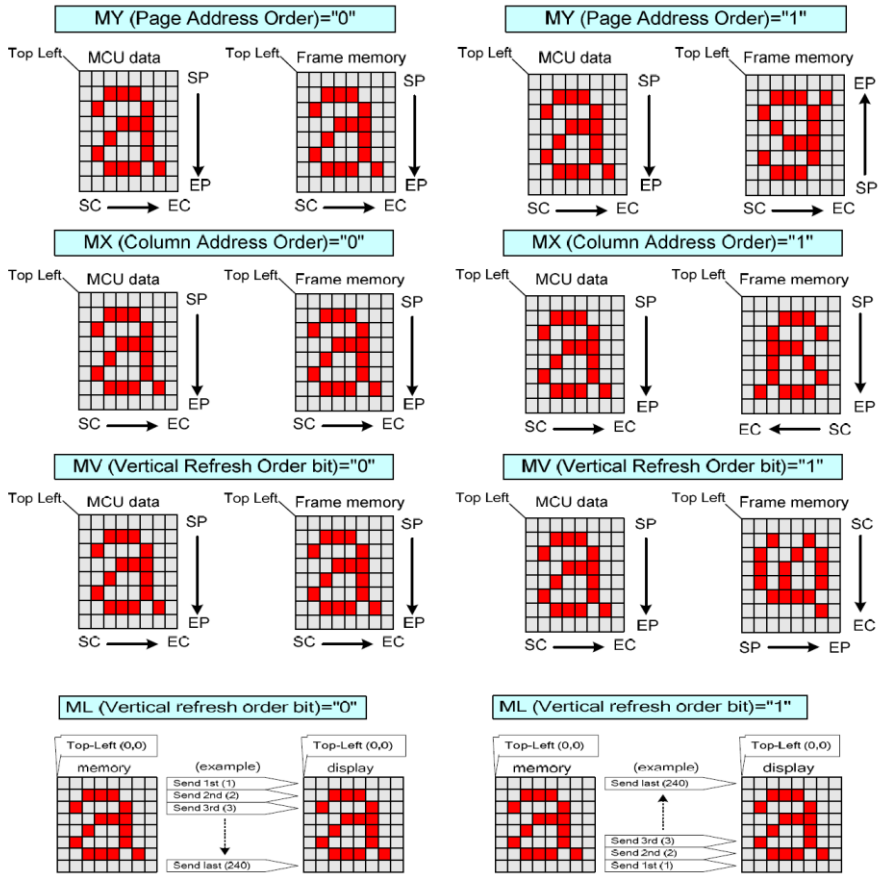
When M=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:
 

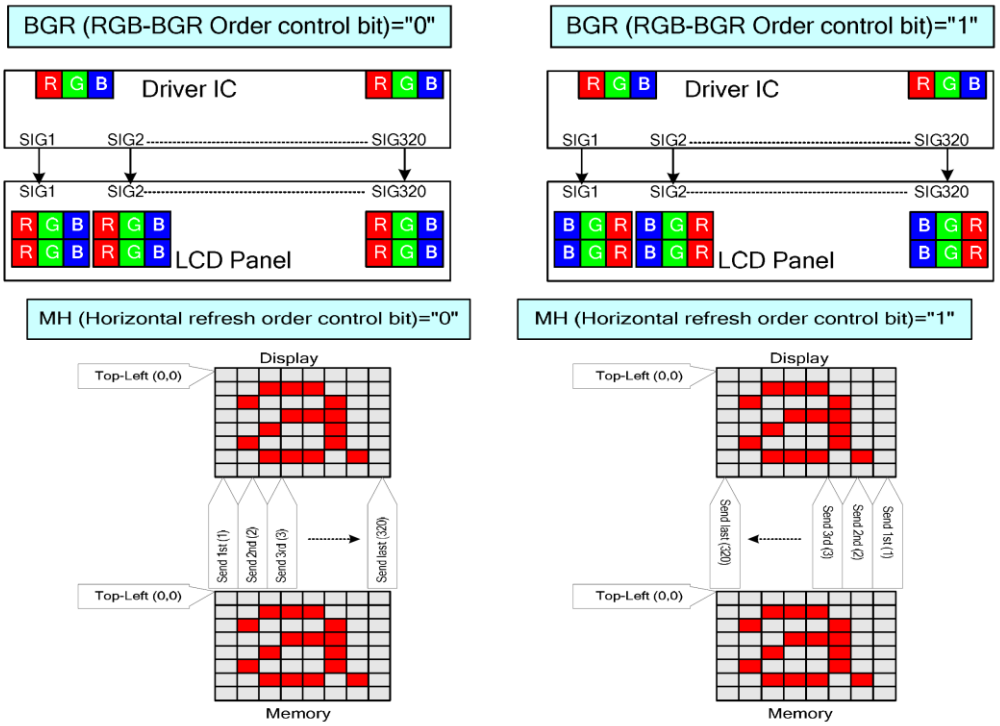
Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already ON</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table></td></tr>
</table>

Flow Chart	

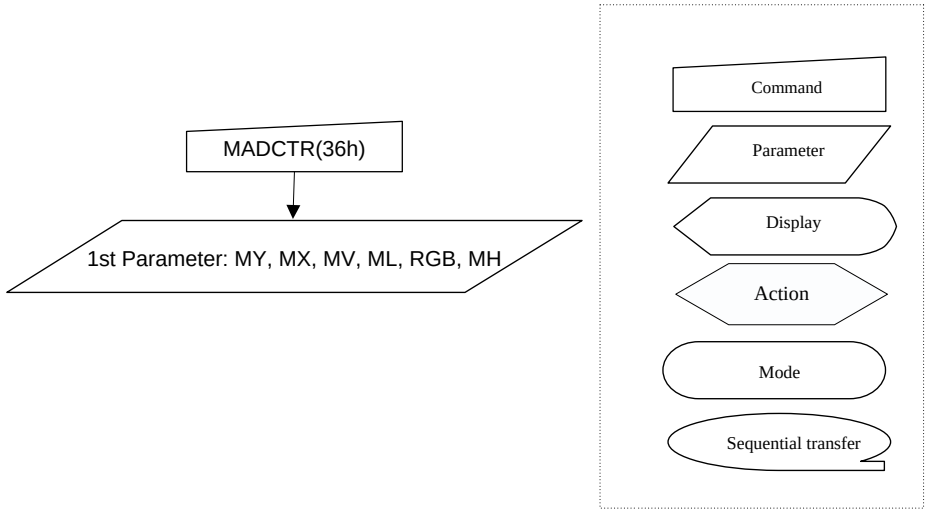
TE Line Output OFF
TEON(35h)
1st Parameter: M bit
TE Line Output ON
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.18. Memory Access Control(36h)

<table>
<tr><td>36h</td><td colspan="12">Tearing Effect Line ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>36h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>MY</td><td>MX</td><td>MV</td><td>ML</td><td>BGR</td><td>MH</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="12">This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.
<table><tr><th>Bit</th><th>Name</th><th>Description</th></tr><tr><td>MY</td><td>Row Address Order</td><td rowspan="3">These 3 bits control MCU to memory write/read direction.</td></tr><tr><td>MX</td><td>Column Address Order</td></tr><tr><td>MV</td><td>Row / Column Exchange</td></tr><tr><td>ML</td><td>Vertical Refresh Order</td><td>LCD vertical refresh direction control.</td></tr><tr><td>BGR</td><td>RGB-BGR Order</td><td>Color selector switch control
(0=RGB color filter panel, 1=BGR color filter panel)</td></tr><tr><td>MH</td><td>Horizontal Refresh ORDER</td><td>LCD horizontal refreshing direction control.</td></tr></table>Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.
 
</td></tr>
</table>

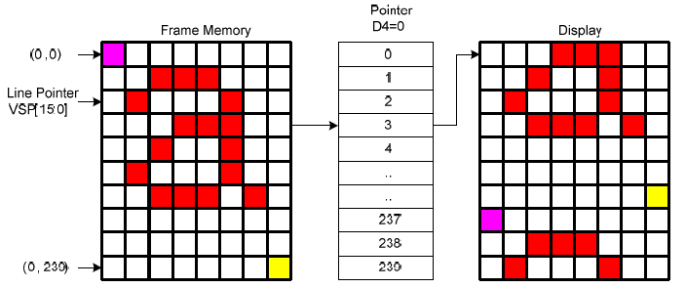
<table>
<tr><td></td><td>


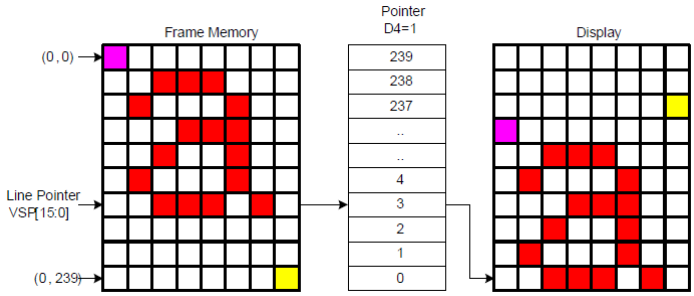
Note: Top-Left (0,0) means a physical memory location.
</td></tr>
<tr><td>Restriction</td><td>This command has no effect when Tearing Effect output is already ON</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00h</td></tr>
<tr><td>SW Reset</td><td>No change</td></tr>
<tr><td>HW Reset</td><td>8’h00h</td></tr>
</table>
</td></tr>
</table>

Flow Chart	

MADCTR(36h)
1st Parameter: MY, MX, MV, ML, RGB, MH
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.19. Vertical Scrolling Start Address (37h)

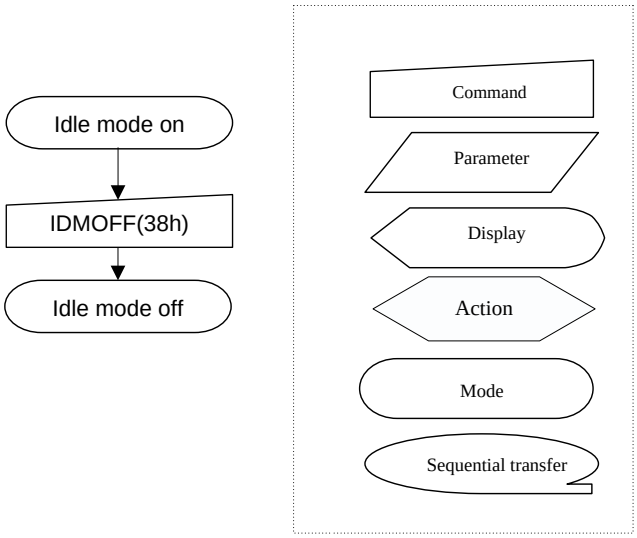
<table>
<tr><td>37h</td><td colspan="12">VSCRSADD (Vertical Scrolling Start Address)</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>37h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">VSP [15:8]</td><td>00</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">VSP [7:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="12">This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area
and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-
When MADCTL B4=0
Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 240 and VSP=’3’.
 

When MADCTL B4=1
Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 240 and VSP=’3’.
 

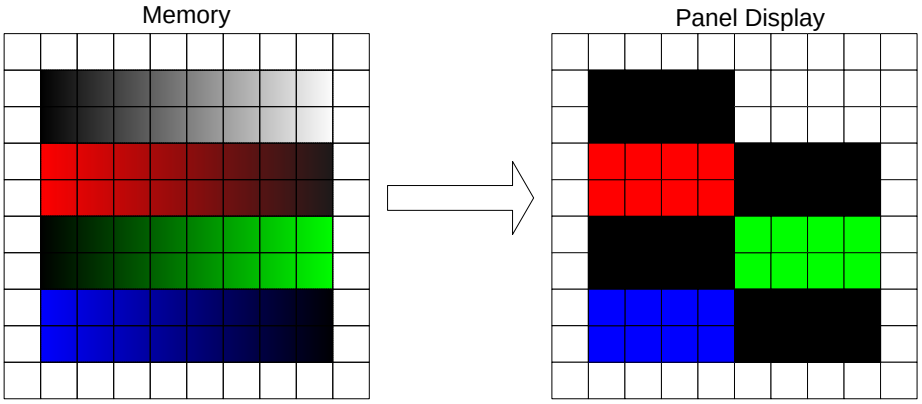
Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.
(2) This command is ignored when the GC9A01 enters Partial mode.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when Tearing Effect output is already ON</td></tr>
</table>

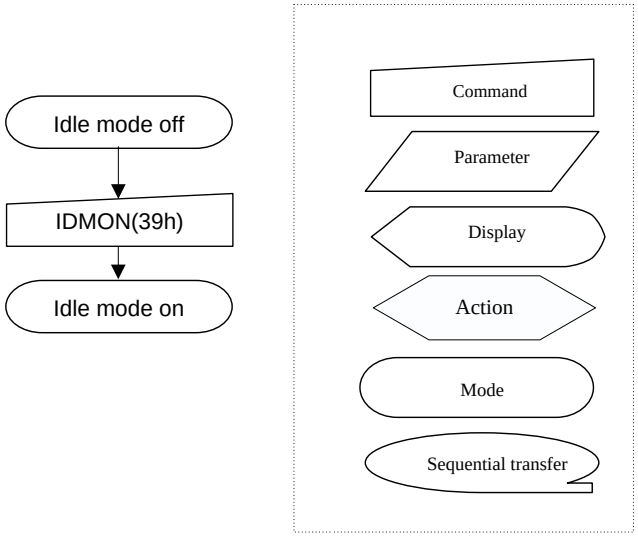
<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VSP [15:0]</th></tr>
<tr><td>Power On Sequence</td><td>16’h0000h</td></tr>
<tr><td>SW Reset</td><td>16’h0000h</td></tr>
<tr><td>HW Reset</td><td>16’h0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

6.2.20. Idle Mode OFF (38h)

<table>
<tr><td>38h</td><td colspan="13">Idle Mode OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>38h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from Idle mode on.
In the idle off mode, LCD can display maximum 262,144 colors.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle mode OFF</td></tr><tr><td>SW Reset</td><td>Idle mode OFF</td></tr><tr><td>HW Reset</td><td>Idle mode OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

6.2.21. Idle Mode ON (39h)

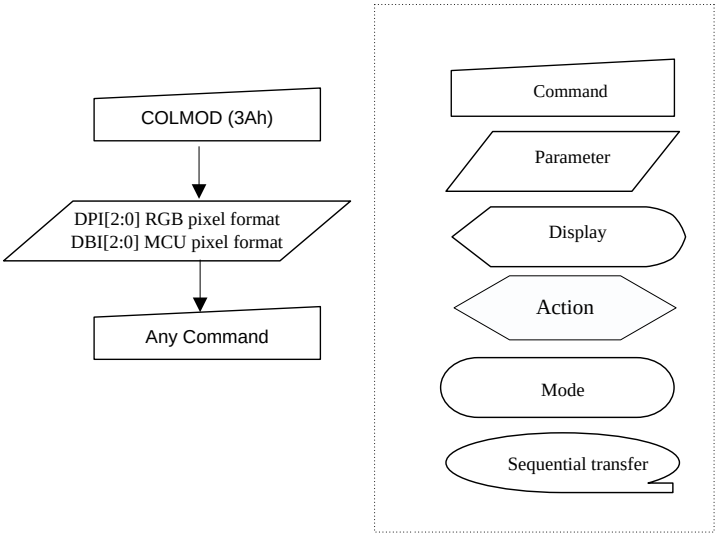
<table>
<tr><td>39h</td><td colspan="13">Idle Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>39h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to enter into Idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.
 
<table><tr><td></td><td colspan="3">Memory Contents vs. Display Color</td></tr><tr><td></td><td>R5 R4 R3 R2 R1 R0</td><td>G5 G4 G3 G2 G1 G0</td><td>B5 B4 B3 B2 B1 B0</td></tr><tr><td>Black</td><td>0XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr><tr><td>Blue</td><td>0XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr><tr><td>Red</td><td>1XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr><tr><td>Magenta</td><td>1XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr><tr><td>Green</td><td>0XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr><tr><td>Cyan</td><td>0XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr><tr><td>Yellow</td><td>1XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr><tr><td>White</td><td>1XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr></table>X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

<table>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Idle mode OFF</td></tr>
<tr><td>SW Reset</td><td>Idle mode OFF</td></tr>
<tr><td>HW Reset</td><td>Idle mode OFF</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>


</td></tr>
</table>

6.2.22. COLMOD: Pixel Format Set (3Ah)

<table>
<tr><td>3Ah</td><td colspan="13">Pixel Format Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3Ah</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td colspan="3">DPI [2:0]</td><td>0</td><td colspan="3">DBI [2:0]</td><td>66</td></tr>
<tr><td>Description</td><td colspan="13">This command sets the pixel format for the RGB image data used by the interface. DPI [2:0] is the pixel format select of RGB interface and DBI [2:0] is the pixel format of MCU interface. If a particular interface, either RGB interface or MCU interface, is not used then the corresponding bits in the parameter are ignored. The pixel format is shown in the table below.
<table>
<tr><th colspan="3">DPI [2:0]</th><th>RGB Interface Format</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table>
<table>
<tr><th colspan="3">DBI [2:0]</th><th>MCU Interface Format</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>12 bits / pixel</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table>
If using RGB Interface must selection serial interface.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>DPI [2:0]</th><th>DBI [2:0]</th></tr>
<tr><td>Power On Sequence</td><td>3’b110</td><td>3’b110</td></tr>
<tr><td>SW Reset</td><td>No Change</td><td>No Change</td></tr>
<tr><td>HW Reset</td><td>3’b110</td><td>3’b110</td></tr>
</table>
</td></tr>
</table>

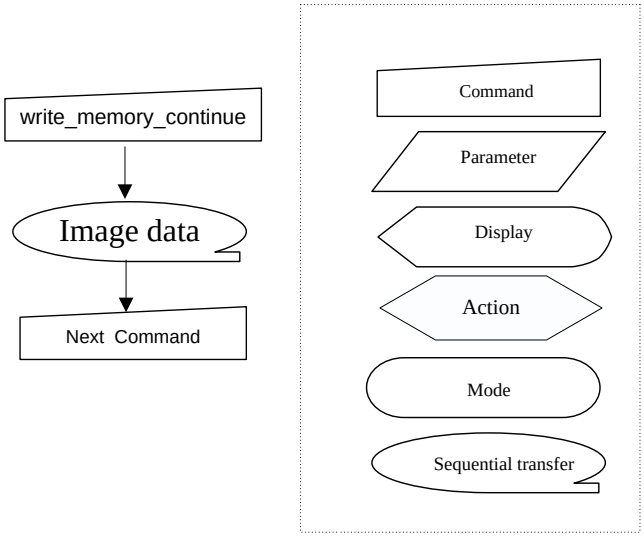
Flow Chart	

COLMOD (3Ah)
DPI[2:0] RGB pixel format
DBI[2:0] MCU pixel format
Any Command
Command
Parameter
Display
Action
Mode
Sequential transfer

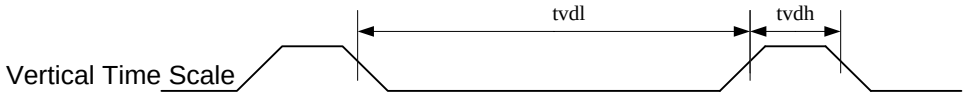
6.2.23. Write Memory Contiue (3Ch)

3Ch	write_memory_continue												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	D1[17..8]	0	0	1	1	1	1	0	0	3Ch
1st Parameter	1	1	↑	Dx[17..8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	0003FF
Xth Parameter	1	1	↑	D1[17..8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	0003FF
Nth Parameter	1	1	↑	Dn[17..8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	0003FF
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. **If set_address_mode B5 = 0:** Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC –SC + 1) * (EP – SP + 1) the extra pixels are ignored. **If set_address_mode B5 = 1:** Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP –SP + 1) the extra pixels are ignored. Sending any other command can stop frame Write. Frame Memory Access and Interface setting (B3h), WEMODE=0 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored. Frame Memory Access and Interface setting (B3h), WEMODE=1												

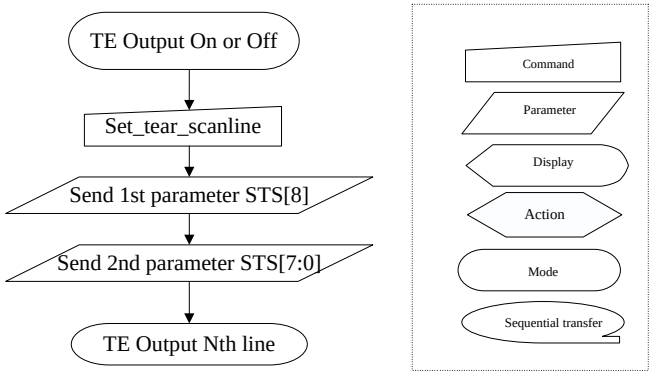
	When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.
Restriction	A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Random value</td></tr>
<tr><td>SW Reset</td><td>No change</td></tr>
<tr><td>HW Reset</td><td>No change</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

6.2.24. Set_Tear_Scanline (44h)

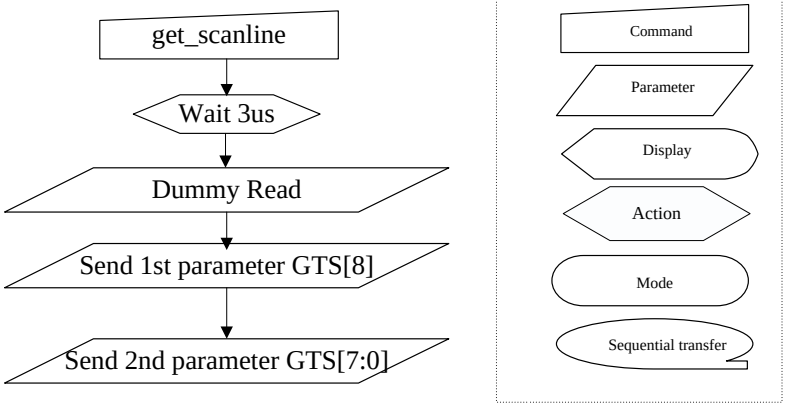
<table>
<tr><td>44h</td><td colspan="13">Set_Tear_Scanline</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>44h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>STS [8]</td><td>00</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>STS [7]</td><td>STS [6]</td><td>STS [5]</td><td>STS [4]</td><td>STS [3]</td><td>STS [2]</td><td>STS [1]</td><td>STS [0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line equal the value of STS[8:0]
 

Note:that set_tear_scanline with STS is equivalent to set_tear_on with 8+GateN(N=1、2、3...240)
eg:when the STS[8:0]=8,the TE will output at the position of Gate1.
when the STS[8:0]=9,the TE will output at the position of Gate2.
when the STS[8:0]=10,the TE will output at the position of Gate3.
…….
The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>STS [8:0]=0000h</td></tr><tr><td>SW Reset</td><td>STS [8:0]=0000h</td></tr><tr><td>HW Reset</td><td>STS [8:0]=0000h</td></tr></table></td></tr>
</table>

Flow Chart	

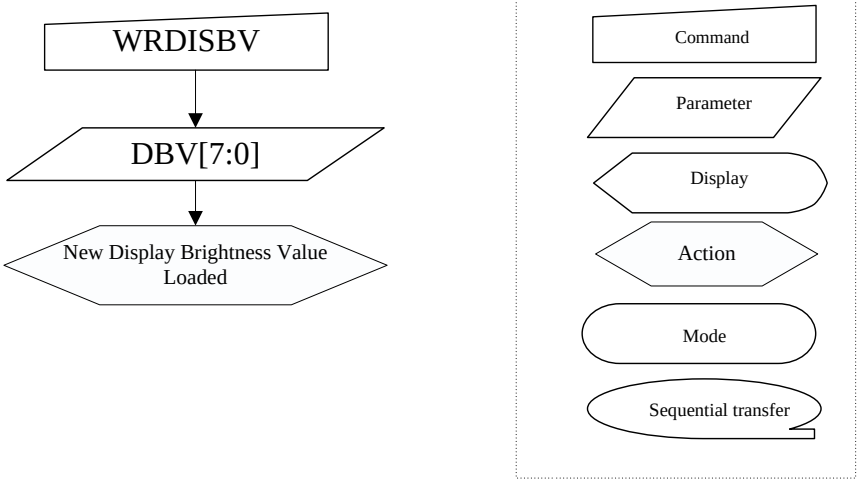
TE Output On or Off
Set_tear_scanline
Send 1st parameter STS[8]
Send 2nd parameter STS[7:0]
TE Output Nth line
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.25. Get_Scanline (45h)

<table>
<tr><td>45h</td><td colspan="13">Get_Scanline</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>45h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>GTS [8]</td><td>00</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>GTS [7]</td><td>GTS [6]</td><td>GTS [5]</td><td>GTS [4]</td><td>GTS [3]</td><td>GTS [2]</td><td>GTS [1]</td><td>GTS [0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command returns the setting value of STS[8:0] .
When in Sleep Mode, the value returned by get_scanline is undefined.</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>GTS [9:0]=0000h</td></tr><tr><td>SW Reset</td><td>GTS [9:0]=0000h</td></tr><tr><td>HW Reset</td><td>GTS [9:0]=0000h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

6.2.26. Write Display Brightness (51h)

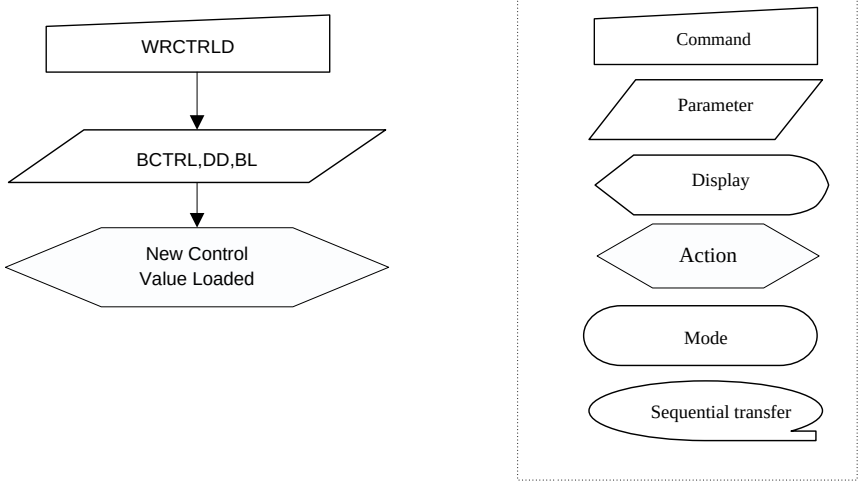
<table>
<tr><td>51h</td><td colspan="13">Write Display Brightness</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>51h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>DBV[7]</td><td>DBV[6]</td><td>DBV[5]</td><td>DBV[4]</td><td>DBV[3]</td><td>DBV[6]</td><td>DBV[5]</td><td>DBV[4]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to adjust the brightness value of the display.
It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification.
In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>DBV [7:0]= 8’h00</td></tr><tr><td>SW Reset</td><td>DBV [7:0]= 8’h00</td></tr><tr><td>HW Reset</td><td>DBV [7:0]= 8’h00</td></tr></table></td></tr>
</table>

Flow Chart	

WRDISBV
DBV[7:0]
New Display Brightness Value Loaded
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.27. Write CTRL Display (53h)

<table>
<tr><td>53h</td><td colspan="13">Write CTRL Display</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>53h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>BCTRL</td><td>0</td><td>DD</td><td>BL</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to return brightness setting.
BCTRL: Brightness Control Block On/Off,
‘0’ = Off (Brightness registers are 00h)
‘1’ = On (Brightness registers are active, according to the DBV[7..0] parameters.)
DD: Display Dimming
‘0’ = Display Dimming is off
‘1’ = Display Dimming is on
BL: Backlight On/Off
‘0’ = Off (Completely turn off backlight circuit. Control lines must be low.)
‘1’ = On</td></tr>
<tr><td>Restriction</td><td colspan="13">The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter
(= more than 2 RDX cycle) on DBI.
Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>BCTRL</th><th>DD</th><th>BL</th></tr><tr><td>Power On Sequence</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr><tr><td>SW Reset</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr><tr><td>HW Reset</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr></table></td></tr>
</table>

Flow Chart	

WRCTRLD
BCTRL,DD,BL
New Control
Value Loaded
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.28. Read ID1 (DAh)

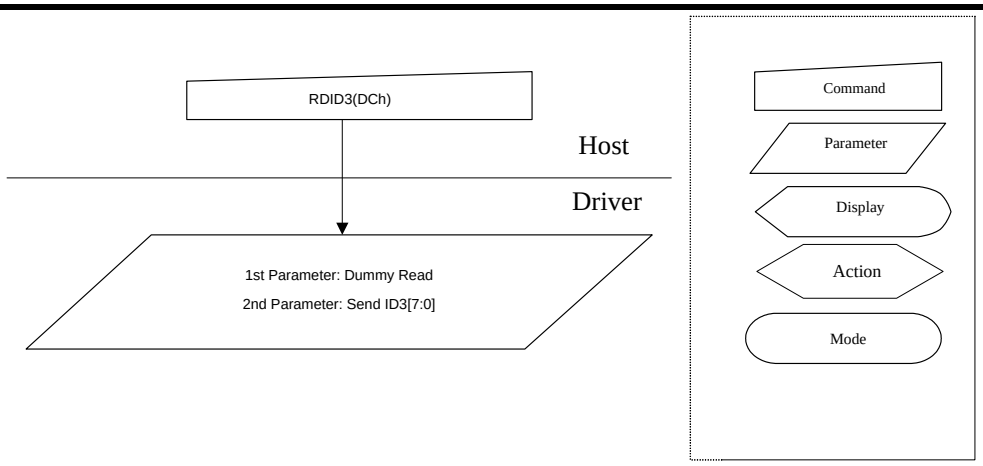
DCh	Read ID2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID3 [7:0]								Program value
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID The ID3 can be programmed by MTP function. X = Don't care												
Restriction	None												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

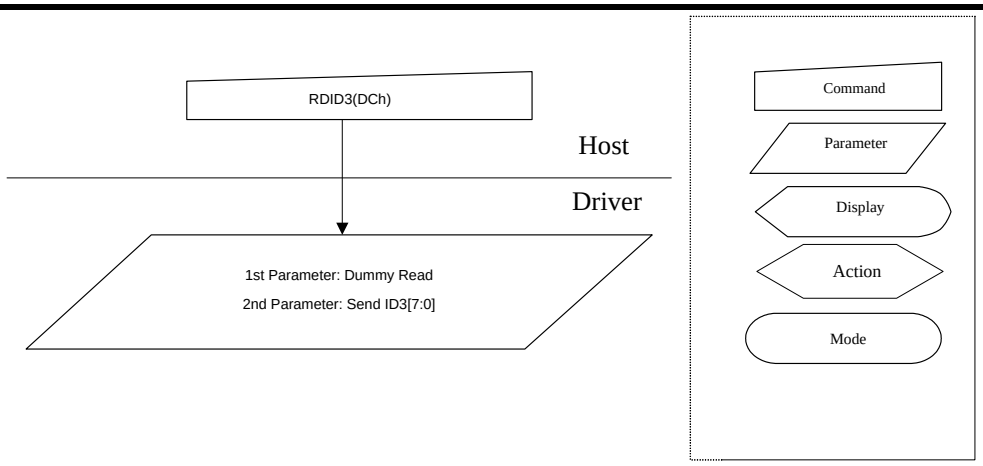
Default

Status	Default Value (After MTP program)
Power On Sequence	8'h00
SW Reset	8'h00
HW Reset	8'h00

Flow Chart	 RDID3(DCh) Host Driver 1st Parameter: Dummy Read 2nd Parameter: Send ID3[7:0] Command Parameter Display Action Mode

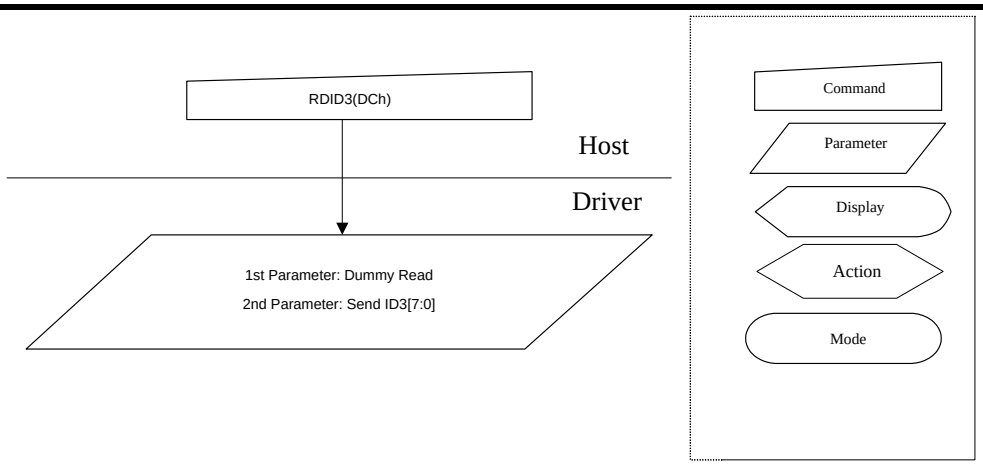
6.2.29. Read ID2 (DBh)

<table>
<tr><td>DCh</td><td colspan="13">Read ID2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>DBh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID3 [7:0]</td><td>Program value</td></tr>
<tr><td>Description</td><td colspan="13">This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User’s agreement) and changes each time a revision is made to the display, material or construction specifications.
The 1st parameter is dummy data.
The 2nd parameter is LCD module/driver version ID
The ID3 can be programmed by MTP function.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value (After MTP program)</th></tr><tr><td>Power On Sequence</td><td>8’h9A</td></tr><tr><td>SW Reset</td><td>8’h9A</td></tr><tr><td>HW Reset</td><td>8’h9A</td></tr></table></td></tr>
</table>

Flow Chart	 RDID3(DCh) Host Driver 1st Parameter: Dummy Read 2nd Parameter: Send ID3[7:0] Command Parameter Display Action Mode

6.2.30. Read ID3 (DCh)

<table>
<tr><td>DCh</td><td colspan="13">Read ID2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>DCh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID3 [7:0]</td><td>Program value</td></tr>
<tr><td>Description</td><td colspan="13">This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User’s agreement) and changes each time a revision is made to the display, material or construction specifications.
The 1st parameter is dummy data.
The 2nd parameter is LCD module/driver version ID
The ID3 can be programmed by MTP function.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value (After MTP program)</th></tr><tr><td>Power On Sequence</td><td>8’h01</td></tr><tr><td>SW Reset</td><td>8’h01</td></tr><tr><td>HW Reset</td><td>8’h01</td></tr></table></td></tr>
</table>

Flow Chart	 RDID3(DCh) Host Driver 1st Parameter: Dummy Read 2nd Parameter: Send ID3[7:0] Command Parameter Display Action Mode

6.3. Description of Level 2 Command

6.3.1. RGB Interface Signal Control (B0h)

<table>
<tr><td>B0h</td><td colspan="14">RGB Interface Signal Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B0h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>RCM[1]</td><td>RCM[0]</td><td>0</td><td>VSPL</td><td>HSPL</td><td>DPL</td><td>EPL</td><td>01</td></tr>
<tr><td>Description</td><td colspan="14">Sets the operation status of the display interface. The setting becomes effective as soon as the command is received.
EPL: DE polarity (“0”= High enable for RGB interface, “1”= Low enable for RGB interface)
DPL: DOTCLK polarity set (“0”= data fetched at the rising time, “1”= data fetched at the falling time)
HSPL: HSYNC polarity (“0”= Low level sync clock, “1”= High level sync clock)
VSPL: VSYNC polarity (“0”= Low level sync clock, “1”= High level sync clock)
RCM [1:0]: RGB interface selection (refer to the RGB interface section).
<table>
<tr><th colspan="2">RCM[1:0]</th><th>RIM</th><th colspan="3">DPI[1:0]</th><th>RGB interface Mode</th><th>RGB Mode</th><th>Used Pins</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>18-bit RGB interface (262K colors)</td><td rowspan="3">DE Mode
Valid data is determined by the DE signal</td><td>VSYNC,HSYNC,DE, DOTCLK,D[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>16-bit RGB interface (65K colors)</td><td>VSYNC,HSYNC,DE, DOTCLK,D[17:13] & D[11:1]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td colspan="3">-</td><td>6-bit RGB interface (262K colors)</td><td>VSYNC,HSYNC,DE, DOTCLK,D[5:0]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>18-bit RGB interface (262K colors)</td><td rowspan="3">SYNC Mode In SYNC mode, DE signal is ignored; blanking porch is determined by B5h command</td><td>VSYNC,HSYNC,DOTCLK, D[17:0]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>16-bit RGB interface (65K colors)</td><td>VSYNC,HSYNC,DOTCLK, D[17:13] & D[11:1]</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td colspan="3">-</td><td>6-bit RGB interface (262K colors)</td><td>VSYNC,HSYNC,DOTCLK, D[5:0]</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="14"></td></tr>
</table>

Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	RCM[1:0]	VSPL	HSPL	DPL	EPL
Power On Sequence	2'b00	1'b0	1'b0	1'b0	1'b1
SW Reset	2'b00	1'b0	1'b0	1'b0	1'b1
HW Reset	2'b00	1'b0	1'b0	1'b0	1'b1

HBP [4:0]	Number of HSYNC of f ont/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31
11111	32
HBP [4:0]	Number of HSYNC of f ont/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31

11111	32
HBP [4:0]	Number of HSYNC of f ont/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31
11111	32
HBP [4:0]	Number of HSYNC of f ont/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31
11111	32

6.3.2. Blanking Porch Control (B5h)

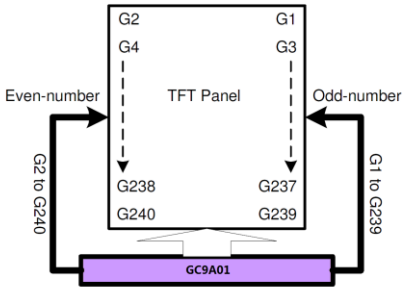
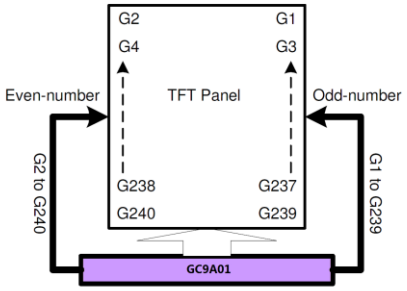
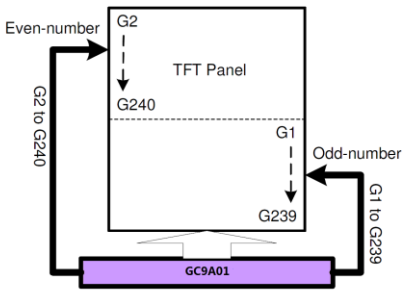
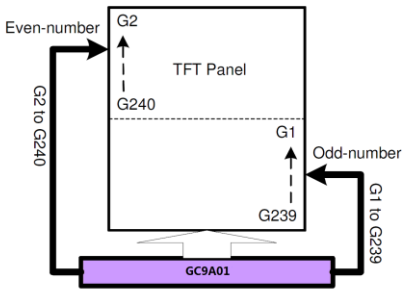
<table>
<tr><td>B5h</td><td colspan="13">Blanking Porch Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>B5h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">VFP [7:0]</td><td>08</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td colspan="7">VBP [6:0]</td><td>08</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td colspan="5">HBP [4:0]</td><td>14</td></tr>
<tr><td>Description</td><td colspan="13">
Note:The Third parameter must write,but it is not valid.
VFP [6:0] / VBP [6:0]: The VFP [6:0] and VBP [6:0] bits specify the line number of vertical front and back porch period respectively.
<table>
<tr><th>VFP [6:0]
VBP [6:0]</th><th>Number of HSYNC of front/back porch</th><th>VFP [6:0]
VBP [6:0]</th><th>Number of HSYNC of front/back porch</th></tr>
<tr><td>0000000</td><td>Setting inhibited</td><td>1000000</td><td>64</td></tr>
<tr><td>0000001</td><td>Setting inhibited</td><td>1000001</td><td>65</td></tr>
<tr><td>0000010</td><td>2</td><td>1000010</td><td>66</td></tr>
<tr><td>0000011</td><td>3</td><td>1000011</td><td>67</td></tr>
<tr><td>0000100</td><td>4</td><td>1000100</td><td>68</td></tr>
<tr><td>0000101</td><td>5</td><td>1000101</td><td>69</td></tr>
<tr><td>:
:</td><td>:
:</td><td>:
:</td><td>:
:</td></tr>
<tr><td>0111101</td><td>61</td><td>1111101</td><td>125</td></tr>
<tr><td>0111110</td><td>62</td><td>1111110</td><td>109.5</td></tr>
<tr><td>0111111</td><td>63</td><td>1111111</td><td>127</td></tr>
</table>
Note: VFP + VBP ≦ 254 HSYNC signals
HBP [4:0]: HBP [4:0] bits specify the line number of horizontal back porch period respectively.
<table>
<tr><th>HBP [4:0]</th><th>Number of HSYNC of f ont/back porch</th></tr>
<tr><td>00000</td><td>Setting inhibited</td></tr>
<tr><td>00001</td><td>Setting inhibited</td></tr>
<tr><td>00010</td><td>2</td></tr>
<tr><td>00011</td><td>3</td></tr>
<tr><td>00100</td><td>4</td></tr>
<tr><td>00101</td><td>5</td></tr>
<tr><td>:
:</td><td>:
:</td></tr>
<tr><td>11101</td><td>30</td></tr>
<tr><td>11110</td><td>31</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><td></td><td>
<table>
<tr><td>11111</td><td>32</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td>EXTC should be high to enable this command</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>VFP [6:0]</th><th>VBP [6:0]</th><th>HBP [4:0]</th></tr>
<tr><td>Power On Sequence</td><td>7’h08</td><td>7’h08</td><td>5’h14</td></tr>
<tr><td>SW Reset</td><td>7’h08</td><td>7’h08</td><td>5’h14</td></tr>
<tr><td>HW Reset</td><td>7’h08</td><td>7’h08</td><td>5’h14</td></tr>
</table>
</td></tr>
</table>

6.3.3. Display Function Control (B6h)

<table>
<tr><td>B6h</td><td colspan="13">Display Function Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>B6h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>GS</td><td>SS</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">
note:the first parameter must write,but it is not valid.
SS: Select the shift direction of outputs from the source driver.
<table>
<tr><th>SS</th><th>Sourc Output Scan Direction</th></tr>
<tr><td>0</td><td>S1 → S360</td></tr>
<tr><td>1</td><td>S360 → S1</td></tr>
</table>
In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, and B dots to the source driver pins.
To assign R, G, B dots to the source driver pins from S1 to S360, set SS = 0.
To assign R, G, B dots to the source driver pins from S360 to S1, set SS = 1.

GS: Sets the direction of scan by the gate driver in the range determined by SCN [4:0] and NL [4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.
<table>
<tr><th>GS</th><th>Gate Output Scan Direction</th></tr>
<tr><td>0</td><td>G1→G240</td></tr>
<tr><td>1</td><td>G240→G1</td></tr>
</table>
SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module
</td></tr>
</table>

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1→G2→G3→G4→ …… ….→G237→G238→G239→G240
0	1		G240→G239->G238→G237→…… …. →G4→G3→G2→G1
1	0		G1→G3→……..→G237→G239→ G2→G4→……→G238→G240
1	1		G240→G238→……..→G4→G2→ G239→G237→……→G3→G1

NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected
by the number of lines set by NL [5:0]. The number of lines must be the same or more than the number of lines necessary
for the size of the liquid crystal panel.

NL [5:0]						LCD Drive Line
0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	1	16 lines
0	0	0	0	1	0	24 lines
0	0	0	0	1	1	32 lines

NL [5:0]						LCD Drive Line
0	1	0	1	0	1	176 lines
0	1	0	1	1	0	184 lines
0	1	0	1	1	1	192 lines
0	1	1	0	0	0	200 lines

		0	0	0	1	0	0	40 lines		0	1	1	0	0	1	208 lines
		0	0	0	1	0	1	48 lines		0	1	1	0	1	0	216 lines
		0	0	0	1	1	0	56 lines		0	1	1	0	1	1	224 lines
		0	0	0	1	1	1	64 lines		0	1	1	1	0	0	232 lines
		0	0	1	0	0	0	72 lines		0	1	1	1	0	1	240 lines
		0	0	1	0	0	1	80 lines		Others						Setting prohibited
		0	0	1	0	1	0	88 lines								
		0	0	1	0	1	1	96 lines								
		0	0	1	1	0	0	104 lines								
		0	0	1	1	0	1	112 lines								
		0	0	1	1	1	0	120 lines								
		0	0	1	1	1	1	128 lines								
		0	1	0	0	0	0	136 lines								
		0	1	0	0	0	1	144 lines								
		0	1	0	0	1	0	152 lines								
		0	1	0	0	1	1	160 lines								

Restriction	EXTC should be high to enable this command

Register Availability

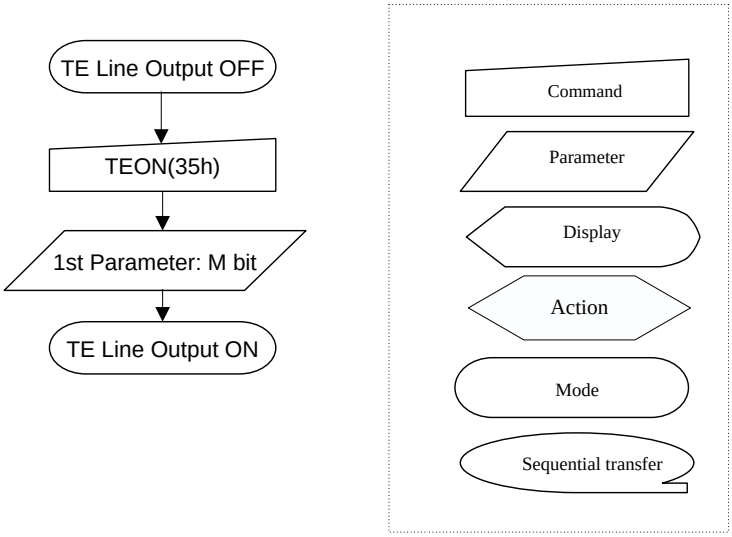
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	-	GS	SS	SM
Power On Sequence	-	1’b0	1’b0	1’b0
HW Reset	-	1’b0	1’b0	1’b0

6.3.4. Tearing Effect Control (BAh)

<table>
<tr><td>35h</td><td colspan="13">Tearing Effect Width Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>BAh</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>te_pol</td><td colspan="7">te_width[6:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">te_pol is used to adjust the Tearing Effect output signal pulse polarity.
<table><tr><td>te_pol</td><td>Tearing Effect polarity</td></tr><tr><td>0</td><td>Positive pulse</td></tr><tr><td>1</td><td>negative pulse</td></tr></table>te_width[6:0] is used to adjust the Tearing Effect output signal pulse width with display lines in unit
<table><tr><td>te_width[6:0]</td><td>Tearing Effect width(display line time)</td></tr><tr><td>0</td><td>1line time</td></tr><tr><td>1</td><td>2line time</td></tr><tr><td>…</td><td>…</td></tr><tr><td>N</td><td>N+1 line time</td></tr><tr><td>…</td><td>…</td></tr><tr><td>7f</td><td>128 line time</td></tr></table>Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already ON</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>0x00</td></tr><tr><td>SW Reset</td><td>0x00</td></tr><tr><td>HW Reset</td><td>0x00</td></tr></table></td></tr>
</table>

Flow Chart	

TE Line Output OFF
TEON(35h)
1st Parameter: M bit
TE Line Output ON
Command
Parameter
Display
Action
Mode
Sequential transfer

6.3.5. Interface Control (F6h)

<table>
<tr><td>F6h</td><td colspan="13">Interface Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>F6h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>1</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td colspan="2">DM [1:0]</td><td>RM</td><td>RIM</td><td>C0</td></tr>
<tr><td>Description</td><td colspan="13">
DM [1:0]: Select the display operation mode.
<table>
<tr><th>DM[1]</th><th>DM[0]</th><th>Display Operation Mode</th></tr>
<tr><td>0</td><td>0</td><td>Internal clock operation</td></tr>
<tr><td>0</td><td>1</td><td>RGB Interface Mode</td></tr>
<tr><td>1</td><td>0</td><td>VSYNC interface Mode</td></tr>
<tr><td>1</td><td>1</td><td>Setting disabled</td></tr>
</table>
RM: Select the interface to access the GRAM.
Set RM to “1” when writing display data by the RGB interface.
<table>
<tr><th>RM</th><th>Interface for RAM Access</th></tr>
<tr><td>0</td><td>System interface/VSYNC interface</td></tr>
<tr><td>1</td><td>RGB interface</td></tr>
</table>
RIM: Specify the RGB interface mode when the RGB interface is used. These bits should be set before display operation through the RGB interface and should not be set during operation.
<table>
<tr><th>RIM</th><th>COLMOD [6:4]</th><th>RGB Interface Mode</th></tr>
<tr><td rowspan="2">0</td><td>110 (262K color)</td><td>18- bit RGB interface (1 transfer/pixel)</td></tr>
<tr><td>101 (65K color)</td><td>16- bit RGB interface (1 transfer/pixel)</td></tr>
<tr><td>1</td><td>(262K color)</td><td>6- bit RGB interface (3 transfer/pixel)</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="13">EXTC should be high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="4">Default Value</th></tr>
<tr><th>MDT[1:0]</th><th>DM [1:0]</th><th>RM</th><th>RIM</th></tr>
<tr><td>Power On Sequence</td><td>2’b00</td><td>2’b00</td><td>1’b0</td><td>1’b0</td></tr>
<tr><td>SW Reset</td><td>2’b00</td><td>2’b00</td><td>1’b0</td><td>1’b0</td></tr>
<tr><td>HW Reset</td><td>2’b00</td><td>2’b00</td><td>1’b0</td><td>1’b0</td></tr>
</table>
</td></tr>
</table>

6.4. Description of Level 3 Command

6.4.1. Frame Rate (E8h)

<table>
<tr><td>E8h</td><td colspan="13">Frame Rate</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>E8h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td colspan="4">dinv[2:0]</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0x14</td></tr>
<tr><td>Description</td><td colspan="13">DINV[2:0] : Set display inversion mode
<table><tr><th>DINV[2:0]</th><th>Inversion</th></tr><tr><td>0</td><td>1 column inversion</td></tr><tr><td>1</td><td>1 dot inversion</td></tr><tr><td>2</td><td>2 dot inversion</td></tr><tr><td>3</td><td>2 column inversion</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

Default		Status	Default Value
			DINV[3:0]
		Power On Sequence	4’h1
		SW Reset	4’h1
		HW Reset	4’h1

6.4.2. SPI 2DATA control(E9h)

<table>
<tr><td>E9h</td><td colspan="12">SPI 2DATA control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>E9h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>2data_en</td><td colspan="3">2data_mdt[2:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="12">2DATA_EN: Set 2_data_line mode in 3-wire/4-wire SPI.
2DATA_MDT[2:0] Set pixel data format in 2_data_line mode.

<table><tr><th>2DATA_MDT[2:0]</th><th>Data Format</th></tr><tr><td>000</td><td>65K color 1pixle/transition</td></tr><tr><td>001</td><td>262K color 1pixle/transition</td></tr><tr><td>010</td><td>262K color 2/3pixle/transition</td></tr><tr><td>100</td><td>4M color 1pixle/transition</td></tr><tr><td>110</td><td>4M color 2/3pixle/transition</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="12">Inter command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>2DATA_EN</th><th>2DATA_MDT[2:0]</th></tr><tr><td>Power On Sequence</td><td>1’b0</td><td>3’b000</td></tr><tr><td>SW Reset</td><td>1’b0</td><td>3’b000</td></tr><tr><td>HW Reset</td><td>1’b0</td><td>3’b000</td></tr></table></td></tr>
</table>

6.4.3. Power Control 1 (C1h)

<table>
<tr><td>C1h</td><td colspan="13">Power Control 1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>C1h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>vcire</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">vcire: Select the external reference voltage VDDB or internal reference voltage VDDBR.
<table><tr><td>vcire =0</td><td>Internal reference voltage 2.5V (default)</td></tr><tr><td>vcire =1</td><td>External reference voltage VDDB</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><td rowspan="2">Status</td><td>Default Value</td></tr><tr><td>vcire</td></tr><tr><td>Power On Sequence</td><td>1’b0</td></tr><tr><td>SW Reset</td><td>1’b0</td></tr><tr><td>HW Reset</td><td>1’b0</td></tr></table></td></tr>
</table>

6.4.4. Power Control 2 (C3h)

<table>
<tr><td>C3h</td><td colspan="13">Power Control 2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>C3h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="7">vreg1_vbp_d[6:0]</td><td>3C</td></tr>
<tr><td>Description</td><td colspan="13">Set the voltage level value to output the VREG1A and VREG1B OUT level, which is a reference level for the grayscale voltage level.(Table is valid when vrh=0x28)
VREG1A=(vrh+vbp_d)*0.02+4
VREG1B=vbp_d*0.02+0.3
<table>
<tr><th>vreg1_vbp_d[6:0]</th><th>VREG1A/V</th><th>VREG1B/V</th></tr>
<tr><td>7'h00</td><td>4.8</td><td>0.3</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>N</td><td>(N+40)*0.02+4</td><td>N*0.02+0.3</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>7’h55</td><td>6.5</td><td>2.0</td></tr>
<tr><td>7’h56</td><td>reserved</td><td>reserved</td></tr>
<tr><td>…</td><td>…</td><td></td></tr>
<tr><td>7’h7F</td><td>reserved</td><td>reserved</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>vreg1_vbp_d[6:0]</th></tr>
<tr><td>Power On Sequence</td><td>7h3c</td></tr>
<tr><td>SW Reset</td><td>7h3c</td></tr>
<tr><td>HW Reset</td><td>7h3c</td></tr>
</table></td></tr>
</table>

6.4.5. Power Control 3 (C4h)

<table>
<tr><td>C4h</td><td colspan="12">Power Control 3</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>C4h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="7">vreg1_vbn_d[6:0]</td><td>3C</td></tr>
<tr><td>Description</td><td colspan="12">Set the voltage level value to output the VREG2A OUT level, which is a reference level for the grayscale voltage level(Table is valid when vrh=0x28)
VREG2A=(vbn_d-vrh)*0.02-3.4
VREG2B=vbn_d*0.02+0.3
<table>
<tr><th>vreg1_vbn_d[6:0]</th><th>VREG2A/V</th><th>VREG2B/V</th></tr>
<tr><td>7'h00</td><td>-4.2</td><td>0.3</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>N</td><td>N*0.02-4.2</td><td>N*0.02+0.3</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>7’h55</td><td>-2.5</td><td>2.0</td></tr>
<tr><td>7’h56</td><td>reserved</td><td>reserved</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>7’h7F</td><td>reserved</td><td>reserved</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>vreg1_vbn_d[6:0]</th></tr>
<tr><td>Power On Sequence</td><td>7’h3C</td></tr>
<tr><td>SW Reset</td><td>7’h3C</td></tr>
<tr><td>HW Reset</td><td>7’h3C</td></tr>
</table></td></tr>
</table>

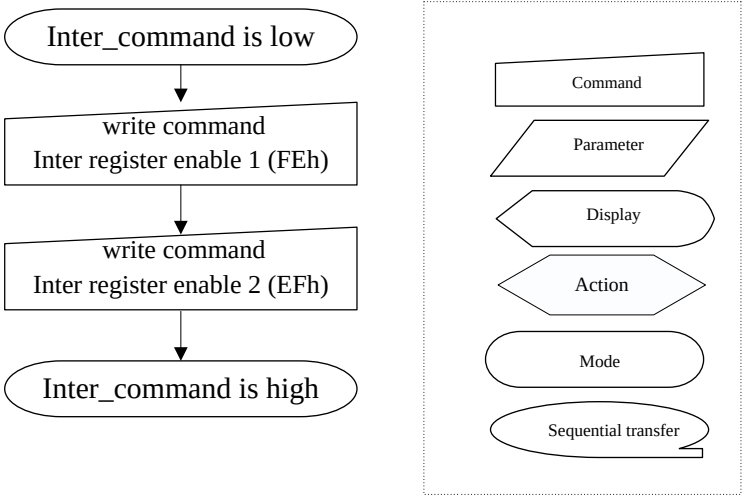
6.4.6. Power Control 4 (C9h)

<table>
<tr><td>C9h</td><td colspan="13">Power Control 4</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>C9h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td colspan="6">vrh[5:0]</td><td>28</td></tr>
<tr><td>Description</td><td colspan="13">Set the voltage level value to output the VREG1A OUT level, which is a reference level for the grayscale voltage level. (Table is valid when vbp_d=0x3C and vbn_d=0x3C)
VREG1A=(vrh+vbp_d)*0.02+4
VREG2A=(vbn_d-vrh)*0.02-3.4
<table>
<tr><th>vrh[5:0]</th><th>VREG1A/V</th><th>VREG2A/V</th></tr>
<tr><td>6'h00</td><td>5.2</td><td>-2.2</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>N</td><td>(N+60)*0.02+4</td><td>(100-N)*0.02-4.2</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>6’h28</td><td>6</td><td>-3</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>6’h3F</td><td>6.46</td><td>-3.46</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>vrh[5:0]</th></tr>
<tr><td>Power On Sequence</td><td>6’h28</td></tr>
<tr><td>SW Reset</td><td>6’h28</td></tr>
<tr><td>HW Reset</td><td>6’h28</td></tr>
</table></td></tr>
</table>

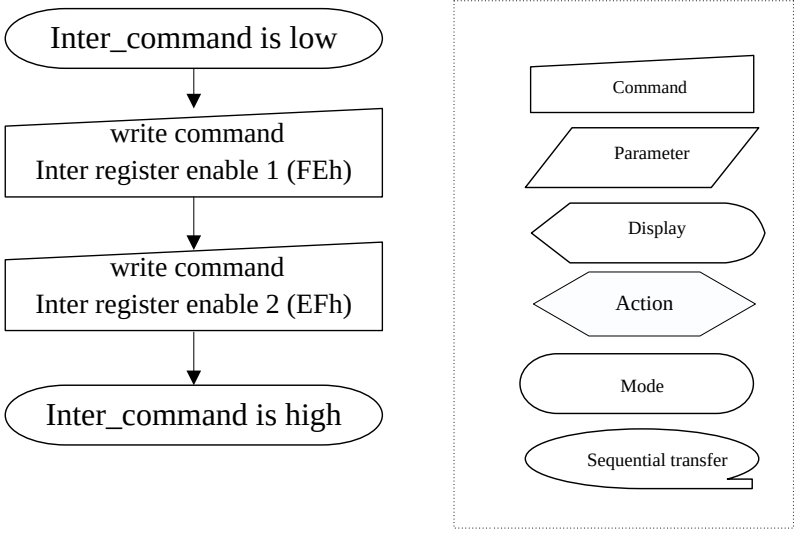
6.4.7. Power Control 7(A7h)

<table>
<tr><td>A7h</td><td colspan="13">Power Control 7</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>A7h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>0</td><td colspan="4">vdd_ad[3:0]</td><td>48</td></tr>
<tr><td>Description</td><td colspan="13">vdd_ad: Set the voltage level value to output the DVDD level,
<table>
<tr><th>vdd_ad[3:0]</th><th>DVDD(V)</th><th>vdd_ad[3:0]</th><th>DVDD(V)</th></tr>
<tr><td>4'h00</td><td>1.483</td><td>4'h08</td><td>1.994</td></tr>
<tr><td>4'h01</td><td>1.545</td><td>4'h09</td><td>2.109</td></tr>
<tr><td>4'h02</td><td>1.590</td><td>4'h0</td><td>2.193</td></tr>
<tr><td>4'h03</td><td>1.638</td><td>4'h0b</td><td>2.286</td></tr>
<tr><td>4'h04</td><td>1.714</td><td>4'h0c</td><td>2.385</td></tr>
<tr><td>4'h05</td><td>1.279</td><td>4'h0d</td><td>1.713</td></tr>
<tr><td>4'h06</td><td>1.859</td><td>4'h0e</td><td>1.713</td></tr>
<tr><td>4'h07</td><td>1.925</td><td>4'h0f</td><td>1.713</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>vdd_ad[3:0]</th></tr>
<tr><td>Power On Sequence</td><td>4’b48</td></tr>
<tr><td>SW Reset</td><td>4’b48</td></tr>
<tr><td>HW Reset</td><td>4’b48</td></tr>
</table></td></tr>
</table>

6.4.8. Inter Register Enable1(FEh)

<table>
<tr><td>FEh</td><td colspan="13">Inter register enable 1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>FEh</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used for Inter_command controlling.
To set Inter_command high ,you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously.
Once Inter_command is set high, only hardware or software reset can turn it to low.
 
</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13"></td></tr>
</table>

6.4.9. Inter Register Enable2(EFh)

<table>
<tr><td>EFh</td><td colspan="13">Inter register enable 2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>EFh</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used for Inter_command controlling.
To set Inter_command high ,you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously.
Once Inter_command is set high, only hardware or software reset can turn it to low.
 
</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13"></td></tr>
</table>

6.4.10. SET_GAMMA1 (F0h)

<table>
<tr><td>F0h</td><td colspan="13">SET_GAMMA1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>F0h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>dig2gam_dig2j0_n[1:0]</td><td colspan="7">dig2gam_vr1_n[5:0]</td><td>80</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>dig2gam_dig2j1_n[1:0]</td><td colspan="7">dig2gam_vr2_n[5:0]</td><td>03</td></tr>
<tr><td>3st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td></td><td colspan="4">dig2gam_vr4_n[4:0]</td><td>08</td></tr>
<tr><td>4nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td></td><td colspan="4">dig2gam_vr6_n[4:0]</td><td>06</td></tr>
<tr><td>5st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="4">dig2gam_vr0_n[3:0]</td><td colspan="4">dig2gam_vr13_n[3:0]</td><td>05</td></tr>
<tr><td>6nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td colspan="8">dig2gam_vr20_n[6:0]</td><td>2B</td></tr>
<tr><td>Description</td><td colspan="13">dig2gam_dig2j0_n[1:0]: γ gradient adjustment register for negative polarity
dig2gam_dig2j1_n[1:0]: γ gradient adjustment register for negative polarity
dig2gam_vr0_n[3:0]: γ gradient adjustment register for negative polarity
dig2gam_vr1_n[5:0]: γ gradient adjustment register for negative polarity
dig2gam_vr2_n[5:0]: γ gradient adjustment register for negative polarity
dig2gam_vr4_n[4:0]: γ gradient adjustment register for negative polarity
dig2gam_vr6_n[4:0]: γ gradient adjustment register for negative polarity
dig2gam_vr13_n[3:0]: γ gradient adjustment register for negative polarity
dig2gam_vr20_n[6:0]: γ gradient adjustment register for negative polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Id e Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

Default		Status	Default Value				
			dig2gam_dig2j0_n[1:0]	dig2gam_dig2j1_n[1:0]	dig2gam_vr0_n[3:0]	dig2gam_vr1_n[5:0]	dig2gam_vr2_n[5:0]	dig2gam_vr4_n[4:0]
		Power On Sequence	2'h02	2'h00	4'h00	6'h00	6'h03	5'h08
		SW Reset	2'h02	2'h00	4'h00	6'h00	6'h03	5'h08
		HW Reset	2'h02	2'h00	4'h00	6'h00	6'h03	5'h08

Default		Status	Default Value				
			dig2gam_vr6_n[4:0]	dig2gam_vr13_n[3:0]	dig2gam_vr20_n[6:0]			
		Power On Sequence	5'h06	4'h05	7'h2b			
		SW Reset	5'h06	4'h05	7'h2b			
		HW Reset	5'h06	4'h05	7'h2b			

6.4.11. SET_GAMMA2 (F1h)

<table>
<tr><td>F1h</td><td colspan="13">SET_GAMMA2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>F1h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td colspan="7">dig2gam_vr43_n[6:0]</td><td>41</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="2">dig2gam_vr27_n[2:0]</td><td colspan="6">dig2gam_vr57_n[4:0]</td><td>97</td></tr>
<tr><td>3st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="2">dig2gam_vr36_n[2:0]</td><td colspan="6">dig2gam_vr59_n[4:0]</td><td>98</td></tr>
<tr><td>4nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td colspan="7">dig2gam_vr61_n[5:0]</td><td>13</td></tr>
<tr><td>5st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td colspan="7">dig2gam_vr62_n[5:0]</td><td>17</td></tr>
<tr><td>6nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="4">dig2gam_vr50_n[3:0]</td><td colspan="4">dig2gam_vr63_n[3:0]</td><td>CD</td></tr>
<tr><td>Description</td><td colspan="13">dig2gam_vr43_p[6:0]: γ gradient adjustment register for negative polarity
dig2gam_vr27_p[2:0]: γ gradient adjustment register for negative polarity
dig2gam_vr57_p[4:0]: γ gradient adjustment register for negative polarity
dig2gam_vr59_p[4:0]: γ gradient adjustment register for negative polarity
dig2gam_vr36_p[2:0]: γ gradient adjustment register for negative polarity
dig2gam_vr61_p[5:0]: γ gradient adjustment register for negative polarity
dig2gam_vr62_p[5:0]: γ gradient adjustment register for negative polarity
dig2gam_vr50_p[3:0]: γ gradient adjustment register for negative polarity
dig2gam_vr63_p[3:0]: γ gradient adjustment register for negative polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mo e On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

Default

Status	Default Value					
	dig2gam_vr43_p[6:0]	dig2gam_vr27_p[2:0]	dig2gam_vr57_p[4:0]	dig2gam_vr59_p[4:0]	dig2gam_vr36_p[2:0]	dig2gam_vr61_p[5:0]
Power On Sequence	7'h41	3'h04	5'h17	5'h18	3'h04	6'h13
SW Reset	7'h41	3'h04	5'h17	5'h18	3'h04	6'h13
HW Reset	7'h41	3'h04	5'h17	5'h18	3'h04	6'h13

Default

Status	Default Value					
	dig2gam_vr62_p[5:0]	dig2gam_vr50_p[3:0]	dig2gam_vr63_p[3:0]			
Power On Sequence	6'h17	4'h0C	4'h0D			
SW Reset	6'h17	4'h0C	4'h0D			
HW Reset	6'h17	4'h0C	4'h0D			

6.4.12. SET_GAMMA3 (F2h)

<table>
<tr><td>F2h</td><td colspan="13">SET_GAMMA3</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>F2h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>dig2gam_dig2j0_p[1:0]</td><td colspan="7">dig2gam_vr1_p[5:0]</td><td>40</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>dig2gam_dig2j1_p[1:0]</td><td colspan="7">dig2gam_vr2_p[5:0]</td><td>03</td></tr>
<tr><td>3st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td></td><td colspan="5">dig2gam_vr4_p[4:0]</td><td>08</td></tr>
<tr><td>4nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td></td><td colspan="5">dig2gam_vr6_p[4:0]</td><td>0B</td></tr>
<tr><td>5st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="4">dig2gam_vr0_p[3:0]</td><td colspan="4">dig2gam_vr13_p[3:0]</td><td>08</td></tr>
<tr><td>6nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td colspan="8">dig2gam_vr20_p[6:0]</td><td>2E</td></tr>
<tr><td>Description</td><td colspan="13">dig2gam_dig2j0_p[1:0]: γ gradient adjustment register for positive polarity
dig2gam_dig2j1_p[1:0]: γ gradient adjustment register for positive polarity
dig2gam_vr1_p[5:0]: γ gradient adjustment register for positive polarity
dig2gam_vr2_p[5:0]: γ gradient adjustment register for positive polarity
dig2gam_vr4_p[4:0]: γ gradient adjustment register for positive polarity
dig2gam_vr6_p[4:0]: γ gradient adjustment register for positive polarity
dig2gam_vr0_p[3:0]: γ gradient adjustment register for positive polarity
dig2gam_vr13_p[3:0]: γ gradient adjustment register for positive polarity
dig2gam_vr20_p[6:0]: γ gradient adjustment register for positive polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle M de Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

Default

Status	Default Value					
	dig2gam_dig2j0_p[1:0]	dig2gam_dig2j1_p[1:0]	dig2gam_vr1_p[5:0]	dig2gam_vr2_p[5:0]	dig2gam_vr4_p[4:0]	dig2gam_vr6_p[4:0]
Power On Sequence	2'h01	2'h00	6'h00	6'h03	5'h08	5'h0B
SW Reset	2'h01	2'h00	6'h00	6'h03	5'h08	5'h0B
HW Reset	2'h01	2'h00	6'h00	6'h03	5'h08	5'h0B

Default

Status	Default Value					
	dig2gam_vr0_p[3:0]	dig2gam_vr13_p[3:0]	dig2gam_vr20_p[6:0]			
Power On Sequence	4'h00	4'h08	7'h2E			
SW Reset	4'h00	4'h08	7'h2E			
HW Reset	4'h00	4'h08	7'h2E			

6.4.13. SET_GAMMA4 (F3h)

<table>
<tr><td>F3h</td><td colspan="13">SET_GAMMA4</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>F3h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td colspan="7">dig2gam_vr43_p[6:0]</td><td>3F</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="2">dig2gam_vr27_p[2:0]</td><td colspan="6">dig2gam_vr57_p[4:0]</td><td>98</td></tr>
<tr><td>3st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="2">dig2gam_vr36_p[2:0]</td><td colspan="6">dig2gam_vr59_p[4:0]</td><td>B4</td></tr>
<tr><td>4nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td colspan="7">dig2gam_vr61_p[5:0]</td><td>14</td></tr>
<tr><td>5st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td colspan="7">dig2gam_vr62_p[5:0]</td><td>18</td></tr>
<tr><td>6nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="4">dig2gam_vr50_p[3:0]</td><td colspan="4">dig2gam_vr63_p[3:0]</td><td>CD</td></tr>
<tr><td>Description</td><td colspan="13">dig2gam_vr43_p[6:0]: γ gradient adjustment register for positive polarity
dig2gam_vr27_p[2:0]: γ gradient adjustment register for positive polarity
dig2gam_vr57_p[4:0]: γ gradient adjustment register for positive polarity
dig2gam_vr36_p[2:0]: γ gradient adjustment register for positive polarity
dig2gam_vr59_p[4:0]: γ gradient adjustment register for positive polarity
dig2gam_vr61_p[5:0]: γ gradient adjustment register for positive polarity
dig2gam_vr62_p[5:0]: γ gradient adjustment register for positive polarity
dig2gam_vr50_p[3:0]: γ gradient adjustment register for positive polarity
dig2gam_vr63_p[3:0]: γ gradient adjustment register for positive polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

Default

Status	Default Value					
	dig2gam_vr43_p[6:0]	dig2gam_vr27_p[2:0]	dig2gam_vr57_p[4:0]	dig2gam_vr36_p[2:0]	dig2gam_vr59_p[4:0]	dig2gam_vr61_p[5:0]
Power On Sequence	7'h3F	3'h04	5'h18	3'h05	5'h14	6'h14
SW Reset	7'h3F	3'h04	5'h18	3'h05	5'h14	6'h14
HW Reset	7'h3F	3'h04	5'h18	3'h05	5'h14	6'h14

Default

Status	Default Value					
	dig2gam_vr62_p[5:0]	dig2gam_vr50_p[3:0]	dig2gam_vr63_p[3:0]			
Power On Sequence	6'h18	4'h0C	4'h0D			
SW Reset	6'h18	4'h0C	4'h0D			
HW Reset	6'h18	4'h0C	4'h0D			

7. Electrical Characteristics

7.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When GC9A01 is used out of the absolute maximum ratings, GC9A01 may be permanently damaged. To use GC9A01 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, GC9A01 will malfunction and cause poor reliability.

Table43.

Item	Symbol	Unit	Value
Supply voltage	VDDB	V	-0.3~+4.6
Supply voltage(Logic)	VDDI	V	-0.3~+4.6
Supply voltage(Digital)	DVDD	V	-0.3~+2.0
Driver supply voltage	VGH-VGL	V	-0.3~+27.0
Logic input voltage range	VIN	V	-0.3~VDDI+0.3
Logic output voltage range	VO	V	-0.3~VDDI+0.3
Operation temperature	Topr	℃	-40~+80
Storage temperature	Tstg	℃	-40~+80
Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.			

7.2. DC Characteristics

General DC Characteristics

Table44.

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VDDB	V	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	VDDI	V	I/O supply voltage	1.65	2.8	3.3	Note2
Digital Operating voltage	DVDD	V	Digital supply voltage	-	1.5	-	Note2
Gate Driver High Voltage	VGH	V	-	8.0	-	12.0	Note3
Gate Driver Low Voltage	VGL	V	-	-11.0	-	-7.0	Note3
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.7*VDDI	-	VDDI	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	VSSB	-	0.3*VDDI	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*VDDI	-	VDDI	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	VSSB	-	0.2*VDDI	Note1,2,3
Logic High Level Input Current	IIH	uA	-	-	-	1	Note1,2,3
Logic Low Level Input Current	IIL	uA	-	-1	-	-	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=VDDI or VSSB	-0.1	-	+0.1	Note1,2,3
Source Driver							
Positive Source Output Range	Vsout	V	-	VREG1B	-	VREG1A	
Negative Source Output Range	Vsout	V	-	VREG2A	-	VREG2B	

Note 1: VDDI=1.65 to 3.3V, VDDB=2.5 to 3.3V, AGND=VSS=0V, Ta=-30 to 70 (to +85 no damage)℃

Note2: Please supply digital VDDI voltage equal or less than analog VDDB voltage.

Note3: CSX, RDX, WRX, D[17:0], D/CX, RESX, TE, DOTCLK, VSYNC, HSYNC, DE, SDA, SCL, IM3, IM2, IM1,IM0, and Test pins.

7.3. AC Characteristics

7.3.1. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-Ⅰ)

Figure90.

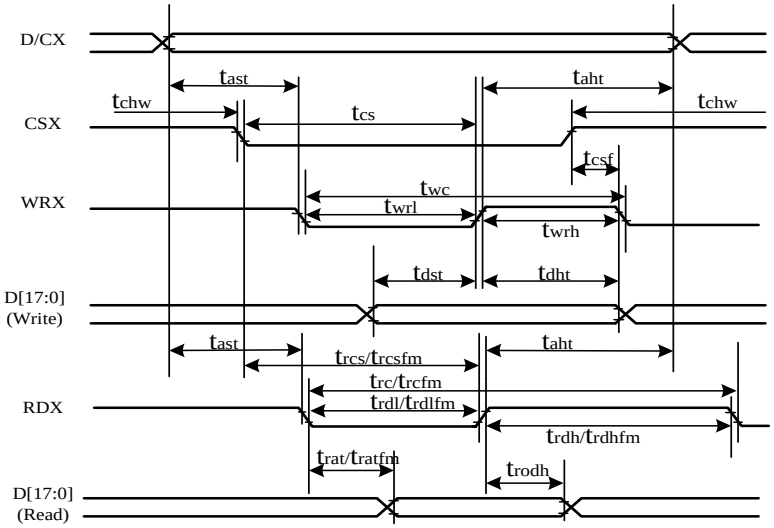


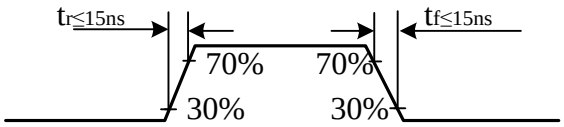
Table45.

Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	380	-	ns	
	trdhfm	Read Control H duration(FM)	180	-	ns	
	trdlfm	Read Control L duration(FM)	200	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control H pulse duration	90	-	ns	
	trdl	Read Control L pulse duration	70	-	ns	
D[17:0], D[15:0],	tdst	Write data setup time	10	-	ns	For maximum CL=30pF
	tdht	Write data hold time	10	-	ns	

D[8:0], D[7:0]	trat	Read access time	-	40	ns	For minimum CL=8pF
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

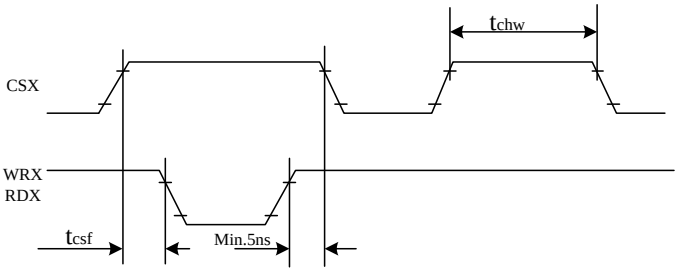
Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VDDB=2.5V to 3.3V, VSS=0V

Figure91.



CSX timings :

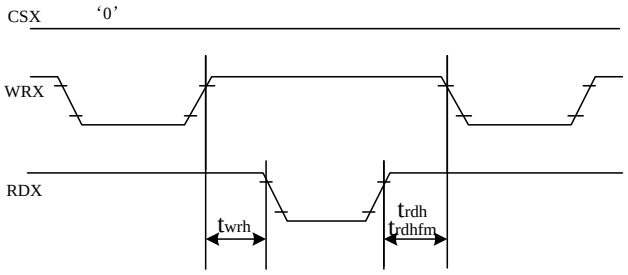
Figure92.



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:

Figure92.



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.3.2. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-Ⅱ)

Figure93.

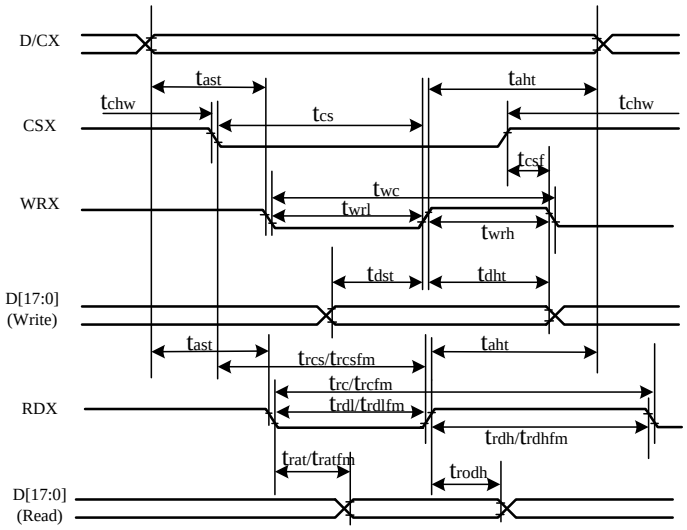
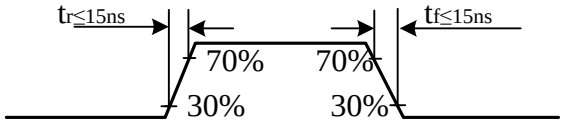


Table46.

Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	380	-	ns	
	trdhfm	Read Control H duration(FM)	180	-	ns	
	trdlfm	Read Control L duration(FM)	200	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	70	-	ns	
D[17:0], D[17:10] &D[8:1], D[17:10] ,D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

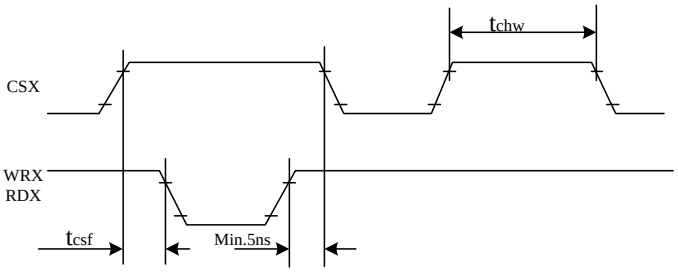
Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VDDB=2.5V to 3.3V, VSS=0V.

Figure94.



CSX timings :

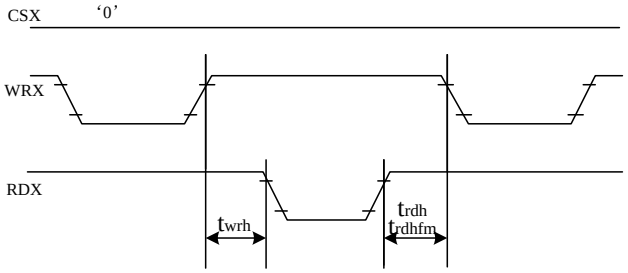
Figure95.



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:

Figure96.



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.3.3. Display Serial Interface Timing Characteristics (3-line SPI system)

Figure97.

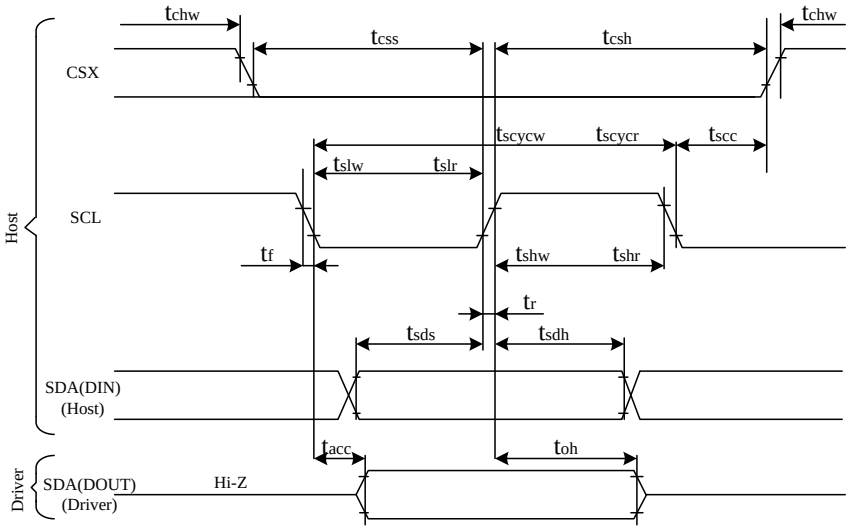
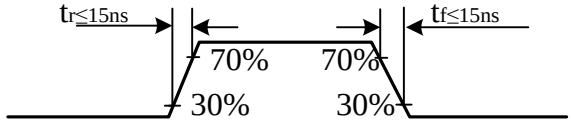


Table47.

Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	10	-	ns	
	tshw	SCL "H" Pulse Width (Write)	5	-	ns	
	tslw	SCL "L" Pulse Width (Write)	5	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA/SDI (Input)	tsds	Data setup time (Write)	5	-	ns	
	tsdh	Data hold time (Write)	5	-	ns	
SDA/SD0(Outp)	tacc	Access time (Read)	10	-	ns	
CSX	tscc	SCL-CSX	10	-	ns	
	tchw	CSX "H" Pulse Width	10	-	ns	
	tcss	CSX-SCL Time	20	-	ns	
	tcsh		40	-	ns	

Note: Ta = 25 ℃, VDDI=1.65V to 3.3V, VDDB=2.5V to 3.3V, VSSB=VSSB=0V

Figure98.



7.3.4. Display Serial Interface Timing Characteristics (4-line SPI system)

Figure98.

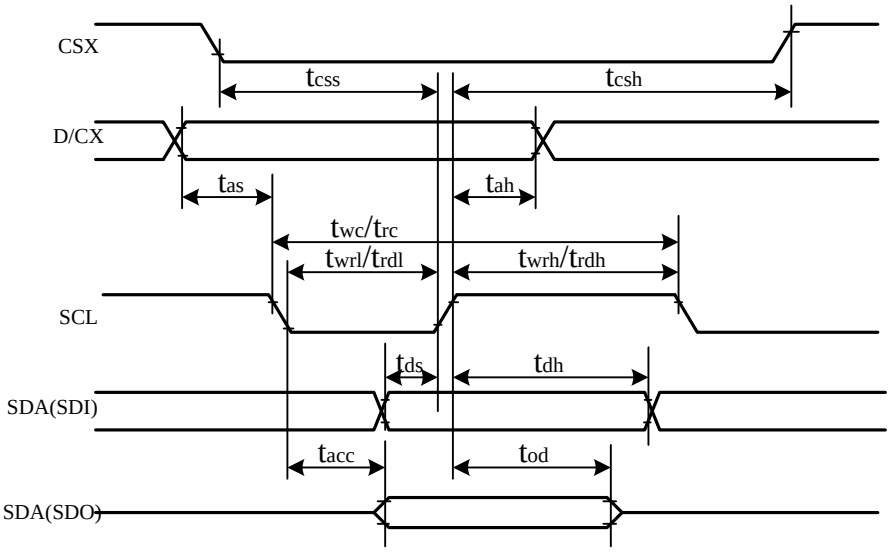
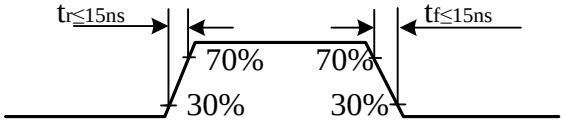


Table48.

Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	20	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial Clock Cycle (Write)	10	-	ns	
	twrh	SCL "H" Pulse Width (Write)	5	-	ns	
	twrl	SCL "L" Pulse Width (Write)	5	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL "H" Pulse Width (Read)	60	-	ns	
	trdl	SCL "L" Pulse Width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA/SDI (Input)	tds	Data setup time (Write)	5	-	ns	
	tdh	Data hold time (Write)	5	-	ns	
SDA/SD0 (Output)	tacc	Access time (Read)	10	-	ns	

Note: Ta = 25 ℃, VDDI=1.65V to 3.3V, VDDB=2.5V to 3.3V, AGND=VSS=0V

Figure99.



7.3.5. Parallel 18/16/6-bit RGB Interface Timing Characteristics

Figure100.

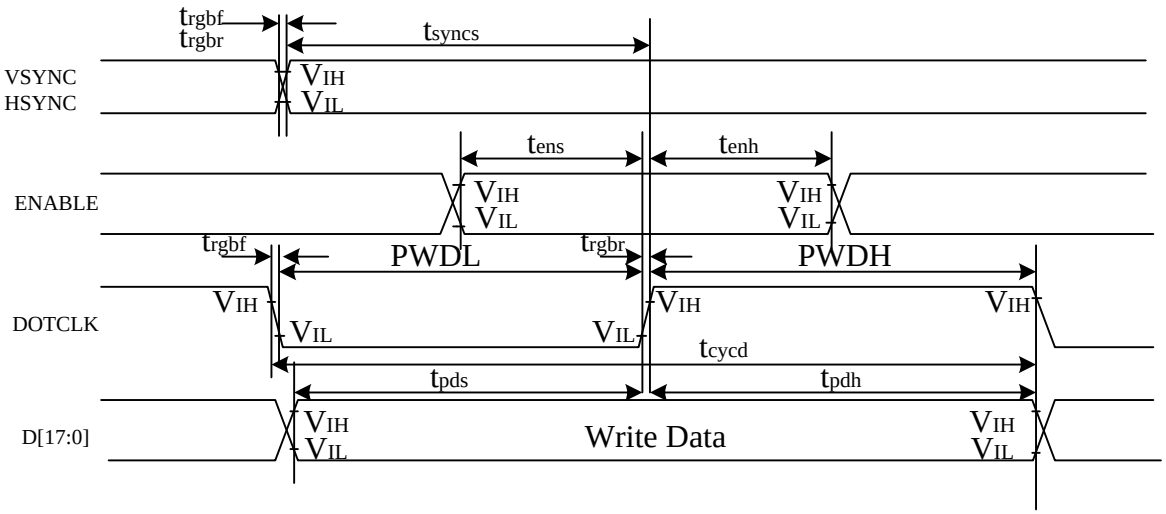


Table49.

Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/HSYNC	tsyncs	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	tens	DE setup time	15	-	ns	
	tenh	DE hold time	15	-	ns	
D[17:0]	tpos	Data setup time	15	-	ns	
	tpdh	Date hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	tcycd	DOTCLK cycle time	100	-	ns	
	trgbr,trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC/HSYNC	tsyncs	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	tens	DE setup time	15	-	ns	
	tenh	DE hold time	15	-	ns	
D[17:0]	tpos	Data setup time	15	-	ns	
	tpdh	Date hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	tcycd	DOTCLK cycle time	100	-	ns	
	trgbr,trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VDDB=2.5V to 3.3V, AGND=VSS=0V

Figure101.