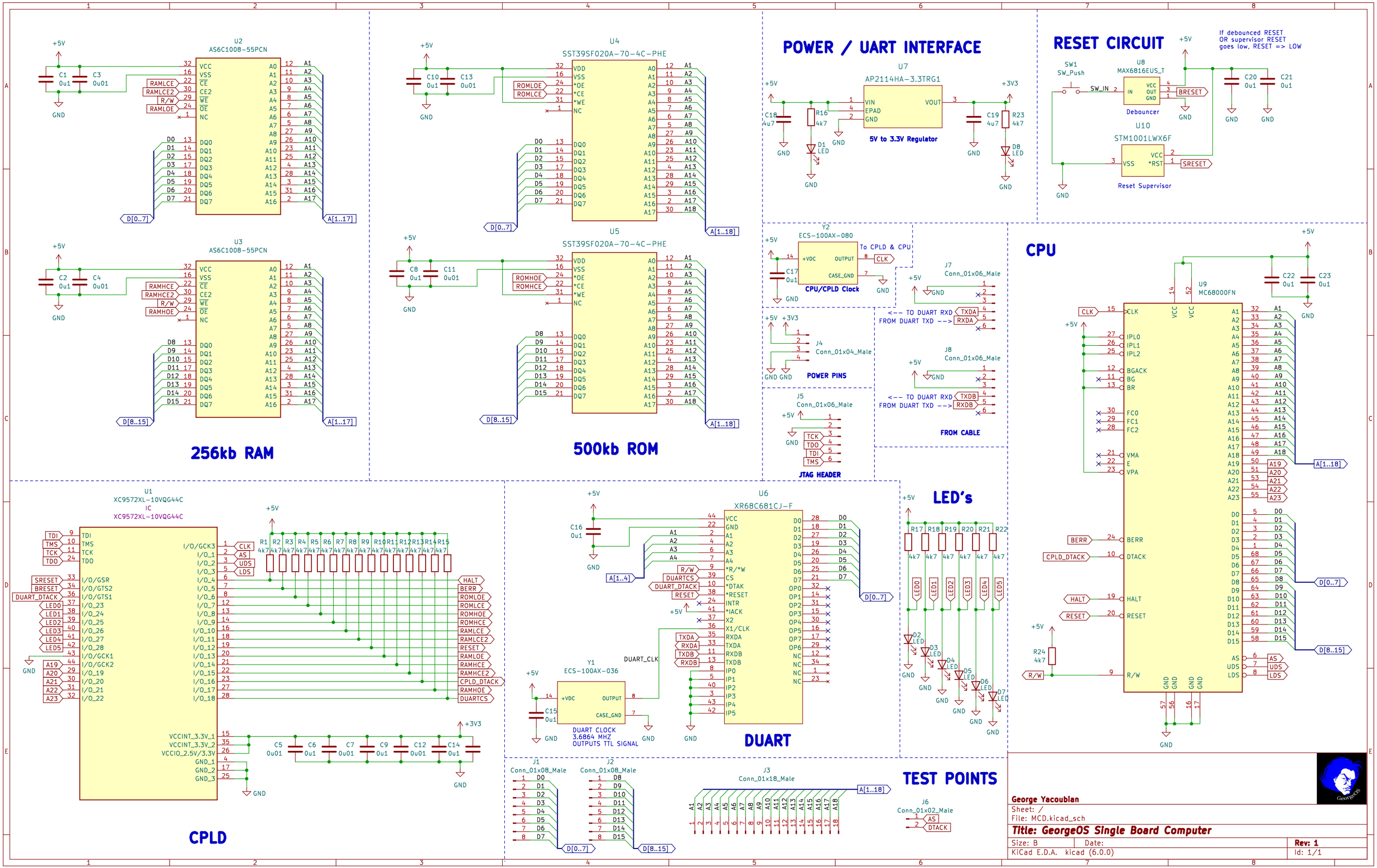
256kb RAM
U2
AS6C1008-55PCN
U3
AS6C1008-55PCN
500kb ROM
U4
SST39SF020A-70-4C-PHE
U5
SST39SF020A-70-4C-PHE
POWER / UART INTERFACE
U7
AP2114HA-3.3TRG1
5V to 3.3V Regulator
Y2
ECS-100AX-080
CPU/CPLD Clock
To CPLD & CPU
J4
Conn_01x04_Male
POWER PINS
J5
Conn_01x06_Male
JTAG HEADER
J7
Conn_01x06_Male
J8
Conn_01x06_Male
FROM CABLE
RESET CIRCUIT
If debounced RESET OR supervisor RESET goes low, RESET => LOW
SW1
SW_Push
U8
MAX6816EUS_T
Debouncer
U10
STM1001LWX6F
Reset Supervisor
CPU
U9
MC68000FN
CPLD
U1
XC9572XL-10VQG44C
U6
XR68C681CJ-F
DUART
Y1
ECS-100AX-036
DUART CLOCK
3.6864 MHZ
OUTPUTS TTL SIGNAL
LED's
TEST POINTS
J1
Conn_01x08_Male
J2
Conn_01x08_Male
J3
Conn_01x18_Male
J6
Conn_01x02_Male
George Yacoubian
Sheet: /
File: MCD.kicad_sch
Title: GeorgeOS Single Board Computer
Size: B
Date:
Rev: 1
KiCad E.D.A. kicad (6.0.0)
Id: 1/1