CS622 : Assignment 3

Group 7

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1) On PIN tool generated machine access traces of program 2 (prog2) :

- Number of simulated cycles : 1703426
- Number of L1 cache accesses : 2509903
- Number of L1 cache misses : 246759
- Number of L2 cache misses : 246408

Names and Counts of all messages received by the L1 cache of each core for machine traces of prog2.

Messages	Core 1	Core 2	Core 3	Core 4	Core 5	Core 6	Core 7	Core 8
GET	91	2	2	3	2	2	2	0
PUT	16719	24606	24615	24604	24604	24606	24614	16474
GETX	9	0	0	0	0	0	0	0
PUTX	65844	9	11	10	11	11	11	10
INVALID	13	16	18	16	18	18	17	13
INVALID_ACK	44	7	9	14	9	9	9	28
UPGRADE_ACK	6	1	1	2	1	1	1	4
NACK	0	0	0	0	0	0	0	0

Table 1: The names and counts of all messages received by the L1 caches (prog2).

The names and counts of all messages received by the L2 cache for machine traces of prog2.

Messages	Counts
GET	180842
GETX	65917
SWB	104
UPGRADE	17
ACK	9

Table 2: The names and counts of all messages received by the L2 caches(prog2).

2) On PIN tool generated machine access traces of program 3 (prog3) :

- Number of simulated cycles : 5792852
- Number of L1 cache accesses : 9463513
- Number of L1 cache misses : 656746
- Number of L2 cache misses : 654914

Names and Counts of all messages received by the L1 cache of each core for machine traces of prog3.

Messages	Core 1	Core 2	Core 3	Core 4	Core 5	Core 6	Core 7	Core 8
GET	789	72	53	11	218	43	9	1
PUT	131581	65590	65596	65602	65597	65598	65597	65591
GETX	7	0	0	0	0	0	0	0
PUTX	65854	20	21	22	22	20	19	16
INVALID	881	885	913	586	875	901	601	861
INVALID_ACK	287	436	78	2430	380	159	2290	413
UPGRADE_ACK	38	60	7	343	50	19	324	56
NACK	0	0	0	0	0	0	0	0

Table 3: The names and counts of all messages received by the L1 caches(prog3).

The names and counts of all messages received by the L2 cache for machine traces of prog3.

Messages	Counts
GET	590752
GETX	65994
SWB	1196
UPGRADE	897
ACK	7

Table 4: The names and counts of all messages received by the L2 caches(prog3).

3) On PIN tool generated machine access traces of program 4 (prog4) :

- Number of simulated cycles : 835022
- Number of L1 cache accesses : 1065090
- Number of L1 cache misses : 13220
- Number of L2 cache misses : 131760

Names and Counts of all messages received by the L1 cache of each core for machine traces of prog4.

Messages	Core 1	Core 2	Core 3	Core 4	Core 5	Core 6	Core 7	Core 8
GET	49	1	2	3	2	2	2	2
PUT	8544	8221	8220	8220	8221	8219	8219	8220
GETX	7	0	1	1	1	1	0	0
PUTX	65846	12	11	12	13	13	13	12
INVALID	28	28	29	29	29	29	28	29
INVALID_ACK	78	7	0	22	32	32	26	32
UPGRADE_ACK	10	1	0	3	4	4	3	4
NACK	0	0	0	0	0	0	0	0

Table 5: The names and counts of all messages received by the L1 caches (prog4).

The names and counts of all messages received by the L2 cache for machine traces of prog4.

Messages	Counts
GET	66088
GETX	65932
SWB	63
UPGRADE	29
ACK	11

Table 6: The names and counts of all messages received by the L2 caches(prog4).

Observation

- We are getting simulated cycles less than total machine accesses.
- We are using 20 cycles waiting for NACK, after 20 cycles it is Resend.

Messages

- GET : Read request
- GETX : Write request
- PUT : Response of read request
- PUTX : Response of write request
- UPGRADE : Upgrade request
- UPGRADE_ACK : Acknowledgement of Upgrade Request
- INVALID : Message to invalid given block
- INVALID_ACK : Acknowledgement of INVALID message
- SWB : Sharing Write Back by the owner to the home node
- NACK : Negative Acknowledgement if the block is in process
- ACK : Acknowledgement sent to home node by owner who was in modified state and home node request to send the block to given requester which is also requesting block for write (write after write case).