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prtx

Pratik Shrestha

Education

2019 - Present **Ph.D. in Electrical Engineering**.
Drexel University, Philadelphia, Pennsylvania
Relevant Courseworks: VLSI Design, ASIC Design, Machine Learning, Deep Learning, Hardware Security

2012 - 2016 **Bachelors in Computer Engineering**.
Kathmandu University, Dhulikhel, Kavre, Nepal

Research Experience

Aug 2019 - Present **Graduate Researcher**, Integrated Circuits and Electronics Lab, Drexel University.

- Representation learning guided electronic design automation.
  - Developed an integrated framework for large scale circuit design dataset generation and rapid prototyping of deep learning models.
  - Modelled graph based neural networks to predict timing and interconnect impedance.
- Hardware security and sequential circuit obfuscation.
  - Developed synthesis algorithm and security metric for FSM locking achieving 8.53x increase in security.

Professional Experience

Jan 2018 - Jun 2019 **Engineering Consultant**, Leapfrog Technologies.

- **Ed-Fi Alliance Analytics Middleware:** Rapid synthesis and reporting of Texas school district data across rosters, transcripts, assessments, college applications, etc.
- Developed yaml based domain specific language for rapid query generation.
- Developed python modules for data extraction, parsing, pipeline, storage, report generation.
- Created RESTful API for client-end applications and statistical analysis tool to monitor server traffic.

Jun 2017 - Jun 2019 **Software Engineer**, Beta Analytics.

- **NEPSEguide:** Pricing and risk analytic tools to support financial risk management.
- Designed data entry, normalization, and verification systems supporting 30+ remote data entry workers.
- Designed data warehouse schema to support historical pricing data for Nepal stock exchange.
- Implemented statistical metrics for predictive analyses. Developed stock screener and charting tools to analyze asset performance.

Nov 2016 - Jun 2017 **Associate Developer**, Logic Information Systems.

- Implemented Oracle Retail Analytics Data-warehousing architecture and develop BI solutions.
- Provided 24-hr technical support and consulted offshore clients on ETL batches.

Jun 2016 - Oct 2016 **Software Development Intern**, Logic Information Systems.

- Migrated ETL tool Oracle Data Integrator's (ODI) knowledge modules from Oracle to Teradata.

Technical Proficiency

Languages	Python, Verilog, VHDL, Bash, TCL, SQL (Expertise)
	R, Matlab, Java, Javascript, VBScript, C++, C (Working Knowledge)
EDA	Synopsys: DC Compiler, IC Compiler, PrimeTime; Cadence: Virtuoso, Innovus
Data/ML	Pandas, Tensorboard, Statsmodel, Scikit-learn, Torch, Torch-geometric, NLTK
Databases	PostgreSQL, MongoDB, MS-SQL, Oracle, Teradata
Frameworks	Docker, SQLAlchemy, Scrapy, Airflow, Selenium, Flask, Django

Publications

- **Shrestha, P.**, Phatharodom, S., & Savidis, I. (2022, September). Graph Representation Learning for Gate Arrival Time Prediction. In Proceedings of the 2022 ACM/IEEE Workshop on Machine Learning for CAD (pp. 127-133).
- **Shrestha, P.**, & Savidis, I. (2022, May). Synthesis of Coupling Capacitance Based Hidden State Transitions for Sequential Logic Locking. In 2022 IEEE International Symposium on Circuits and Systems (ISCAS) (pp. 1734-1738). IEEE.