Indian Institute of Technology Kharagpur

AUTUMN Semester, 2020
COMPUTER SCIENCE AND ENGINEERING

Computer Organization Laboratory

Assignment-2: Verilog Design of Binary Adders

Full Marks: 20

Time allowed: 6 hours

INSTRUCTIONS: Make one submission per group in the form of a single zipped folder containing your Verilog source code files(s) and Verilog testbench(es) only, and not the auxiliary files that Vivado generates. Name your submitted zipped folder as `Assgn_2_Grp_<Group_no>.zip` and (e.g. `Assgn_2__Grp_25.zip`). Inside each submitted source and testbench files, there should be a clear header describing the assignment no., problem no., semester, group no., and names of group members. Liberally comment your code to improve its comprehensibility.

1. [**Ripple Carry Binary Adder**] Design (using Verilog), simulate, and synthesize for any target FPGA supported by your version of *Vivado* an 8-bit *ripple carry adder*. Your design should consist of a cascade of eight full adders. Write a testbench to simulate it. After logic synthesis, note its hardware requirement and critical path delay from the synthesis report. The interface of your design should be:
`module ripple_carry_adder (input [7:0] a, input [7:0] b, input cin, output [7:0] sum, output cout);`. (5 marks)

2. [**Hybrid Binary Adder**] Design (using Verilog), simulate, and synthesize for any target FPGA supported by your version of *Vivado*, an 8-bit *hybrid adder*. Your design should consist of a cascade of two 4-bit *carry lookahead adders*. Write a testbench to simulate it. After logic synthesis, note its hardware requirement and critical path delay from the synthesis report. The interface of your design should be:
`module hybrid_adder (input [7:0] a, input [7:0] b, input cin, output [7:0] sum, output cout);`. (6 marks)

3. [**Bit-serial Binary Adder**] Design (using Verilog), simulate and synthesize for any target FPGA supported by your version of *Vivado*, a bit-serial adder. Write a testbench to simulate it. After logic synthesis, note its hardware requirement and critical path delay from the synthesis report. The input-side shift registers used in the datpath of your bit-serial adder should have "parallel load" capabilities such that the 8-bit operands can be loaded in each of them in one clock cycle. Come up with a proper interface of your design, which includes all input control signals and a clock signal. (7 marks)

4. Finally, submit a small 1-page report (in .pdf format) comparing the speed of operation and hardware requirements of the above three designs. This report should be inside the zipped folder you submit. (2 marks)