Indian Institute of Technology Kharagpur

AUTUMN Semester, 2020
COMPUTER SCIENCE AND ENGINEERING

Computer Organization Laboratory

Assignment-3: Verilog Design of Combinational and Sequential Unsigned Multipliers

Full Marks: 20

Time allowed: 6 hours

INSTRUCTIONS: Make one submission per group in the form of a single zipped folder containing your Verilog source code files(s) and Verilog testbench(es). Name your submitted zipped folder as `Assgn_3_Grp_<Group_no>.zip` and (e.g. `Assgn_3__Grp_25.zip`). Inside each submitted source and testbench files, there should be a clear header describing the assignment no., problem no., semester, group no., and names of group members. Liberally comment your code to improve its comprehensibility.

1. [**Combinational Unsigned Binary Multiplier (*Array Multiplier*)**] Design (using Verilog), simulate (using a proper Verilog testbench) and synthesize for any target FPGA platform supported by your version of *Vivado*,a combinational circuit ("Array Multiplier") to multiply two 6-bit unsigned integers. For the general architecture of an array multiplier, please refer to the diagram uploaded on *Moodle*. Note down the hardware footprint and critical path delay of your synthesized design. The interface of your design should be:
`module unsigned_array_mult (input [5:0] a, input [5:0] b, output reg [11:0] product);`. (4 marks)

2. [**Sequential Unsigned Binary Multiplier (left-shift version)**] Consider the iterative multiplication of two n-bit unsigned integers, $X = \sum_{j=0}^{n-1} x_j 2^j$ and $Y = \sum_{j=0}^{n-1} y_j 2^j$, to form the $2n$-bit product $P = X \cdot Y$. Multiplication proceeds by calculating the partial products (associated with corresponding left-shifts) as: $P_{i+1} = P_i + x_i 2^i Y$ for each bit x_i of the multiplier, with $P_0 = 0$ and $P_n = P$. Design (using Verilog), simulate (using a proper Verilog testbench), and synthesize for any target FPGA platform supported by your version of *Vivado*, an **6-bit sequential unsigned binary multiplier** following the above scheme. The input-side operand registers used in the datpath of your multiplier should have "parallel load" capabilities such that the 6-bit operands can be loaded in each of them instantaneously. Note down the hardware footprint and critical path delay of your synthesized design. The interface of your design should be:
`module unsigned_seq_mult_LS (input clk, input rst, input load, input [5:0] a, input [5:0] b, output reg [11:0] product);`, where the signal names suggest their functionality. (7 marks)

3. [**Sequential Unsigned Binary Multiplier (right-shift version)**] Now, design, simulate, and synthesize for any target FPGA platform supported by your version of *Vivado*, the above multiplier using an alternative scheme that considers right-shifting of the partial products:

$$P_i = P_i + x_j Y \quad \text{and} \quad P_{i+1} = 2^{-1} P_i$$

The interface should be `module unsigned_seq_mult_RS (input clk, input rst, input load, input [5:0] a, input [5:0] b, output reg [11:0] product);`.
Other details remain the same. (7 marks)

4. Finally, submit a small 1-page report (in .pdf format) comparing the maximum speed of operation and hardware footprint of the above three designs. This report should be inside the zipped folder you submit. (2 marks)
