Assignment5 Peripheral Report

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1 Introduction

The block diagram of peripheral along with arbiter and signals for dmem usage alone (LOAD and STORE instr.) is given below (in next page).

1.1 Signals Involved and Logic(State Machine):

Memory map of the peripheral: (BASE=512,acc=accumulator, c=count, ce= chip enable, we= write enable):
1. BASE + 0: Write - reset: write any value here to reset internal sum and count to 0 (acc=0, c=0)-STORE;
2. BASE + 4: Write - value: write a number here to add it to internal sum (acc+=wdata, ce=1, we=1)-STORE;
3. BASE + 8: Read - return the total accumulated sum so far (since last reset)(rdata=acc, ce=1)-LOAD;
4. BASE + 12: Read - return the number of values written so far (since last reset)(ce=1, rdata=c)-LOAD.

The zero state is initial where acc and c are zero. When daddr matching with 512 arrives, it remains there. If daddr=516, it moves to another state with ce=1, we=1 and where accumulation (acc+=wdata(input to dmem)) happens as long as data in inputted. If daddr=512, it returns to original state or if daddr=520, it goes to state three which displays the accumlated sum so far in rdata (with ce=1 and we=0). daddr= 512 returns to reset state, daddr=516 returns to accumulator state and daddr=524 goes to the final state where count output is displayed in rdata.

1.2 Testing:

A sample imemini.mem and dmemini.mem files were created with the following instructions so as to test out the implemented by giving appropriate DMEM daddr:

imem$_ini.mem$:
$00000fb3//0ADDR31, R0, R0$
$800010b7//1.LUIR1, 80001000$
$01000137//2.LUIR2, 01000000$

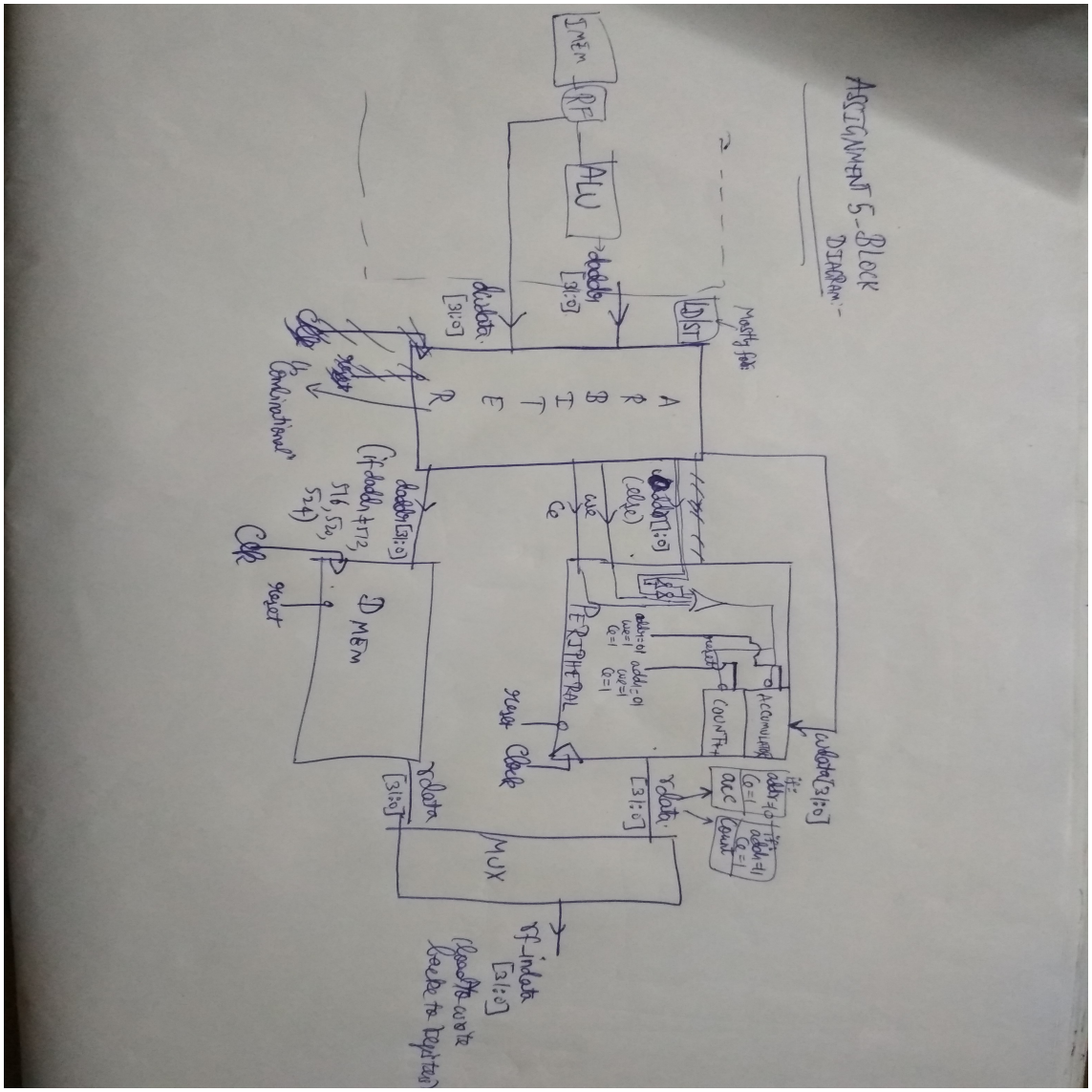

Figure 1: Peripheral Block Diagram along with signals.

$20102023//3.SW512(R0), R1$
$20202223//4.SW516(R0), R2$
$20102223//5.SW516(R0), R1$
$20802183//6.LW520(R0), R3$
$20C02203//7.LW524(R0), R4.Theaboveinitializationemulatesallthe4specificedconditions.$

1.3 Split up of work:

1. Sundar Raman P (EE17B069): Ideation, test bench, testing ini files and arbiter;

2. Pruthvi Raj R G (EE17B114): Ideation, peripheral design, test bench.