ECEN 5593 Advanced Computer Architecture

Initial Proposal

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**Project Description:**

To emulate and synthesize a RISC-V processor using the Nexys A7 board from Digilent (based on the Artix-7 FPGA from Xilinx), and compare the performance between the following:

1. RISC-V implementation without branch prediction
2. RISC-V with simple static prediction
3. RISC-V with a modified dynamic branch predictor

**Project motivation:**

With RISC architecture being the emerging technology for embedded systems and server spaces alike in the future, various implementations have emerged in the market tailored for specific purposes. ARM, for example has a strong (probably a monopoly) foothold in the low-power embedded and mobile processor space, while the Fujitsu designed SPARC ISA dominating the supercomputer market’s processor-of-choice. RISC’s flexible definition and highly scalable architecture allows for use in various industries. This project aims to implement the open-source RISC-V architecture and attempt to improve the overall execution time by exploring various methods of branch prediction, and maybe compare the trade-off in the utilization of logic elements when adding additional logic for branch prediction on an FPGA.

Branch predictors have been around the advent of the first commercial RISC architecture-based processors, and have improved from static implementations to multi-level dynamic predictors. In this project, we plan to implement a variation on the dynamic branch predictor, with variable penalty added to mispredictions, and compare its performance to a simple static and the standard dynamic branch predictor. The platform of choice is the Xilinx’s Vivado Design Suite, a PLD design software to implement the RISC-V architecture as a soft processor. The inbuilt RTL simulator in Vivado IDE is used for RTL level simulation and single-cycle based execution.

**List of tools and hardware:**

1. Vivado IDE (part of Design Suite)
2. Digilent Nexys A7 board
3. Vivado RTL simulator (part of IDE) for simulation
4. Timing Analyzer

**Semester plan:**

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| Week number | Goals to be met |
| Week 3 | Initial proposal report |
| Week 4 | Investigate hardware options and gather materials for literature review |
| Week 5 | Finalize hardware and software tools and architecture port |
| Week 6 | Submit literature review |
| Weeks 7 & 8 | Investigate various synthesis methods to implement processor design and how to integrate benchmarking software with Vivado |
| Week 9 | Finalize base processor design and submit status report 1 |
| Week 10 & 11 | Investigate different hardware implementations for branch predictors. Begin  Implementing various branch predictor designs on Vivado and synthesize. |
| Week 12 | Submit status report 2 |
| Week 13 | Tabulate performance from different versions of branch predictors. |
| Week 14 | Analysis of performance data and generating final report and conference style paper |
| Week 15 | Present final report |