ECEN 5593 Advanced Computer Architecture

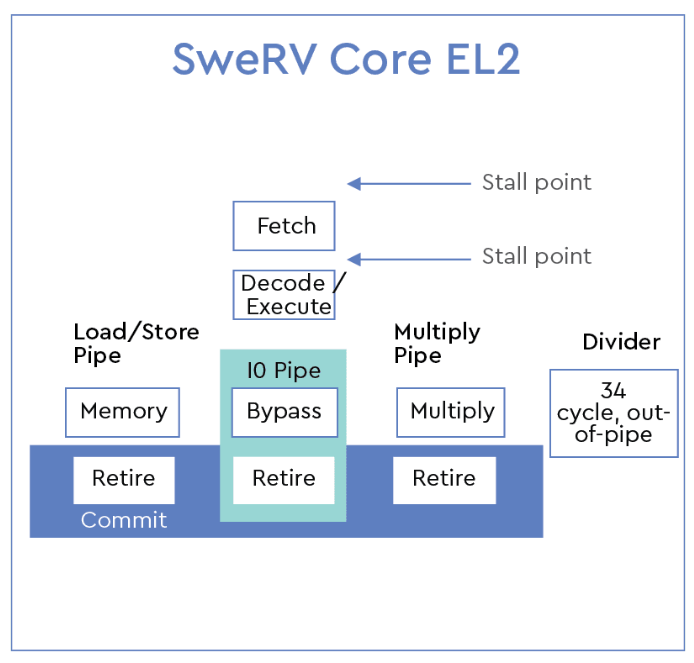
Literature Review

September 2021

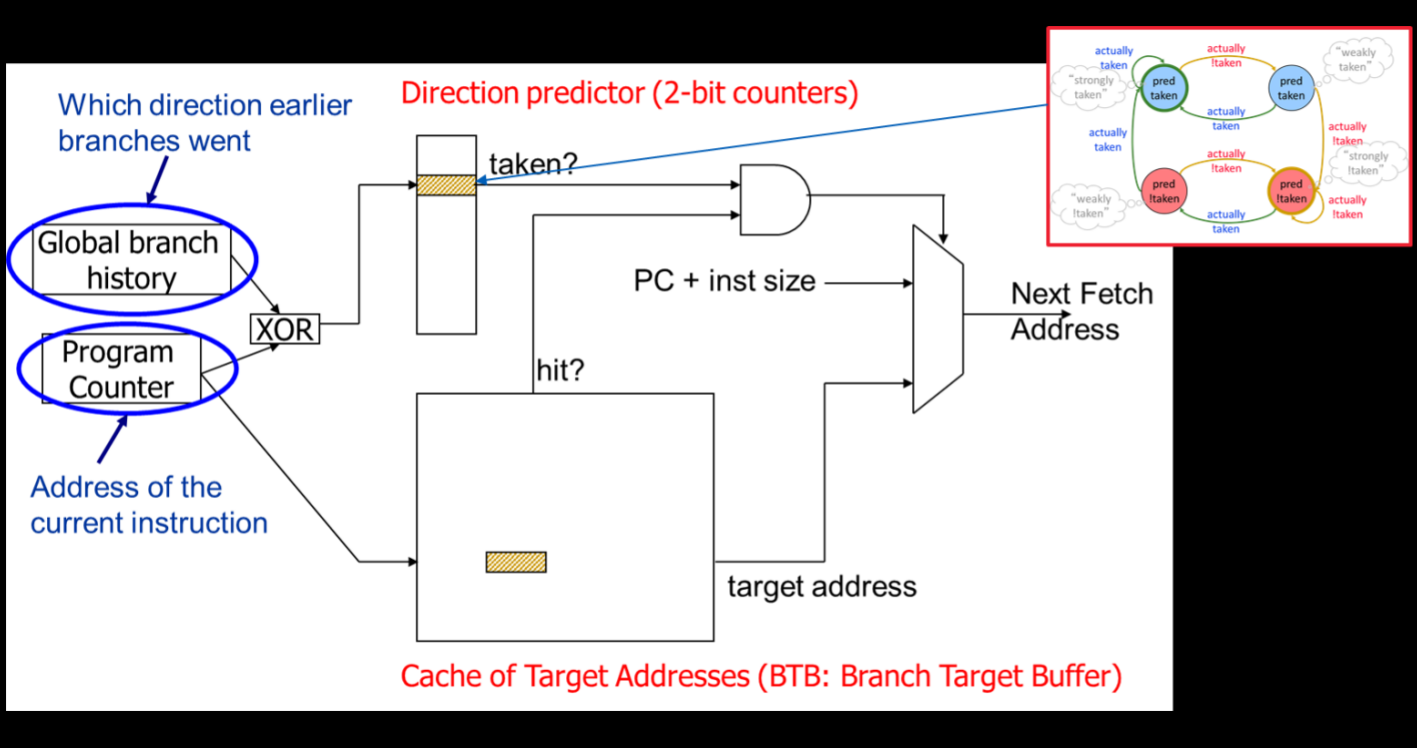
Team Members: Pranav Bharadwaj, Malcolm McKellips

**Project Description:**

The project’s aim is to emulate and synthesis a RISC V processor on the Nexys A7 board from Digilent, using the Artix-7 FPGA from Xilinx. We use this soft processor and compare the performance between different branch predictor setups. The RTL for the RISC-V core is developed by Western Digital, known as the RISC-V SweRV Core Family. We shall be targeting the EL2 core in this family, which has a 4-stage single issue pipeline. This core is based on the RV32I base instruction set with extensions for integer multiplication and division and compressed instructions. The structure of the core pipeline is given below:



The branch prediction of the EL2 core uses the GSHARE architecture with a (2,2) predictor, which involves a 2-bit global history register that keep track of the result of the last 2 executed branches. This value is then XORed with the PC value to create the branch history table. The indexes of the table hold the prediction for the current branch instruction. The counter value is incremented if the prediction holds true, and decremented if not. The working state diagram of this predictor is shown below:



The core IP does not include a RAM by default, but instead provides a memory-bus that can be connected to a memory controller wrapper. Fortunately, the SweRVolf Nexys is a version created for the Digilent Nexys A7 board that uses the on-board 128 MB DDR2 RAM present and supports booting through SPI flash, which allows to modify the bootloader to add modified versions of boot initials. The GPIO of the SweRV core is connected to the board LEDs by default, which allows us to monitor their state during booting.

Our approach is to use the SweRV EL2 core and synthesize it onto the Nexys A7 board, following which we would monitor the performance of the branch predictor by utilising a repetitive set of branch and integer instructions. Since GSHARE is an adaptive branch predictor, we shall compare its performance with a saturated branch predictor and tabulate the results.

References:

* <https://www.westerndigital.com/company/innovations/risc-v>
* <https://riscv.org/wp-content/uploads/2019/04/RISC-V_SweRV_Roadshow-.pdf>
* <https://people.engr.ncsu.edu/efg/521/f02/common/lectures/notes/lec16.pdf>
* <https://github.com/chipsalliance/Cores-SweRV-EL2>
* <https://github.com/chipsalliance/Cores-SweRVolf>