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A Combined Theoretical and Experimental Approach to Deduce the Role of Dielectric Layer on Interface Trap Density in Single Crystal Organic Field-Effect Transistors

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A detailed understanding of charge transport at the interface is necessary to explore the potential of organic field-effect transistors. This can be realized by adequately analyzing the trap states at the interface. In the present work, rubrene-based organic field-effect transistors have been fabricated with three different interfaces. The device properties are used along with a technology computer-aided design to deduce the interface trap density quantitatively. The transfer characteristics are simulated using a double Gaussian density of states and fitted with experimental data by adding traps to the semiconductor dielectric interface. A typical transistor with SiO_2 interface has shown an interface trap density of about $\approx 10^{16}$ cm^{-2}, and it is reduced to 10^{14} cm^{-2} when poly(methyl)methacrylate or polystyrene is coated on SiO_2 interface, attributed to the surface passivation. This approach provides a simple and accurate way to estimate the interfacial traps and offers the possibility to tune the device architecture and performance.

1. Introduction

Organic semiconductors are considered as the potential alternative to current silicon-based inorganic technologies. Due to their high tailorability, ease of synthesis and processing, flexibility, and tunability, organic systems are widely investigated for various applications. Notably, in the recent past, organic electronics-based devices gained much interest in emerging technologies such as portable and wearable electronic sensors, photodetectors, light emitting transistors, and organic lasers.[1–5] In most devices, organic field-effect transistors (OFETs) are used as the basic unit. The gate dielectric layer in OFETs is used to modulate the carrier charge transport in the system and to operate the device effectively.[6] Due to this, defect states that arise between the interface of organic semiconductors and dielectric layers would impact the field-effect mobility of the device. In order to engineer a device, it is essential to understand these charge dynamics at the interface[7–9] (**Figure 1**).

The organic semiconductors, like rubrene and tetracene, can be often grown either in the form of single crystals or thin films. But, the crystals are advantageous as they possess minimal defects and grain boundaries compared to their thin film counterparts, giving rise to better charge transport.[10] The defect states in single crystal OFETs are often induced by two factors:[11] i) intrinsic—such as lattice defects and impurities and ii) extrinsic such as unintentional exposure to gases or radiation, dopants, interfacial effects, bias stress, etc.[12] Often, intrinsic defects are addressed by improving the purity and growth conditions of the organic medium. Whereas in the case of extrinsic factors, proper device engineering is required. Especially in the case of single crystal-based OFETs, semiconductor/dielectric interface plays a crucial role in charge transport.[13] In such a case, the introduction of an additional dielectric layer would improve the field-effect mobility substantially due to the reduction of charge traps at the interface.[14] Organic polymeric layers are widely used in this regard due to their low cost, solution processability, and ease in fabrication.[15] But, in the case of solution-processable organic dielectric layers, there is a limit in attaining a high dielectric constant value (κ) or processing them as a few nm thick layer. In fact, lowering the dielectric layer thickness would introduce pinholes on the surface and lead to a higher leakage current. So, it is essential to study the dielectric layer's composition, surface roughness, and surface energy to properly understand the interface and charge-traps at the interface. This approach will help to model and improve the device's performance. For example, if the significant contribution of trap density is from higher surface roughness at the interface, more efforts can be put forth to smoothen it. Similarly, in the case of observation of large hysteresis, techniques like charge sweeping or using high κ dielectrics can be used to reduce the trap sites.[16] So, before addressing the cause of the issue, it is essential to extract the interface trap sites accurately. Many experimental techniques are available to analyze the interface, such as photoelectron spectroscopy, scanning Kelvin probe measurements, etc.[17] In parallel, many theoretical attempts are also made to simulate and understand

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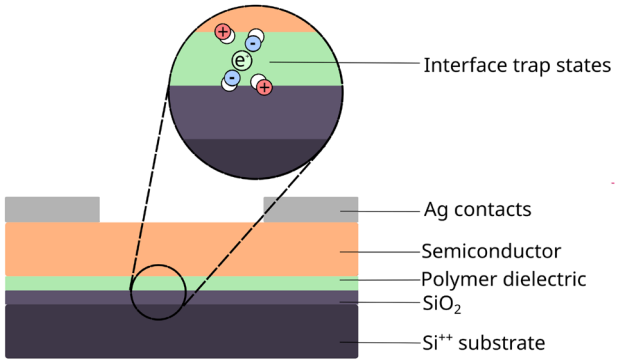

Figure 1. Schematic of the bottom gate top contact OFET architecture device. Usually, multiple traps were created and released at the interface during the device operation.

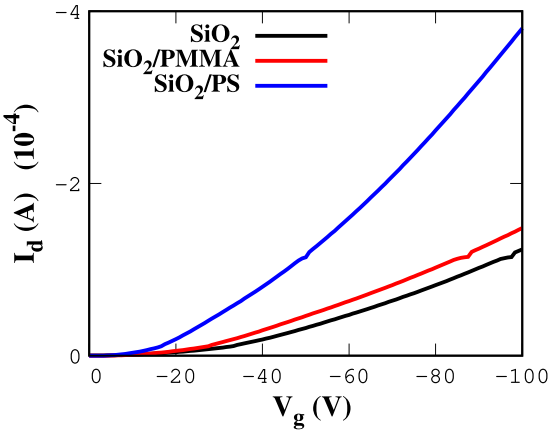

Figure 2. Transfer characteristics of the devices with polymer layers at $V_d = -100$ V.

the interface dynamics.[18] Often, experimental characterizations exclude the disorders that arise due to the complex microstructure, and on the other hand, theoretical analysis misses out on the actual device considerations. So, a combined approach is required to overcome the limitations mentioned above.

In the present work, we have experimentally fabricated a rubrene-based OFET and used its characteristics to simulate the interfacial trap density in the device theoretically. It is a common practice to use polymeric layers as the passivation layers in OFETs fabricated on Si wafers. Here we have substituted two polymeric layers, poly(methyl methacrylate) (PMMA) and polystyrene (PS), with low $\kappa = 3.5$ and 2.5, respectively, on top of SiO_2 and studied their role on trap density. Since our major intention is to device a simple way to deduce charge-traps at the interface of single-crystal and dielectric layer, we have used well-studied rubrene as the semiconductor material. Then, the polymers are chosen based on the fact that they offer better lamination of rubrene single crystals to the Si substrate. In addition to this, low κ of the chosen dielectrics is advantageous resulting lower dielectric loss and broadens the density of states (DOS) to a much lesser degree.[19] We try to deduce the role of surface morphology, hydrophobicity, and the chemical composition of these layers affecting the interfacial traps. The fabricated OFETs are subjected to parametric analysis, and the obtained electrical parameters are used for the theoretical simulation. For this purpose, we used a Gaussian disorder model-based technology computer-aided design (TCAD), which was fitted against the experimental data. The details are discussed in detail in the following sections.

2. Results and Discussions

2.1. OFET Characteristics

Three type of OFETs with different polymeric layers, such as: i) SiO_2; ii) SiO_2/PMMA; and iii) SiO_2/PS are fabricated for the analysis. The fabricated OFETs were subjected to output and transfer characteristics analysis (**Figures 2** and **3**). In order to elucidate the effect of different devices, around five devices were fabricated in each case and their values are averaged for the analysis and discussion. The hole mobility μ was extracted from the saturation regime of the output characteristics, with the drain–source voltage $V_{DS} = -100$ V using the relation below[20]

$$I_{d,sat} = \frac{W}{2L}\mu C_i(V_G - V_{th})^2 \quad (1)$$

where $I_{d,sat}$ is the drain current, W and L are the width and length of the OFET channel, C_i is the capacitance per unit area of the dielectric layer, V_G is the gate voltage, and V_{th} is the threshold voltage. The C_i values were obtained as 11.5, 11.13, and 9.13 nF cm^{-2} for SiO_2, SiO_2/PMMA, and SiO_2/PS, respectively, using a metal–insulator–metal (MIM) capacitor (Figure S1, Supporting Information). The averaged values for the devices are given in **Table 1**. It can be seen that the mobility values improve with the introduction of polymeric layers and PS show a better influence than PMMA in this regard. Similarly, the polymers have positively impacted on device threshold values, and PS shows lower threshold values than the other two systems. The decrease in threshold voltage is an indication of decrease in interface trap density, as higher concentration of traps is responsible for increasing the threshold voltage.

The variation in the mobility and threshold values could be attributed to the decrement in trap concentration at the interface, influenced by the type of passivation layer. To extract the interfacial trap density, the bulk trap density of the devices has to be calculated.[21] This can be estimated from the subthreshold swing S, which is a measurement of how fast the OFET switches from OFF to ON state and calculated from the relation,[22] $S = \frac{dV_g}{d(\log I_d)}$ and measured in V dec^{-1}. The maximum bulk trap concentration is dependent on S as $N_t = \frac{C_i^2}{\epsilon_{sc}q^2}\left(\frac{qS}{kT\ln(10)} - 1\right)^2$, where ϵ_{sc} is the permittivity of semiconductor. The calculated S for the devices are 1.1, 0.89, and 0.92 V dec^{-1} for SiO_2, PMMA, and PS, respectively, which gives N_t in the order of 10^{15} cm^{-3} eV^{-1}. The calculated mobility, threshold (V_{th}), and bulk trap density (N_t^{bulk}) are given in Table 1.

2.2. Theoretical Model for Trap Density Analysis

We have used the extended Gaussian disorder model (EGDM) to describe charge transport in a single crystal OFETs.[23] The model is a combination of Gaussian type DOS and the Miller–Abrahams

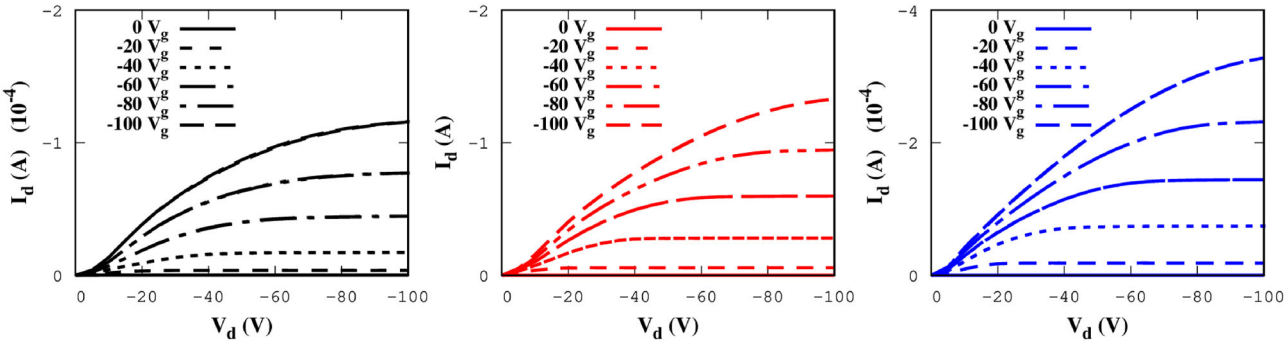

Figure 3. Output characteristics of the devices with polymer layers as: a) SiO_2 only; b) SiO_2/PMMA; and c) SiO_2/PS.

Table 1. Calculated mobility ($cm^2\ V^{-1}\ s^{-1}$), threshold (V_{th} in V), and bulk trap density (N_t^{bulk}) in $10^{15}\ cm^{-3}\ eV^{-1}$, respectively.

Sample	μ_{hole}	V_{th}	N_t^{Bulk}
SiO_2	2.32	−1.36	3.23
PMMA	2.79	−0.69	1.95
PS	3.21	−0.26	1.91

hopping model,[24] which represents the rate of transition from a filled site i to an empty state j

$$\nu_{ij} = \nu_0 \exp\left(-\frac{2r_{ij}}{a} - \frac{\epsilon_j - \epsilon_i + |\epsilon_i - \epsilon_j|}{2kT}\right) \quad (2)$$

where a is the localization length, ν_0 is the attempt to escape frequency ($\approx 10^{12}\ s^{-1}$), r_{ij} is the distance between i and j, ϵ_i and ϵ_j are their corresponding site energies, T is the temperature of the system and k is the Boltzmann constant. In this model, a rigid cubic lattice is introduced, eliminating spatial disorder and giving mobility in the energetic disorder σ. At low electric fields, the mobility is dependent on temperature T, electric field F, and carrier density p as

$$\mu(T, p, F) = \mu_0(T) \times g_1(p, T) \times g_2(F, T) \quad (3)$$

$$g_1(p, T) = \exp\left[\frac{1}{2}(\hat{\sigma}^2 - \hat{\sigma})(2p)^{\delta}\right] \quad (4)$$

$$g_2(F, T) = \exp(0.44(\hat{\sigma}^{3/2} - 2.2))\left[\sqrt{1 + 0.8\left(\frac{eaF}{\sigma}\right)^2} - 1\right] \quad (5)$$

where $\hat{\sigma} = \frac{\sigma}{kt}$ and $\delta = 2(\ln(\hat{\sigma}^2 - \hat{\sigma}) - \ln(ln4))/\hat{\sigma}^2$.

The energetic band structure is given by a double Gaussian DOS, which consists of a primary intrinsic Gaussian DOS and a secondary Gaussian DOS for extrinsic bulk traps used to account for the presence of unintentional dopants. For a donor-like trap density, we get the trap DOS as a function of energy E from HOMO level E_v.[25,26]

$$g(E) = \frac{N_i}{\sigma_i\sqrt{2\pi}} \exp\left(-\frac{(E_v - E)^2}{2\sigma_i^2}\right) + \frac{N_t^{bulk}}{\sigma_t\sqrt{2\pi}} \exp\left(-\frac{(E_v - E + E_d)^2}{2\sigma_t^2}\right) \quad (6)$$

Table 2. Parameters used for the extraction of interfacial trap density.

Parameter	Symbol	Value
Energy gap	E_g	2.19 eV
Electron affinity	E.A.	2.89 eV
Dielectric constant	ϵ_r	3.1 (SiO_2), 3.5 (PMMA), and 2.5 (PS)
Intrinsic total concentration	N_i	$1 \times 10^{21}\ cm^{-3}$
Bulk trap concentration	N_t	$1 \times 10^{15} cm^{-3}$
Intrinsic Gaussian width	σ_i	0.05 eV
Bulk trap Gaussian width	σ_t	0.05 eV
Energy difference between DOS	E_d	0.1 eV
Zero field hole mobility	μ_{0h}	$15.8\ cm^2\ V^{-1}\ s^{-1}$

The shape of the DOS is determined by total intrinsic density N_i, intrinsic degree of disorder σ_i, total bulk trap density N_t^{bulk}, trap degree of disorder σ_t and the energy difference between DOS maximum E_d. For interface trap density, we assumed an exponential donor-like trap DOS and given as[27]

$$h(E) = \frac{N_t^{int}}{kT_c} \exp\left(\frac{E_v - E}{kT_c}\right) \quad (7)$$

From Equation (7), the total trap DOS N_t^{int} and the characteristic temperature T_c help to determine the distribution of interface traps.

2.3. Interface Trap Density Calculations

For the extraction of interfacial trap density, along with the N_t values, other molecular and device parameters such as energy gap, electron affinity, dielectric constant, total intrinsic concentration, intrinsic Gaussian width, bulk trap Gaussian width, the energy difference between the density of states (DOS) and zero field hole mobility are required. These parameters are either experimentally derived or taken from the previous reports and given in **Table 2**.[28,29] We simulate the transfer characteristics using double Gaussian DOS with the EGDM mobility model to extract the interface trap density. The total intrinsic concentration is taken to be an order of $10^{21}\ cm^{-3}$ which is standard for organic semiconductors.[30] For the secondary DOS, the volume or bulk trap concentration is taken as $10^{15}\ cm^{-3}$. The bulk trap

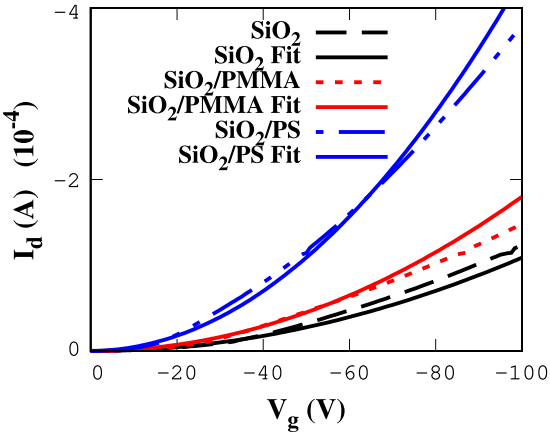

Figure 4. The best theoretical fit to experimental data for the devices.

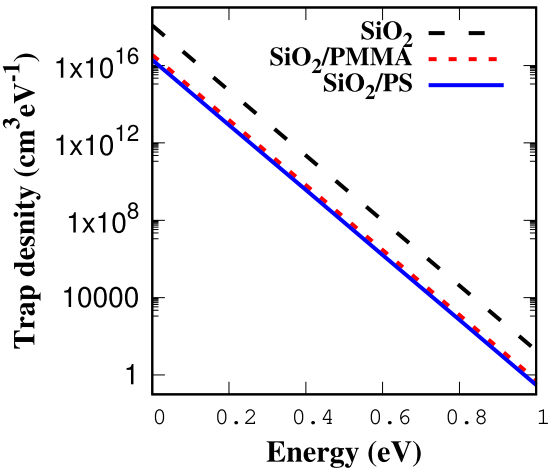

Figure 5. Interface donor-like trap density plotted as a function of energy from LUMO level (E_v) for different interfaces.

concentration is estimated from the subthreshold swing calculations discussed earlier. In the present work, we assumed that the interface trap density has an exponential profile. We simulated the transfer characteristics using the above-mentioned model and compared the characteristics to experimental data. To extract interface trap density, we add donor-like traps until we obtain a good fit for experimental and simulated curves. The best fits are shown in **Figure 4**, and their corresponding trap DOS is plotted in **Figure 5**. The obtained N_t^{int} values are in the order of 3×10^{16} cm^{-2} for SiO_2, 9×10^{14} cm^{-2} for PMMA, and 5×10^{14} cm^{-2} for PS, respectively at $T_c = 300$ K.

It can be seen that the interfacial trap density reduces up to twofold when the passivation layers are introduced. Usually, the semiconductor and the dielectric layer influence these interface trap sites. In the case of semiconductors, the presence of impurities in the active medium would disturb the crystal lattice and eventually alter the bandgap.[31] Also, the surface morphology would induce local variations in the transfer integrals and may cause molecular misalignment.[32] To elucidate these two factors, we have improved the quality of the crystal by recrystallization process about thrice. In the present case, grown crystals were collected and reused as the source for this purpose. So, the role of molecular impurity would have a negligible impact on trap density. Further, the surface roughness of the dielectric layer plays a dominant role in the performance of OFETs as they can impede the flow of charge at the interface and reduce the mobility of the OFET.[33,34] In the present case, the surface roughness of the dielectric layers are characterized using atomic force microscopy (AFM) and given in **Figure 6**. The calculated root mean square roughness values are 0.5, 0.8, and 1.4 nm for PMMA, PS, and SiO_2, respectively. The values are negligibly low and indicate the minimal effect on charge transport.

Hydrophobicity is another essential factor affecting charge transport on the semiconductor dielectric interface.[35,36] Water can react with functional groups present on the dielectric interface to form charge trapping sites like hydroxyl groups.[37] The affinity for water can be derived from the water contact angle (θ) measurements for the different dielectrics. The calculated contact angles (see Figure S3, Supporting Information) for all three dielectrics are 54°, 82°, and 81° for SiO_2, PMMA, and PS, respectively. The high hydrophilic behavior of SiO_2 indicating a high probability of reaction with water to form hydroxyl charge trap sites.

In other words, devices with no polymer dielectric have a high concentration of donor-like traps, particularly in shallow states due to the surface contamination[12] (**Figure 7**). For deeper energy states, the trap density decreases sharply, denoted by the low T_c of 300 K. The interface traps in dielectrics are often attributed to dangling bonds which, when reacting with water, can form hydroxyl groups that act as charge trapping sites.[38] The presence of dangling oxygen bonds and the high hydrophilicity of SiO_2 gives rise to a much higher number of traps than the polymer dielectrics, even in deeper energy states. In the case of PMMA and PS, PMMA shows a slightly higher number of traps than PS. Even though PS and PMMA have comparable water contact angles, the presence of oxygen atoms in PMMA molecules can lead to the formation of some charge trapping hydroxyl groups.[39] On the other hand, PS has chemically inert benzene rings as their functional groups leading to formation of less number of traps.[37,40] In both cases, the trap states approach zero at deeper states (≈1 eV), indicating trap-free charge transport.

3. Conclusion

Interfacial trap states played a vital role in charge transport in OFETs. In the present work, we have combined both experimental and theoretical approaches to calculate the trap density values. For this purpose, rubrene-based OFET was used as the test bed with three different dielectric layer configurations, such as i) bare SiO_2 and the SiO_2 with passivation layers, ii) PMMA, and iii) PS were used. The devices were subjected to output and transfer characteristics, from which the mobility and threshold values are calculated. It was observed that the mobility value increases and threshold value decreases with the introduction of polymers, and PS shows better results than that of the PMMA. Further, using experimental analysis, the bulk trap density of the devices was calculated. A Gaussian disorder model was used for the extraction of interfacial trap density. For this purpose, the experimental data were fitted to the theoretical curve till a best fit was obtained. The results follow a similar trend as the mobility values, indicating the influence of trap states on carrier charge transport.

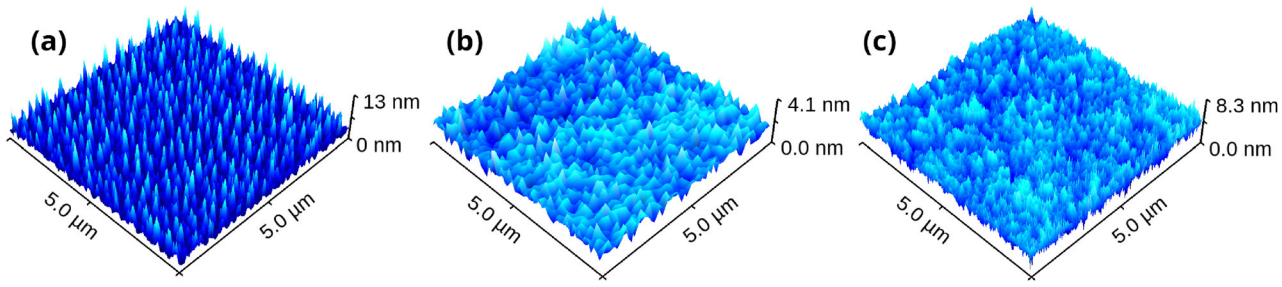

Figure 6. AFM images for: a) SiO_2; b) SiO_2/PMMA; and c) SiO_2/PS.

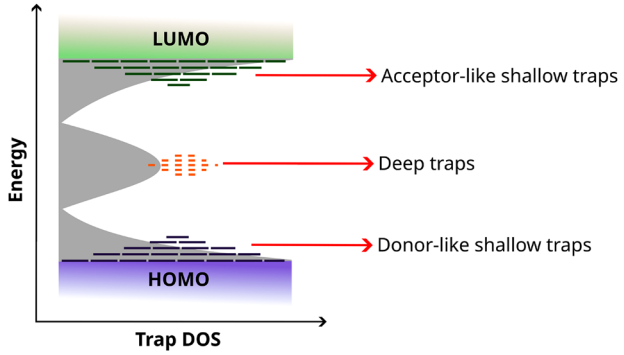

Figure 7. Dynamics of different trap sites when an electric potential is applied. Introduction of polymer layer helps to reduce the donor-like shallow traps greatly.

The origin of the trap states could be interpreted as the surface contamination effects where SiO_2 is more prone than that of PS and PMMA. Chemical inertness and hydrophilic nature resulted in lower trap densities in the case of polymers. The present approach can be directly used to model interfacial trap states for any combination of organic semiconductors and dielectrics, and to engineer an effective device.

4. Experimental Section

Materials Used: Rubrene (99.99% purity), poly(methyl methacrylate) (PMMA), and polystyrene (PS) were purchased from Sigma Aldrich and used for the experiments without any further purification.

Crystal Growth: Rubrene single crystals were grown by utilizing a three-zone physical vapor transport system. In order to avoid the presence of any minor impurities, the grown crystals were recrystallized thrice. The crystals were grown in an inert gas atmosphere and the selected crystals were transformed into a glove box once the final round of growth was completed.

Fabrication of OFET: The p-doped silicon wafers are used as the substrates with a 300 nm SiO_2 layer as the dielectric layer. No additional buffer layers were used for the first set of samples and then crystals were electrostatically laminated directly on the dielectric layer. Then, the samples were loaded into a thermal evaporator attached to the glovebox and silver contacts of thickness 100 nm were deposited by evaporation at an average pressure of about 10^{-7} Torr. Further, PMMA and PS were used to fabricate the second and third sets of samples. The prepared polymeric solution was coated as thin layers of about 50 nm on the SiO_2/Si substrate by spin coating. Then the crystal lamination and contact fabrication steps were repeated.

Electrical Characterization: The fabricated OFET devices were subjected to transfer and output characteristics analysis using a parametric analyzer (Keysight B1500A). For this purpose, the samples were connected to the micromanipulators inside the glovebox and covered by a black cloth to do the measurements without any light-induced effects.

AFM and Contact Angle Measurements: The surfaces of the polymer dielectric thin films were analyzed by AFM (Park Systems NX 10) in tapping mode. The contact angles of the polymer dielectric films with distilled water were measured using a Holmarc Contact Angle Meter (Model No: HO-ED-M-01).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Data Availability Statement

The data that supports the findings of this study are available in the supplementary material of this article.

Conflict of Interest

The authors declare no conflict of interest.

Keywords

charge transport, Gaussian disorder model, interfacial traps, organic field effect transistors, trap density calculation

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