

TLM 2.0 Approximately Timed (AT) System Example - Annotated Timing Only

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AT System Example - Annotated Timing

The Goal is to Illustrate:

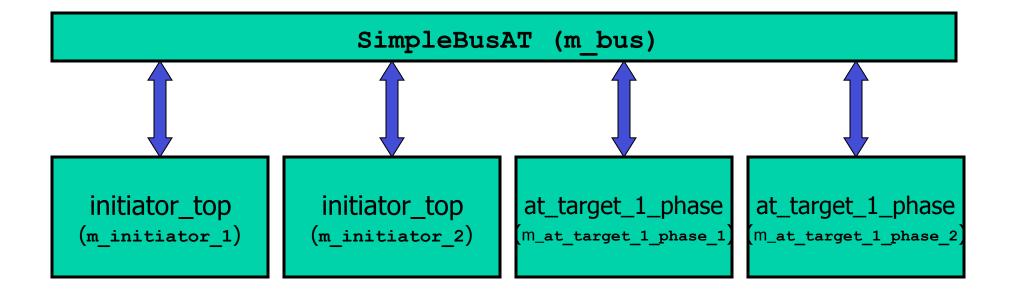
- Application of TLM 2.0 in a real system
- Annotated non-blocking (NB) option of the non-blocking style
 - NB annotated timing has been referred to as "1 phase"
 - Simplest version of non-blocking/AT

Possible Applications:

- Architectural exploration
- Early software development



Example Block Diagram







How to run this example (Linux)

- Set SYSTEMC HOME and TLM HOME
- cd examples/tlm/at_1_phase/build-unix
- make clean
- make
- make run



How to run this example (MSVC)

- Open a explorer window on examples/tlm/at_1_phase/build-windows
- Launch at_1_phase.sln
- Select 'Property Manager' from the 'View' menu
- Under 'at_1_phase > Debug | Win32' select 'systemc'
- Select 'Properties' from the 'View' menu
- Select 'User Macros' under 'Common Properties'
- Update the 'SYSTEMC' and 'TLM' entries and apply
- Build and run

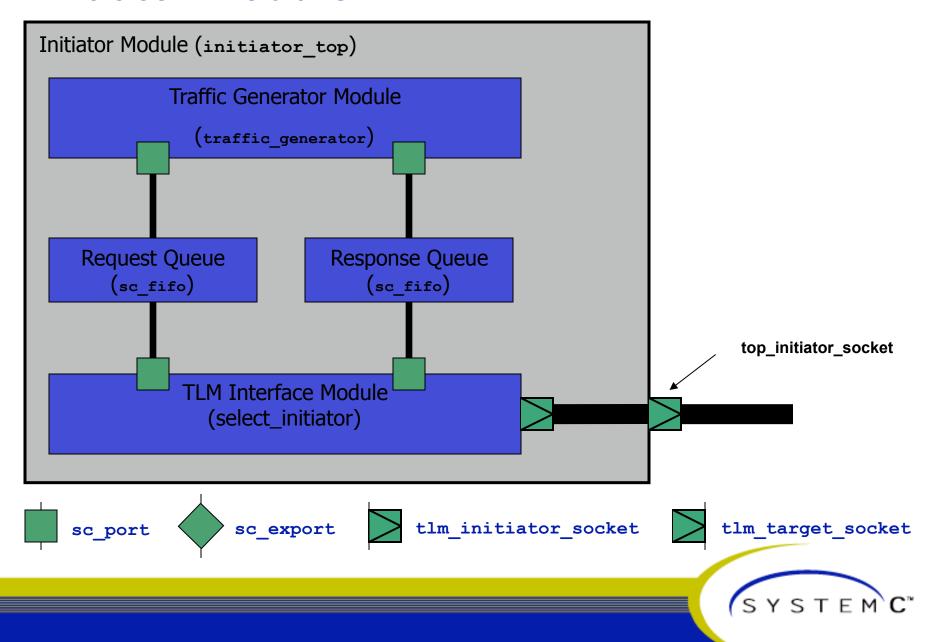


Expected Output (expected.log)

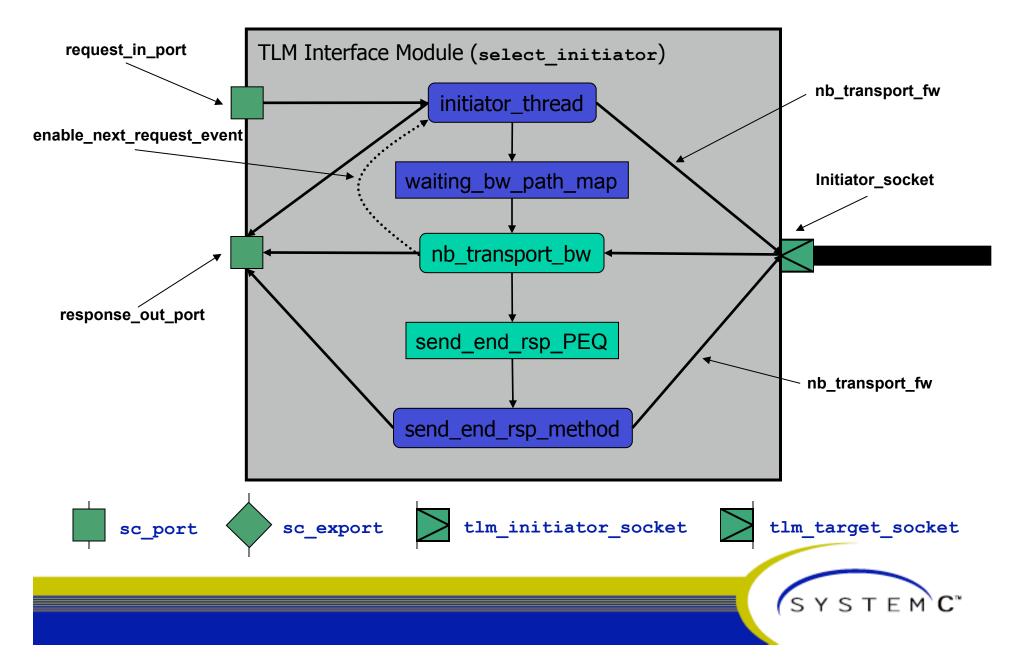
```
Info: traffic_generator.cpp: 0 s - traffic_generator_thread
   Initiator: 101 Starting Traffic
Info: select initiator.cpp: 0 s - initiator thread
   Initiator: 101 starting new transaction for Addr:0x00000100
   Initiator: 101 nb_transport_fw (GP, BEGIN_REQ, 0 s)
Info: select initiator.cpp: 0 s - initiator thread
   Initiator: 101 ACCEPTED (GP, BEGIN REQ, 0 s)
   Initiator: 101 transaction waiting end-request on backward-path
Info: at target 1 phase.cpp: 0 s - nb transport fw
   Target: 201 nb transport fw (GP, BEGIN REQ, 0 s)
Info: memory.cpp: 0 s - print
   ID: 201 COMMAND: WRITE Length: 04
   Addr: 0x0000000000000100 Data: 0x00000100
Info: at target 1 phase.cpp: 0 s - nb transport fw
   Target: 201 COMPLETED (GP, BEGIN REQ, 40 ns)
Info: select initiator.cpp: 40 ns - nb transport bw
   Initiator: 101 nb transport bw (GP, BEGIN RESP, 0 s)from Addr:0x00000100
   Initiator: 101 target omitted end-request timing-point returning ACCEPTED
```



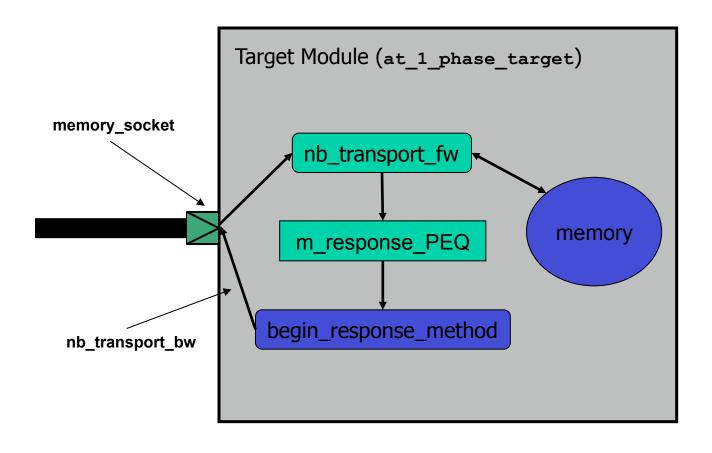
Initiator Module



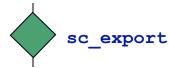
TLM Interface Module

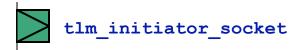


Target Module





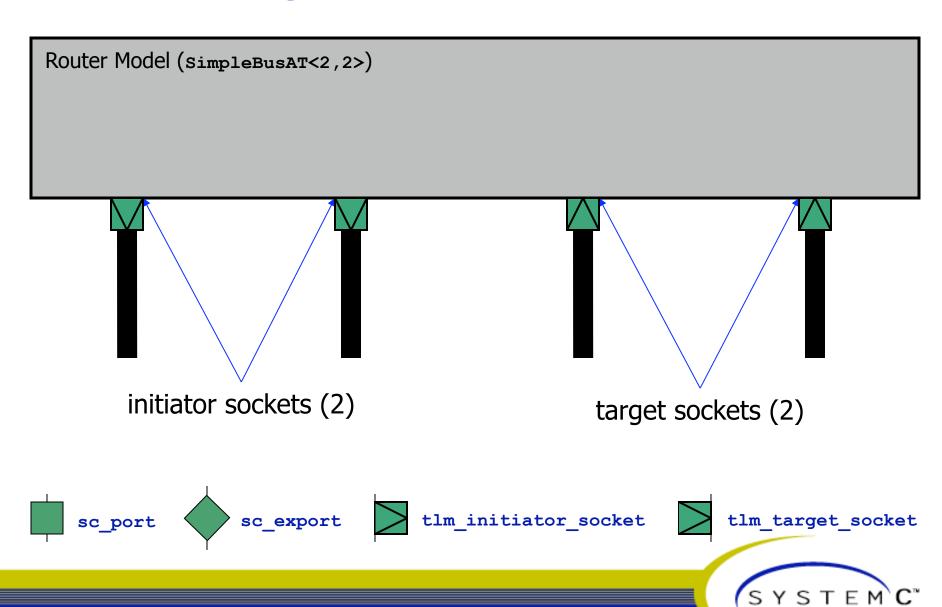








Router Component



Expected Timing

