

# Sai Kishore Pottabatini

H.no:5-5-134/12,Mustafa nagar,Khammam



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## Career Objective :

Looking forward for a challenging career opportunity to excel and grow in good organisation where I can use my knowledge, experience & potential at maximum for mutual benefits.

## Academic Profile :

COURSE	YEAR	COLLEGE/UNIVERSITY	PERCENTAGE
B.Tech (EEE)	2013-17	Malla Reddy Engineering College	62.3%
Intermediate(MPC)	2011-13	Krishnaveni College	79%
SSC	2010-11	Triveni talent school	89%

## Professional Qualificaion :

Advanced VLSI Design and Verification course

Maven Silicon VLSI Design and Training Center, Bangalore January 2019 to December 2019.

## Project :

SPI Controller Core - Verification

HVL: System Verilog

TB Methodology: UVM

EDA Tools: Riviera Pro - Aldec

Description : The SPI IP core provides serial communication capabilities with external device of variable length of transfer word. This core can be configured to connect with 32 slaves.

### Responsibilities:

- Architected the class based verification environment in UVM
- Defined Verification Plan
- Verified the RTL module using UVM
- Generated functional and code for the RTL verification

### Activities :

- Participated in flash mob as a part of VISHESH-2014 FEST on 15th September at Malla Reddy Engineering College.
- Coordinated an event as a part of AKSHARA-2016 (National level Techno-Cultural fest) on 11th march 2016 at Malla Reddy Engineering College.

### Hobbies :

- Playing Cricket and Badminton.
- Watching movies.

### Personal Details :

Date of Birth : 29th june 1995

Father : P.Venkateswarlu

Mother : P.Saritha

Languages Known : Telugu , English , Hindi

Present address : Plot no:149 , gowri shankar colony , M.G road , Secunderabad. .

### Declaration :

I here by declare that the above mentioned information is true to the best of my knowledge.

Date:

Place: Secunderabad

P.SAI KISHORE