Seminar 2
Processor Design

Computer Organization and Components / Datorteknik och komponenter (IS1500), 9 hp
Computer Hardware Engineering / Datorteknik, grundkurs (IS1200), 7.5 hp

KTH Royal Institute of Technology

Introduction

The purpose of seminars is to enable active learning of the more theoretical tasks that are typically part of the final written exam. Seminars are optional. However, we strongly recommend that you perform these seminar exercises and attend the seminar.

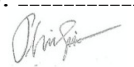
Rules. You may receive up to 1 extra point on the fundamental part of the written exam if:

- you make an honest *attempt* to solve *all* the seminar exercises on your own. You may discuss the exercises with your friends, but you are not allowed to copy any solutions from anyone or anywhere. You need to have written down a potential solution on all assignments. You are not allowed to skip some exercises, you need to try to provide a solution for all exercises.
- you write down your solutions *by hand* on this exercise form. You are not allowed to hand in machine printed solutions, copies, or handwritten solution on another paper format.
- you bring your solution *personally* to the seminar and attend the whole seminar. This means that you are not allowed to hand in a solution on behalf of someone else.
- you need to have signed this form before you hand it in.
- you are not allowed to attend the seminar if you are not bringing a solution, that is, if you do not bring this form filled out with your own solutions, you cannot attend the seminar.
- you must come to the seminar on time when it starts. If you are not there from the beginning, the assistants may refuse that you participate in the seminar.

Note that the extra point is only valid on the next ordinary exam, and the following two retake exams. During the seminar, the teaching assistant or teacher will go through the solutions and you will correct the solution done by another student. You need to have received at least 50% of the total number of points to pass the seminar. In such a case, you get one extra bonus point on the exam. We recommend that you take a photo of your solutions before you hand it in.

By signing the following, I hereby guarantee that I follow the rules above.

Your name (printed): Philip Salqvist

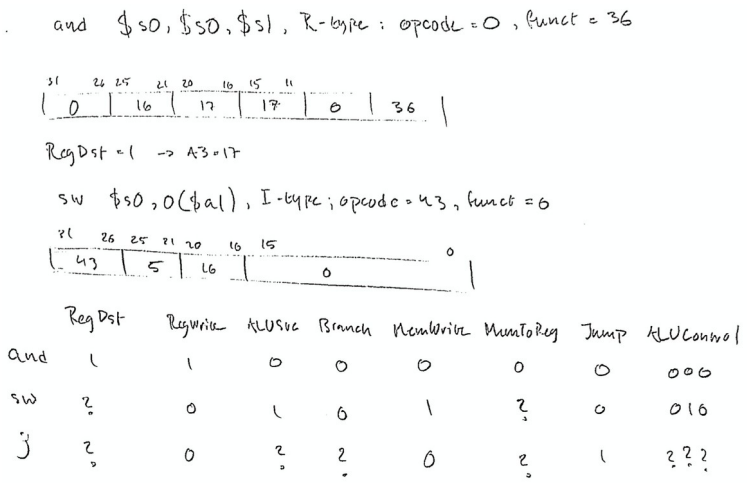
Signature: 

Date: 2021-02-10

Exercises

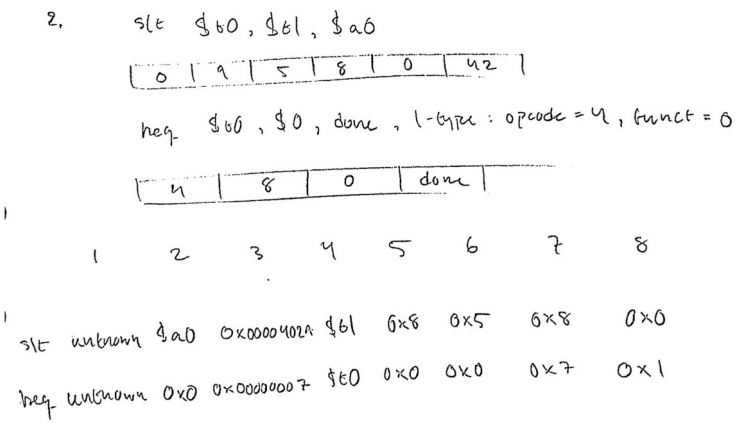
1. Consider the datapath in Figure 1 and the program code in Listning 1 on the last page. Assume that the ALU corresponds to the one presented in Lecture 9, with the extension of a zero signal output. When signal *Inst* corresponds to the machine code for the instructions on code lines 7, 8, and 11, what are then the values of the 8 control signals *Jump*, *RegWrite*, *RegDst*, *ALUSrc*, *ALUControl*, *Branch*, *MemWrite*, and *MemToReg*, for each of these instructions? Answer with either the concrete signal value or with a question mark (?) when it does not matter what the signal value is.

   Your solution:



2. Consider again the datapath in Figure 1 and the program code in Listning 1 on the last page. For each of the code lines 3 and 4, when *Inst* has the corresponding machine code value of these code lines, state the values of the eight signals marked as black filled circles. If the signal has a uniquely defined value, (independent of the loop iteration) state that value as a hexadecimal number. If the value is always located in a specific register, (e.g., `$t0`) then state the register name (e.g., `$t0`). Otherwise, state that the signal value is unknown.

   Your soluti



3. Assume that a processor with a 5-stage pipeline executes at 80 MHz and that the processor can fetch at most 1 instruction in each clock cycle.

   (a) How long is then the clock period?

   (b) Which of the following alternatives is correct: i) The CPI is always larger or equal to 1, ii) the CPI is always smaller than 1, or iii) the CPI is always equal to 1.

Your solution:

a) $T_c = \frac{1}{f_c} = \frac{1}{8 \cdot 10^6} = 0,0000125$ ms

b) i)

4. Assume that we have a MIPS processor with a 5-stage pipeline. Consider the MIPS assembly code below. Explain which instructions that cause a hazard and what kind of hazards these are. State how the hazards can be solved for the different cases. You should suggest the best possible solution, that is, that results in that the code takes as few clock cycles as possible to execute.

```
1          lui     $s0,0x1001
2          addi    $t0,$0,10
3          sw      $t0,12($s0)
4          lw      $t1,8($s0)
5          and     $t0,$t0,$t1
```

Your solution:

The sw instruction uses register $t0, which is not written to by addi until W. sw needs $t0 already during D, so we use forwarding to resolve this data hazard. Furthermore, the result of lw is not in $t1 until the end of M, but the result is needed in the beginning of the E-stage for the and instruction. We use stalling and forwarding to resolve this data hazard.

5. A `bne` instruction can result in a specific kind of hazard.

   (a) What is this kind of hazard called?

   (b) How can such hazard be solved?

   (c) For deep pipelines, such hazards can have very negative impact on the performance. Explain why.

   (d) Which technique is used in modern processors to remedy this negative impact? Motivate why this is the case.

   Your solution:

a) control hazard

b) Move equality comparison and branch address's calculation to the decode stage to reduce misprediction penalty. Although this can introduce a new hazard which can be resolved using stalling and forwarding.

c) If number of pipeline stages increase the branch misprediction penalty increases

d) We can use static Branch Predictors or Dynamic Branch Predictors to statistically determine if a branch is taken or not.

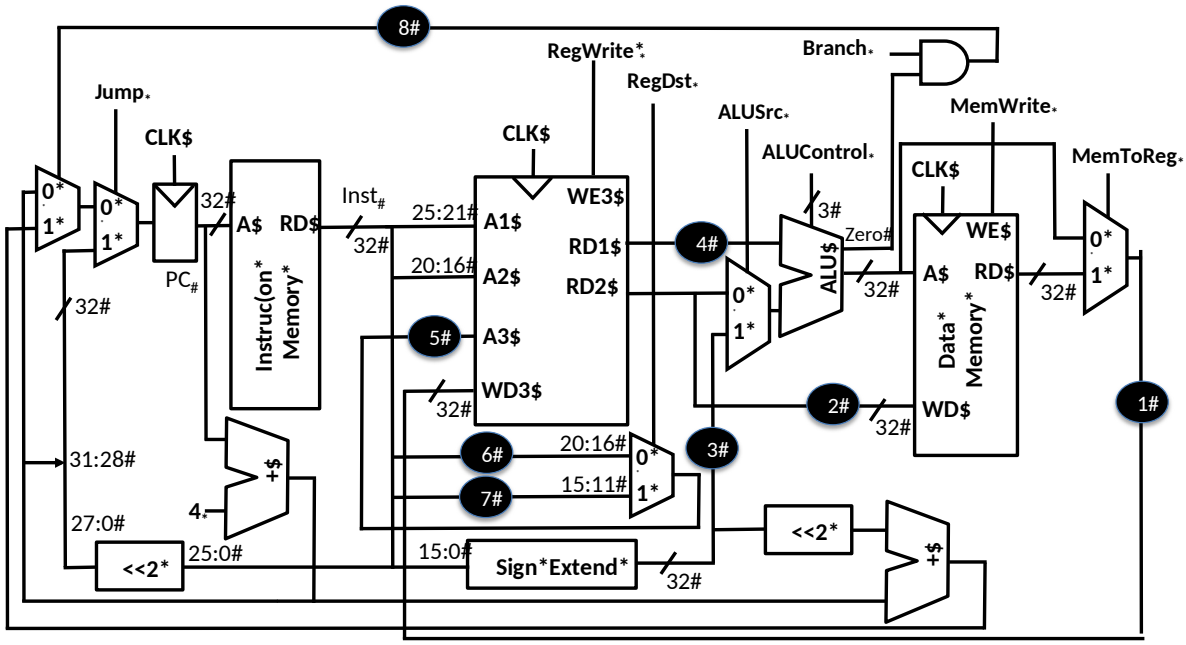
6. State 6 differences or similarities between the ISAs ARM v7, x86, and MIPS.
   Your solution:

1. ARM/MIPS are RISC processors while x86 is CISC.
2. x86 generally have better performance than ARM & MIPS
3. Because of RISC, ARM/MIPS have better power efficiency than x86.
4. ARMv7 is more popular embedded devices while x86 is more popular in laptops, PCs and cloud
5. x86 have 8 general purpose registers while ARM have 16 registers
6. x86 requires more complex than MIPS/ARM.

Corrected by _____. Total number of points: _____

The following figures are used in the seminar exercises above. You need these figures to solve the exercises, but you do not have to print these figures and bring them to the

Figure 1.



Listning 1.

```
1           addi    $t1,$0,0
2   loop:
3           slt     $t0,$t1,$a0
4           beq     $t0,$0,done
5           lw      $s0,4($a1)
6           lw      $s1,8($a1)
7           and     $s0,$s0,$s1
8           sw      $s0,0($a1)
9           addi    $a1,$a1,-12
10          addi    $t1,$t1,1
11          j       loop
12  done:
```