a) control hazard

b) Move equality comparison and branch address calculation to the decode stage to reduce misprediction penalty. Although this can introduce a new hazard which can be resolved using stalling and forwarding.

c) If number of pipeline stages increase the branch misprediction penalty increases

d) We can use static Branch Predictors or Dynamic Branch Predictors to statistically determine if a branch is taken or not.

1. ARM/MIPS are RISC processors while x86 is CISC.
2. x86 generally have better performance than ARM & MIPS
3. Because of RISC, ARM/MIPS have lower power efficiency than x86.
4. ARMv7 is more popular embedded devices while x86 is more popular in laptops, PCs and cloud
5. x86 have 8 general purpose registers while ARM have 16 registers
6. x86 requires more complex than MIPS/ARM.