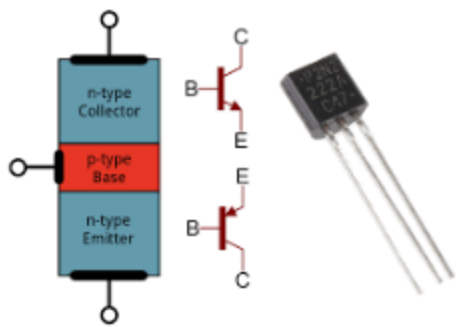
KLE Technological University

Creating Value
Leveraging Knowledge

Basic Electronics
18EECF101

Unit: I

Chapter 3:Transistor



Topic Learning Outcomes

At the end of the topic, students should be able to:

1. Discuss on the transistor CE configuration.
2. Explain significance of DC load line and operating point.
3. Realize the simple applications using transistor.

CO-2: Describe the characteristics of semiconductor devices and their applications in rectifiers, switches, regulators and gates.

Key concepts

1. Transistor construction and operation
2. Transistor voltages and currents
3. Common emitter input and output characteristics
4. DC Load line & Q Point
5. Transistor biasing
6. Base bias circuit
7. Collector base circuit
8. Voltage divider circuit
9. Transistor as switch: NOT gate and DTL NAND gate

Bipolar Junction Transistors

William Shockley invented the first junction transistor, a semiconductor device that can amplify electronic signals such as radio and television signals.

It is an essential ingredient of every electronic circuit, from the simplest amplifier or oscillator to the most elaborate digital computer.

Thus understanding of transistor is very important.

The amplification in the transistor is achieved by passing the signal from a region of low resistance to a region of high resistance .This concept of transfer of resistance has given the name transistor.

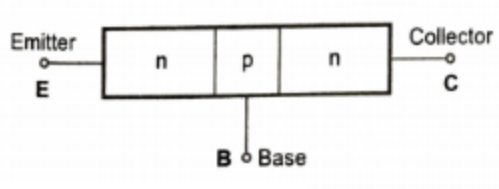
The current conduction in bipolar transistors is because of both the types of charge carriers, holes and electrons. Hence it is called Bipolar Junction Transistors (BJT)

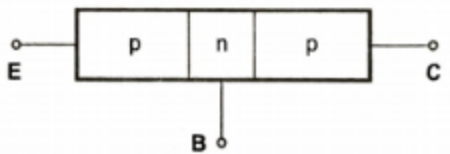
Bipolar Junction Transistors

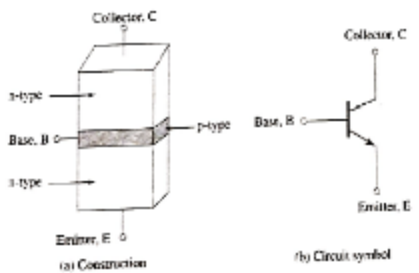
BJTs are basically of two types: an n-p-n and p-n-p type.

When the transistor is formed by sandwiching a single p-region between two n regions its is (a) npn type transistor.

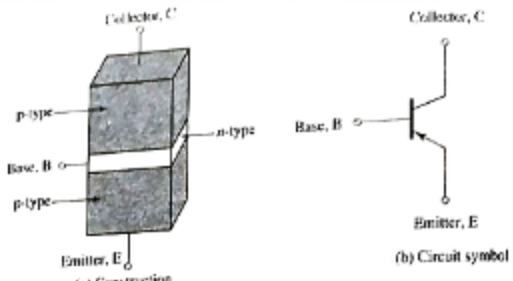
The pnp type has single n region between two p regions.







npn transistor.



pnp transistor.

Construction

The middle region of each transistor type is called base of the transistor. This region is very thin and lightly doped.

The remaining two regions are called emitter and collector.

The emitter and collector are heavily doped .

But the doping level in emitter is slightly greater than that of a collector.

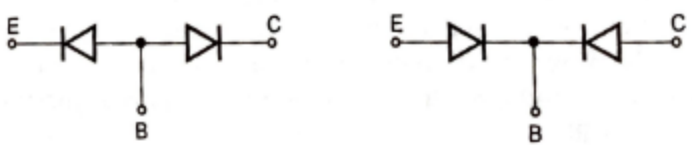
Collector region- area is slightly more than that of a emitter.

Unbiased-transistor

A transistor has two p-n junctions. One junction is between the emitter and the base and is called the emitter-base junction(J_E)

The other junction is between the base and collector and is called collector-base junction, J_C.

Thus the transistor is like two p-n junction diodes connected back-to-back.



(a) npn transistor (b) pnp transistor

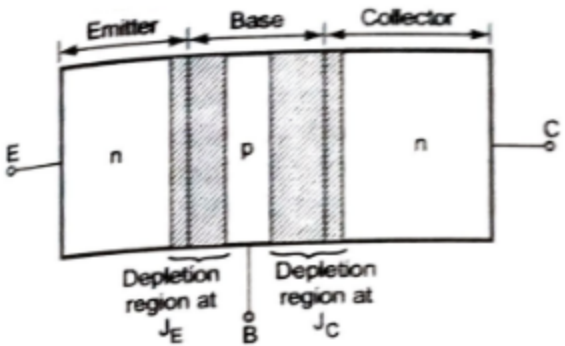
Two-diode transistor analogy

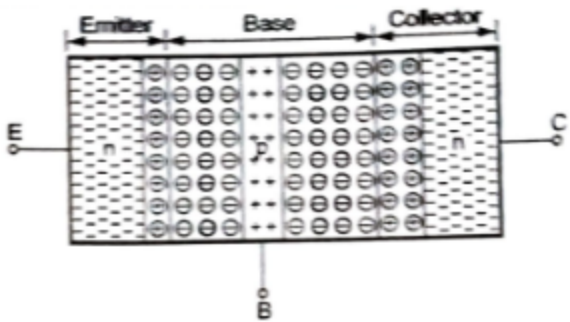
Unbiased-transistor

An unbiased transistor means a transistor with no external voltage is applied

Since transistor is like the two pn junction diodes connected back-to-back, there are depletion regions at the both junctions, emitter junction and collector junction.

But because of different doping levels in the three regions, two depletion regions do no have same width





Biased Transistor

In order to operate transistor properly as a amplifier, it is necessary to correctly bias the two pn junctions with external voltage.

Depending upon external bias voltage polarities applied , the transistor works in one of the three regions

1) Active region 2) Cut-off region 3) Saturation

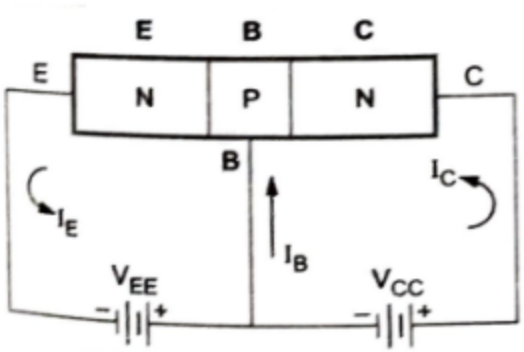
Region	Emitter base junction	Collector base junction
Active	Forward biased	Reverse biased
Cut-off	Reverse biased	Reverse biased
Saturation	Forward biased	Forward biased

Transistors work as an amplifier while they **work** in the active **region**.

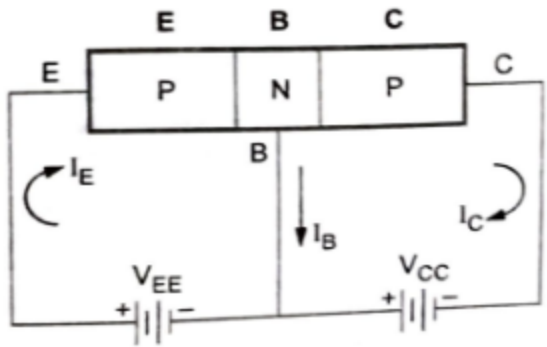
Biased Transistor

To bias the transistor in its active region, the E-B junction is forward biased and C-B junction is reverse biased.

Depending upon external bias voltage polarities applied , the transistor works in one of the three regions



(a) npn



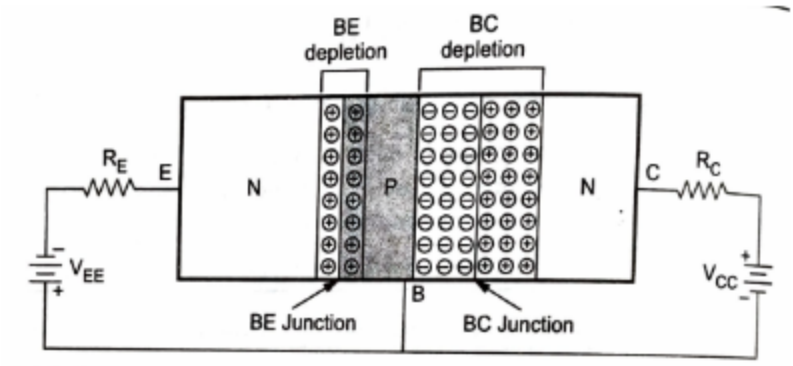
(b) pnp

Working-Biased Transistor

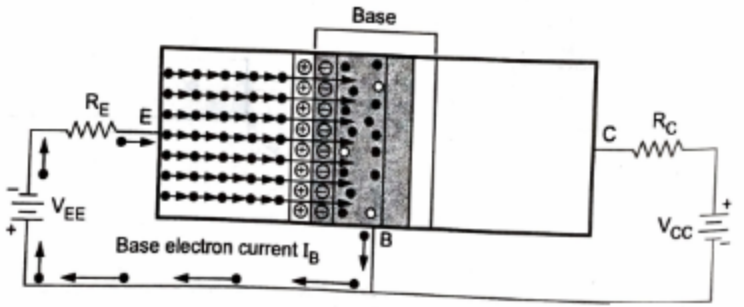
Let us consider the npn transistor for our discussion!!!!!

The B-E junction is FB by the dc source V_{EE}. Thus, the depletion region at this junction is reduced.

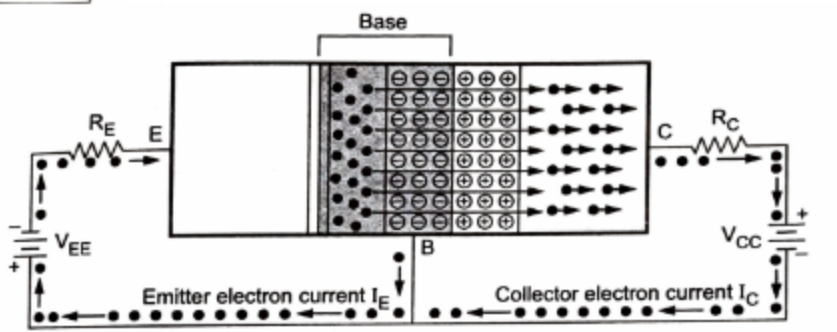
The C-B junction is RB, increasing depletion region at C-B junction.



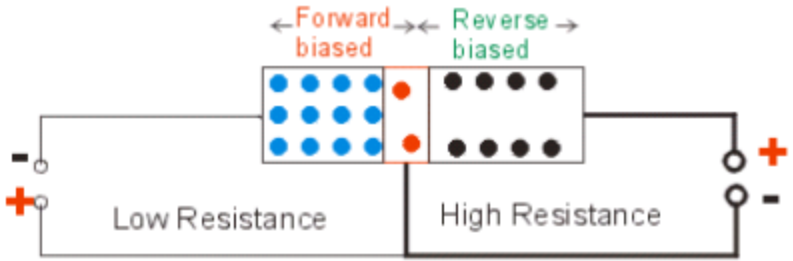
Working-Biased Transistor



$$I_E = I_B + I_C$$



Working



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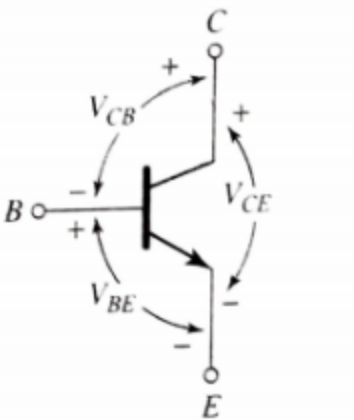
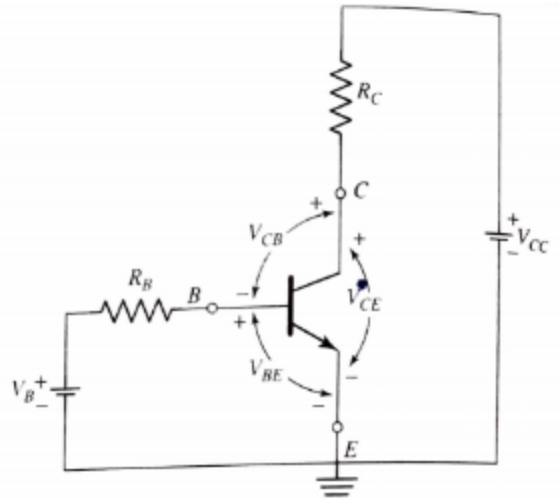
Transistor Voltages n-p-n type

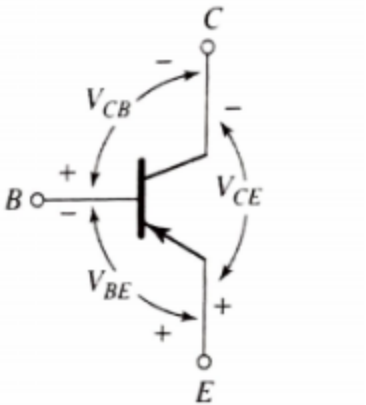


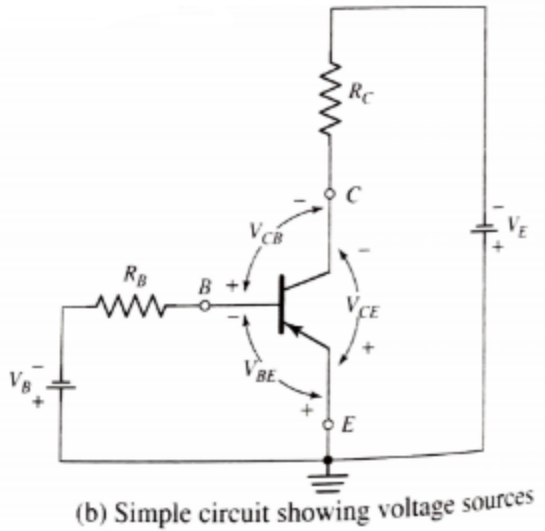
(a) Terminal voltages



(b) Simple circuit showing voltage sources

Transistor Voltages p-n-p type





α and β of transistor

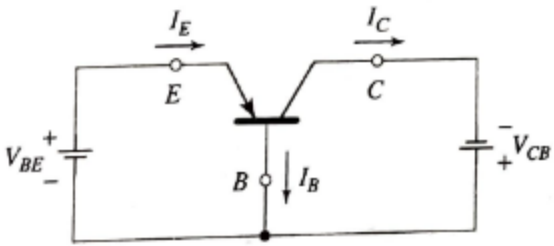
The current gain in the common-emitter circuit is called Beta (β). Beta is the relationship of collector current (output current) to base current (input current). To calculate beta, use the following formula :

$$\beta = \frac{I_C}{I_B} \qquad \beta \text{ ? 25 to 300}$$

The current gain in the common-base circuit is calculated in a method similar to that of the common emitter except that the input current is I_E not I_B and the term Alpha (α) is used in place of beta for gain. Alpha is the relationship of collector current (output current) to emitter current (input current). Alpha is calculated using the formula :

$$\alpha = \frac{I_C}{I_E} \qquad \alpha < 1$$

Equation of I_C in terms of I_B and α_{dc}



$$\therefore\ I_E = I_C + I_B$$

$$\alpha_{dc} = \frac{I_C}{I_E}$$

or $\quad I_C = \alpha_{dc} I_E$

Obtain the relationship between α_{dc} and β_{dc}.

$$I_C = \frac{\alpha_{dc}}{1-\alpha_{dc}} I_B$$

$$\frac{I_C}{I_B} = \frac{\alpha_{dc}}{1-\alpha_{dc}}$$

$$\beta_{dc} = \frac{I_C}{I_B}$$

$$\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}$$

Find β_{dc} in terms of α_{dc}.

$$\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}$$

or $\beta_{dc}(1-\alpha_{dc}) = \alpha_{dc}$

$$\beta_{dc} - \beta_{dc}\alpha_{dc} = \alpha_{dc}$$

$$\beta_{dc} = \alpha_{dc} + \beta_{dc}\alpha_{dc}$$

$$= (1+\beta_{dc})\alpha_{dc}$$

$$\therefore \alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}}$$

Problems

Calculate the values of I_C, I_E and β_{dc} for a transistor with $\alpha_{dc} = 0.98$ and $I_B = 120\ \mu A$.

$$I_C = \frac{\alpha_{dc}}{1 - \alpha_{dc}} I_B$$

Given, $\alpha_{dc} = 0.98$ and $I_B = 120\ \mu A = 0.12\ mA$

$$I_C = \frac{0.98}{1 - 0.98}(0.12)\ mA$$

or $I_C = 5.88\ mA$

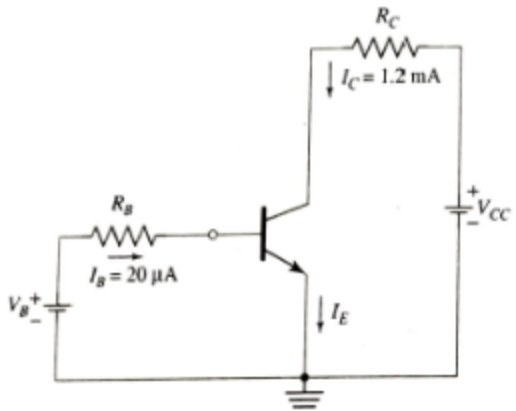
$$I_E = I_C + I_B$$
$$= (5.88 + 0.12)\ mA$$
$$= 6\ mA$$

$$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} = \frac{0.98}{1 - 0.98} = 49$$

$$\therefore \beta_{dc} = 49$$

Problems

2. For the circuit shown below, find ;
(a) The values of α and β of the transistor **(b) Value of I_B for a desired I_C of 5mA**



$$\beta_{dc} = \frac{I_C}{I_B} = \frac{1.2\text{ mA}}{20\ \mu\text{A}} = \frac{1.2\text{ mA}}{0.02\text{ mA}}$$

or $\beta_{dc} = 60$

$$\alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}} = \frac{60}{61}$$

or $\alpha_{dc} = 0.984$

$$I_C = 5\text{ mA}$$

$$I_B = \frac{I_C}{\beta_{dc}} = \frac{5\text{ mA}}{60} = 83.33\ \mu\text{A}$$

Problems

3. For a certain transistor circuit, I_C=12.42mA and I_B=200μA

a) **Find I_E**

b) **Find α and β of the transistor**

c) **Find I_c when I_B=150μA**

(a)

$$I_E = I_C + I_B = (12.42 + 0.2)\,\text{mA}$$

$$\therefore\ I_E = 12.62\,\text{mA}$$

(b)

$$\alpha_{dc} = \frac{I_C}{I_E} = \frac{12.42}{12.62} \qquad \beta_{dc} = \frac{I_C}{I_B} = \frac{12.42}{0.2} = 62.1$$

or $\alpha_{dc} = 0.9842$

(c) When $I_B = 150\,\mu\text{A} = 0.15\,\text{mA}$,

$$I_C = \beta_{dc} I_B = (62.1)(0.15)\,\text{mA}$$

$$\therefore\ I_C = 9.315\,\text{mA}$$

Problems

4. Find I_C and I_E For a transistor with , α =0.99 and I_B=20μA

Problems

5. A certain transistor circuit has I_C=16mA and I_E=16.14mA. Find the new values of I_C and I_E, for the same base current if the Transistor is replaced with a transistor of β=25

Given, $I_C = 16\,\text{mA}$ and $I_E = 16.04\,\text{mA}$

$$I_B = I_E - I_C = (16.04 - 16)\,\text{mA} = 0.04\,\text{mA}$$

$$\therefore\ I_B = 40\,\mu\text{A}$$

For the existing transistor

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{16}{0.04} = 400$$

When a transistor with $\beta_{dc} = 25$ is used,

$$I_C = \beta_{dc} I_B = 25 \times 0.04\,\text{mA}$$

$$\therefore\ I_C = 1\,\text{mA}$$

and $$I_E = I_C + I_B = (1 + 0.04)\,\text{mA}$$

$$\therefore\ I_E = 1.04\,\text{mA}$$

Current amplification in Transistors

By definition

$$\beta_{dc} = \frac{I_C}{I_B}$$

For changes in ΔI_B and ΔI_c in the collector and base currents

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B} \qquad \beta_{ac} = \frac{I_c}{I_b}$$

$$h_{fe} = \frac{I_c}{I_b}$$

if $\Delta I_B = \pm 10\,\mu A$ in a transistor with $\beta_{ac} = 200$, the change in collector current is

$$\Delta I_C = (\pm 10\,\mu A)200$$
$$= \pm 2\,mA$$

I_c and I_b are the *ac* collector current and *ac* base current.

Thus for a small variation in base current results in large variations in collector currents

Voltage amplification in Transistors

Consider the transistor circuit shown. For a given I_B, we can obtain I_C as

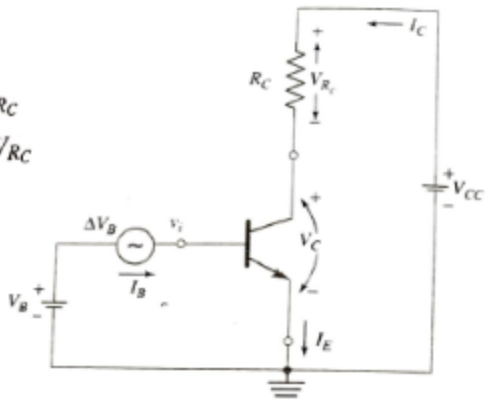
$$I_C = \beta_{dc} I_B$$

By applying KCL at collector loop

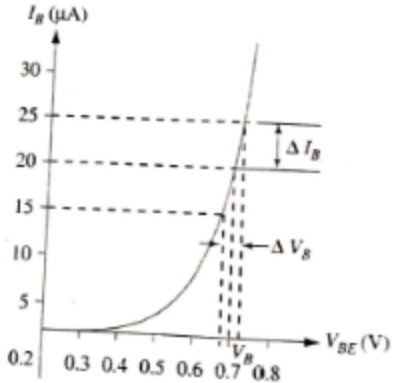
$$V_{CC} = V_C + V_{R_C}$$
$$\therefore V_C = V_{CC} - V_{R_C}$$

where V_{R_C} = voltage across R_C
$= I_C R_C$

$$\therefore V_C = V_{CC} - I_C R_C$$



For a given change in input voltage ΔV_B, we can find the change in base current ΔI_B the transistor input characteristic as shown



$$\therefore \Delta I_C = \beta_{dc} \Delta I_B$$

$$V_C = V_{CC} - I_C R_C$$

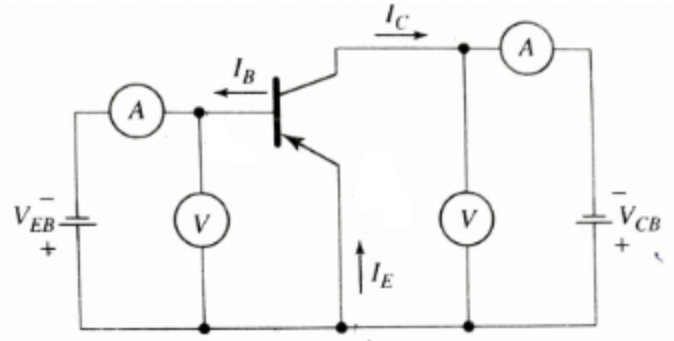
$$v_o = |\Delta V_C| = |\Delta I_C R_C|$$

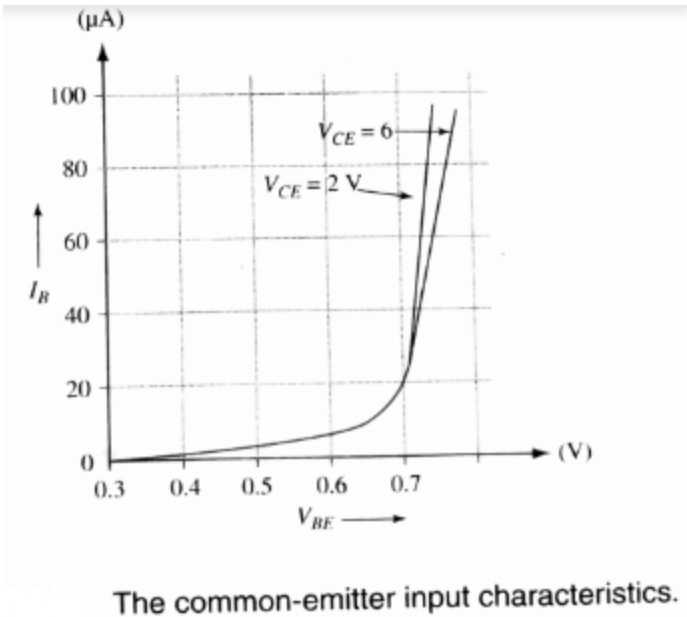
Voltage gain of transistor is given by

$$A_V = \frac{\Delta V_C}{\Delta V_B}$$

Common Emitter Configuration

Input Characteristics: Variation of I_B as a function of V_{BE} at constant V_{CE}





The common-emitter input characteristics.

npn or pnp type??

To which device V-I characteristics , does the input characteristics of transistor resemble?

Input characteristics

The CE Input Characteristics resembles the V-I characteristics of forward biased p-n junction diode

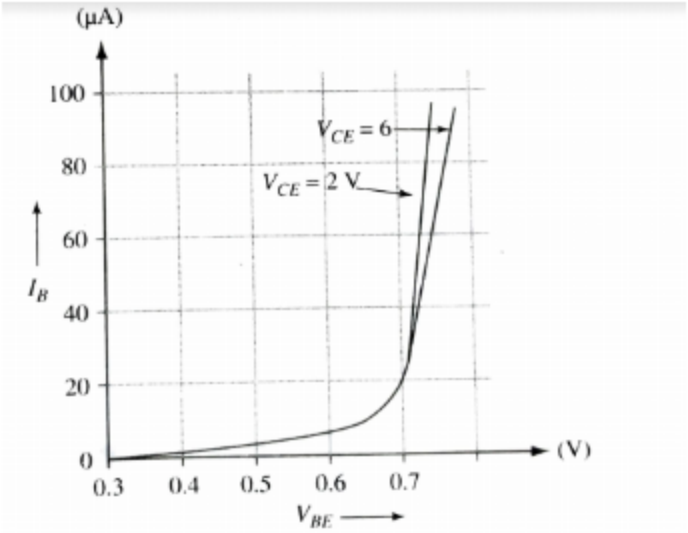
It is important to note the I_B is the small portion of total emitter current I_E that flows across the FB B-E junction

We find that at a constant V_{BE}, I_B decreases with increase in V_{CE}.

This is due to the fact that with increase in V_{CE} , the depletion region at the reverse biased collector-base junction widens, which reduces the base width.

Consequently, more charge carriers from the emitter flow across the C-B junction and fewer flow out of the base terminal

The reduction in base width due to increase in V_{CE} is called base width modulation or Early effect.



The common-emitter input characteristics.

Output Characteristics

Input Characteristics: Variation of I_C as a function of V_{CE} at constant I_B

IB is set to a convenient value, VCE is varied in suitable steps and at each step IC value is recorded.

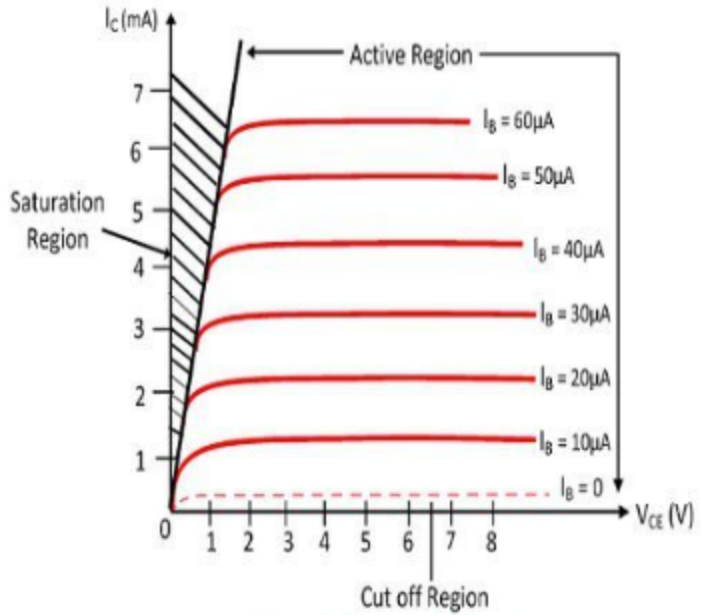
The same procedure is repeated for different settings of IB.

When the base current IB is 0 A, the transistor operates in cut-off region. In this region both the junctions are RB

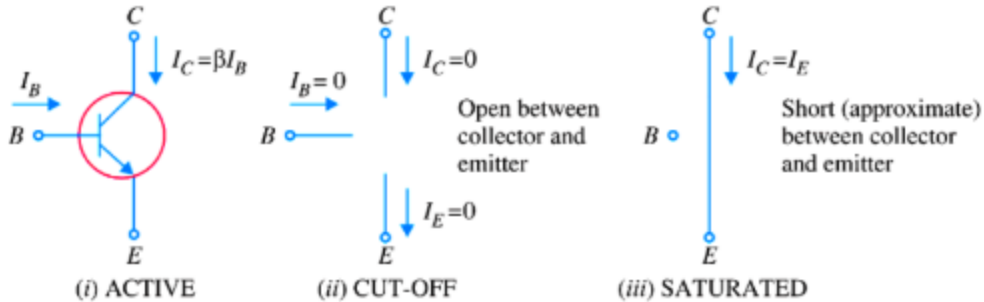
IB is increased by from 0 A to 20μA by increasing VBE.

When the output voltage is reduced to a small value (say 0.2 V), the CB junction is FB.

Since both junctions are FB, transistor operates in saturation region.



Regions of operation



In the **active state**, collector current is β times the base current.

If the transistor is **cut-off,** there is no base current, so there is no collector or emitter current. That is collector emitter pathway is open

In **saturation**, the collector and emitter are, in effect, shorted together. That is the transistor behaves as though a switch has been closed between the collector and emitter

Transistor biasing

The transistor needs to be operated in an appropriate region of its characteristics depending upon the application of the circuit.

When the transistor is used as amplifier it should operate in active region.

The required current and voltages in the transistor circuit are established by using resistive networks with DC power supply.

The process is called biasing and the DC power supply along with resistors used for purpose of biasing is called bias circuit.

When it is operated in cut-off and saturation it can be used as a switch.

The DC load line & operating point

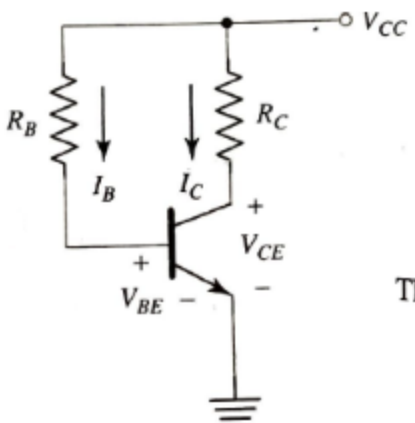
The DC load line for a transistor circuit is a graphical representation of output equation drawn on the transistor output characteristics.

For a C-E circuit, the load line is a graph of collector current (I_C) versus collector-emitter voltage (V_{CE}), for a given value of collector resistance (R_C) and a given supply voltage (V_{CC}).

The load line shows all corresponding levels of I_C and V_{CE} that can exist in a particular circuit.

Procedure for drawing DC load line

Consider an npn transistor in CE configuration biased in the active region.



Apply KVL at input loop (B-E circuit)

$$V_{CC} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

The collector current is given by,

$$I_C = h_{FE} I_B$$

Apply KVL at output loop (B-C circuit)

$$V_{CC} = I_C R_C + V_{CE}$$

$$I_C = \frac{V_{cc} - V_{CE}}{R_C}$$

Comparing the eqn with straight line eqn

$$y = mx + c$$

$$I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C}$$

m=slope= -1/R_C and c= V_{CC}/R_C

To determine 2 points on the graph we assume $V_{CE} = V_{CC}$ & $V_{CE} = 0$

a) When $V_{CE} = V_{CC}$; $I_{C=0}$ .....(Point A)

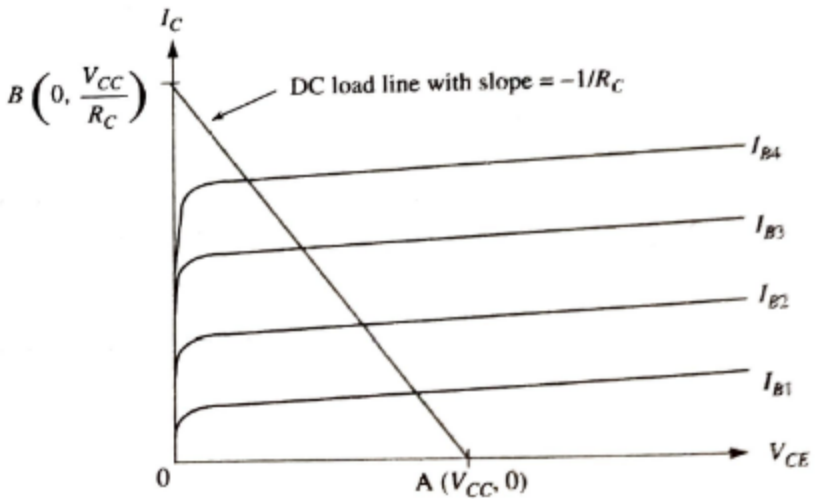
b) When $V_{CE} = 0$; $I_C = \frac{V_{CC}}{R_C}$ ..... (Point B)

Procedure for drawing DC load line

To determine 2 points on the graph we assume $V_{CE} = V_{CC}$ & $V_{CE} = 0$

a) When $V_{CE} = V_{CC}$; $I_{C=0}$ .....(Point A)

b) When $V_{CE} = 0$; $I_C = \frac{V_{CC}}{R_C}$ ..... (Point B)



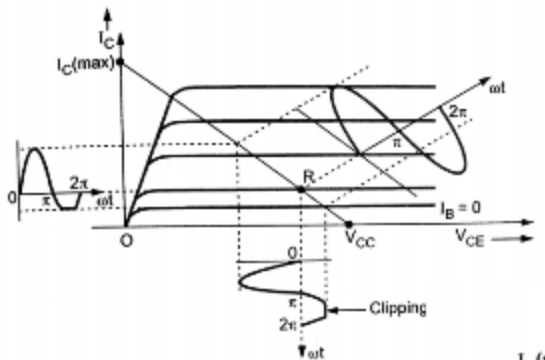
Selection of operating point

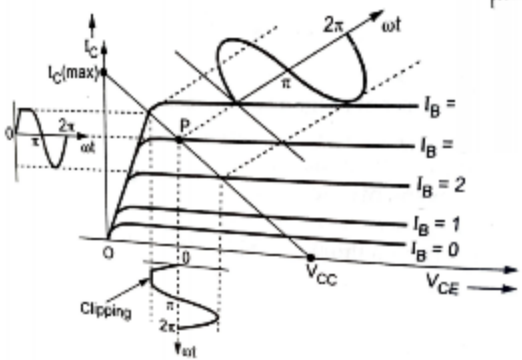
The operating point(Q point) can be selected at 3 different positions on the dc load line

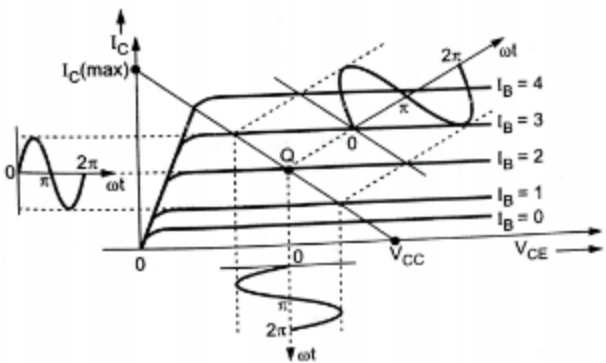
1)Near cut-off

2)Near active

3)Near Saturation

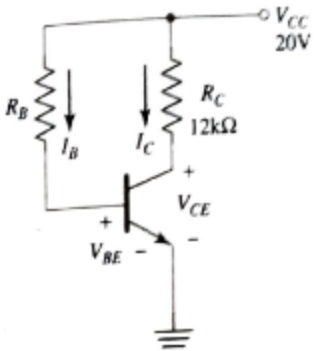


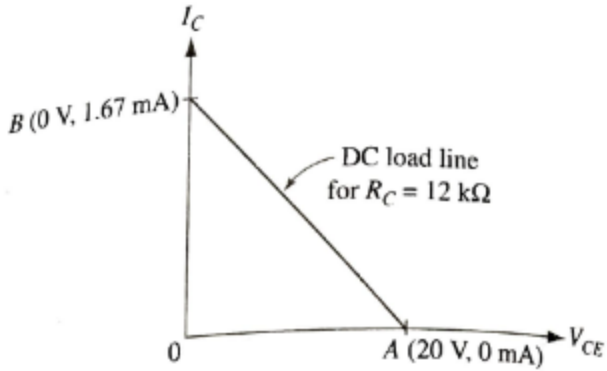




Problem

For the circuit shown below draw the DC load line





Biasing circuits

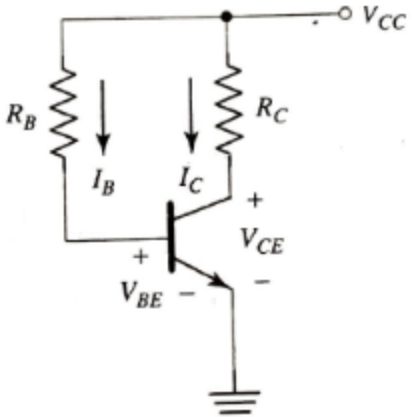
Following are the 3 biasing circuits which are commonly used

a) **Base bias Circuit**
b) **Collector bias Circuit**
c) **Voltage divider circuit**

The biasing circuit must ensure constant levels of the Q point current I_C and voltage V_{CE} regardless the transistor replacement and circuit temperature variation.

Voltage divider bias circuit provides excellent stability of I_C and V_{CE} levels and hence it is commonly used to bias transistors in amplifier circuits.

Base bias circuit



Applying Kirchhoff's Voltage Law to the base-emitter circuit we have

$$V_{CC} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

V_{BE} is taken as 0.7 V for a Silicon transistor and as 0.3 V for a Germanium transistor. $V_{CC} >> V_{BE}$.

Therefore $V_{CC} - V_{BE} \simeq V_{CC}$. Now, from equation we have

$$I_B \simeq \frac{V_{CC}}{R_B}$$

Since V_{CC} and R_B are constant quantities, I_B is a constant quantity.

The collector current is calculated as

$$I_C = h_{FE} I_B$$

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C$$

Base bias circuit-Problems

1. For a base bias circuit, V_{CC}=18V, R_C=2.2KΩ, R_B=470KΩ, V_{BE}=0.7 V. Find the levels of I_C and V_{CE} when $h_{FE(min)}$ =50 and $h_{FE(max)}$ =200. Draw the DC load line and indicate the Q points

Case 1: When $h_{FE} = h_{FE(\min)} = 50$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{18\,\text{V} - 0.7\,\text{V}}{470\,\text{k}\Omega} = 36.81\,\mu\text{A}$$

$$I_C = h_{FE(\min)} I_B = 50 \times 36.81\,\mu\text{A} = 1.84\,\text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 18\,\text{V} - (1.84\,\text{mA} \times 2.2\,\text{k}\Omega) = 13.95\,\text{V}$$

$$Q_1(V_{CE}, I_C) = Q_1(13.95\,\text{V}, 1.84\,\text{mA})$$

Case 2: When $h_{FE} = h_{FE(\max)} = 200$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{18\,\text{V} - 0.7\,\text{V}}{470\,\text{k}\Omega} = 36.81\,\mu\text{A}$$

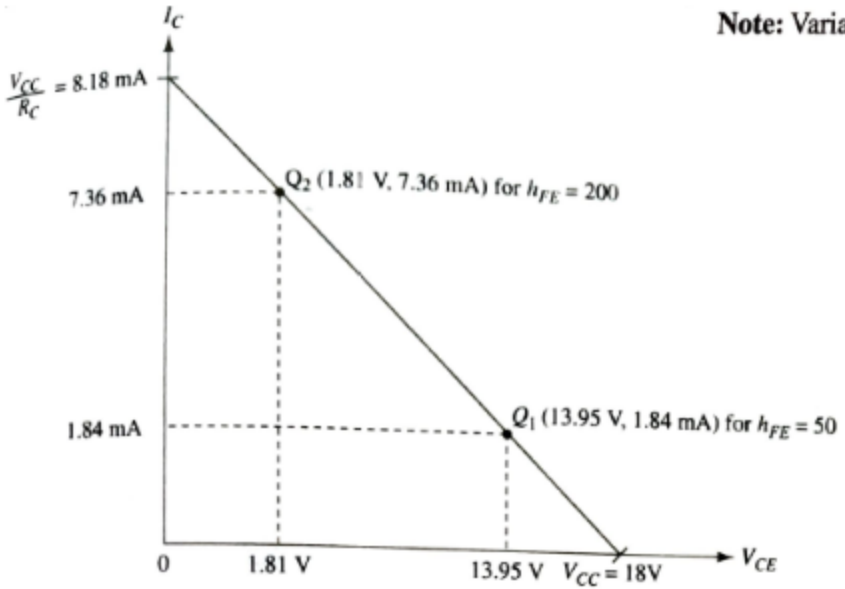
Note that I_B is unaffected by h_{FE}

$$I_C = h_{FE(\max)} I_B = 200 \times 36.81\,\mu\text{A} = 7.36\,\text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 18\,\text{V} - (7.36\,\text{mA} \times 2.2\,\text{k}\Omega) = 1.81\,\text{V}$$

$$Q_2(V_{CE}, I_C) = Q_2(1.81\,\text{V}, 7.36\,\text{mA})$$

Base bias circuit-Problems



Note: Variation in h_{FE} results in drastic drift in the Q point.

Base bias circuit-Problems

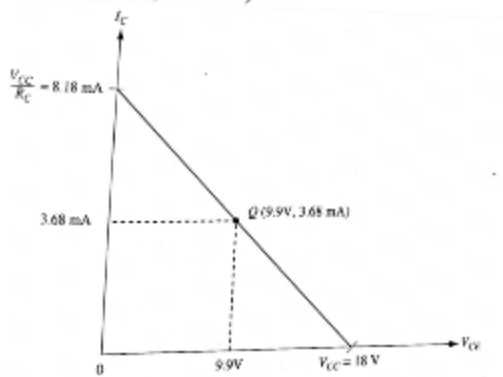
For the base bias circuit shown in Fig. 3.41, find I_B, I_C and V_{CE} if $R_C = 2.2\,k\Omega$, $R_B = 470\,k\Omega$, $V_{CC} = 18\,V$, $h_{FE} = 100$, $V_{BE} = 0.7\,V$. Draw the DC load line and indicate the Q point.

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$
$$= \frac{18\,V - 0.7\,V}{470\,k\Omega}$$
$$= 36.81\,\mu A$$

$$I_C = h_{FE}\, I_B$$
$$= 100 \times 36.81\,\mu A$$
$$= 3.68\,mA$$

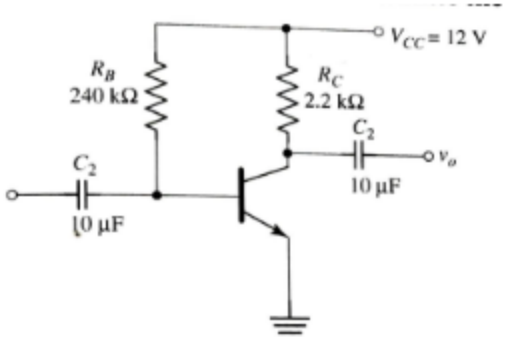
$$V_{CE} = V_{CC} - I_C R_C$$
$$= 18\,V - (3.68\,mA \times (2.2\,k\Omega)$$
$$= 9.9\,V$$

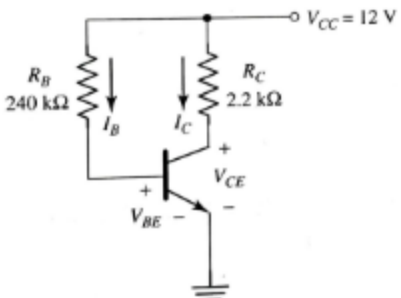
Co-ordinates of Q point are $Q(V_{CE}, I_C) = Q(9.9\,V, 3.68\,mA)$



Base bias circuit-Problems

3. In a circuit shown below a silicon transistor with β=50 is used. Find I_C and V_{CE}. Draw the DC load line and indicate the Q point.

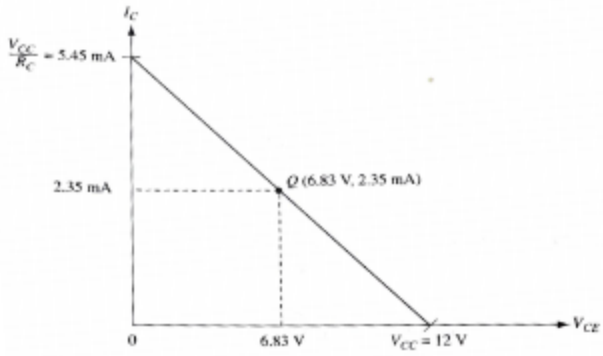




$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$
$$= \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega}$$
$$= 0.047\text{ mA or } 47\,\mu\text{A}$$

$$I_C = h_{FE} I_B$$
$$\beta = h_{FE} = 50$$
$$I_C = (50)(0.047\text{ mA})$$
$$= 2.35\text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C$$
$$= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega)$$
$$= 6.83\text{ V}$$
$$Q(V_{CE},\ I_C) = Q(6.83\text{ V}, 2.35\text{ mA})$$



Base-bias Circuit design

The base bias circuit is shown in Fig. 3.42

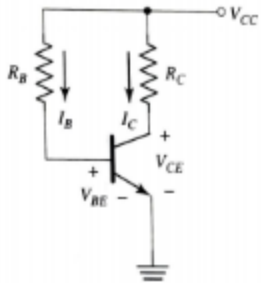


Fig. 3.42 Base-bias circuit.

The values of V_{CC}, V_{CE}, V_{BE}, I_C and h_{FE} will be given. The design steps are as follows:

(a) First calculate R_C using the relation

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} \tag{3.35}$$

(b) Then calculate I_B using the relation

$$I_B = \frac{I_C}{h_{FE}}$$

(c) Finally calculate R_B using the relation

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

Base-bias Circuit design

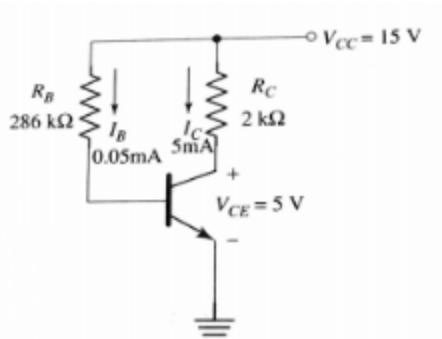
Design a base bias circuit to have $V_{CE} = 5\,V$ and $I_C = 5A$. The supply voltage is 15 V and the transistor has $h_{FE} = 100$.

$$V_{CE} = 5\,V, \quad I_C = 5\,mA$$
$$V_{CC} = 15\,V, \quad h_{FE} = 100$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{15\,V - 5\,V}{5\,mA} = 2\,k\Omega$$

$$I_B = \frac{I_C}{h_{FE}} = \frac{5\,mA}{100} = 0.05\,mA$$

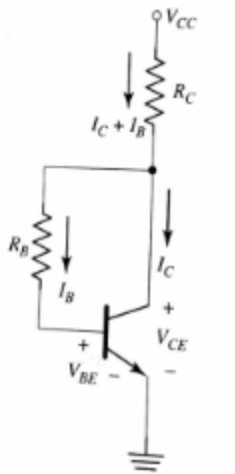
$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$



Assume a Silicon transistor for which $V_{BE} = 0.7\,V$

$$\therefore R_B = \frac{15\,V - 0.7\,V}{0.05\,mA} = 286\,k\Omega$$

Collector to Base bias



Applying KVL to the path consisting of the drops V_{CE}, I_BR_B, and V_{BE} we have,

$$V_{CE} - I_BR_B - V_{BE} = 0$$
$$V_{CE} = I_BR_B + V_{BE}$$
$$I_B = \frac{V_{CE} - V_{BE}}{R_B}$$

Applying KVL to the C-E loop,

$$V_{CC} - R_C(I_B + I_C) - V_{CE} = 0$$
$$V_{CE} = V_{CC} - R_C(I_B + I_C)$$

Substituting equation for V_{CE} in above equation

$$I_BR_B + V_{BE} = V_{CC} - R_C(I_B + I_C)$$
$$I_BR_B + I_BR_C + I_CR_C = V_{CC} - V_{BE}$$

Using $I_C = h_{FE}I_B$,

$$I_BR_B + I_BR_C + h_{FE}I_BR_C = V_{CC} - V_{BE}$$

$$I_B\left[R_B + (1 + h_{FE}R_C)\right] = V_{CC} - V_{BE}$$
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + h_{FE})R_C}$$

(a) I_CR_C increases
(b) V_{CE} decreases
(c) I_B decreases
(d) $I_C = h_{FE}I_B$ decreases

Collector to Base bias-Problems

5.A collector-to-bias circuit shown has , V_{CC}=15V, R_C=1.8KΩ, R_B=39KΩ, V_{BE}=0.7 V. Find the levels of I_C and V_{CE} when h_{FE}=50 . Draw the DC load line and indicate the Q points

$$V_{CC} = 15\,\text{V}, \quad V_{BE} = 0.7\,\text{V}, \quad h_{FE} = 50$$
$$R_C = 1.8\,\text{k}\Omega, \quad h_{FE} = 50, \quad R_B = 39\,\text{k}\Omega$$

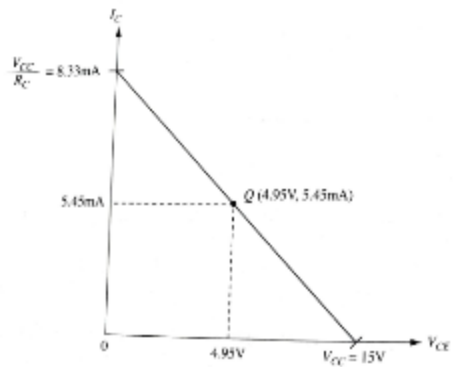
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + h_{FE})R_C} = \frac{15\,\text{V} - 0.7\,\text{V}}{39\,\text{k}\Omega + (1 + 50)(1.8\,\text{k}\Omega)}$$
$$= 0.109\,\text{mA}$$

$$I_C = h_{FE} I_B$$
$$= (50)(0.109\,\text{mA})$$
$$= 5.45\,\text{mA}$$

$$V_{CE} = I_B R_B + V_{BE}$$
$$= (0.109\,\text{mA})(39\,\text{k}\Omega) + 0.7\,\text{V}$$
$$= 4.95\,\text{V}$$

or $$V_{CE} = V_{CC} - R_C(I_C + I_B)$$
$$= 15 - 1.8\,\text{k}\Omega(5.45 + 0.109)\,\text{mA}$$
$$= 4.9938\,\text{V}$$

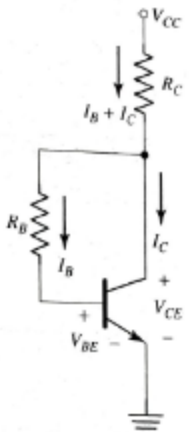
$$Q(V_{CE}, I_C) = Q(4.95\,\text{V}, 5.45\,\text{mA})$$



Collector to Base bias-Problems

A collector-to-base bias circuit has $V_{CC} = 15\,V$, $R_C = 5.6\,k\Omega$, $R_B = 82\,k\Omega$ and $V_{CE} = 5\,V$. Determine the transistor h_{FE} value. Calculate new V_{CE} level when a transistor with $h_{FE} = 50$ is substituted.

Collector to Base bias-Design



The values of V_{CC}, V_{CE}, V_{BE},I_C and h_{FE} will be given. The design steps are as follows.

(a) First calculate I_B using the relation

$$I_B = \frac{I_C}{h_{FE}} \tag{3.42}$$

(b) Then calculate R_C using the relation

$$R_C = \frac{V_{CC} - V_{CE}}{I_C + I_B}$$

(c) Finally calculate R_B using the relation

$$R_B = \frac{V_{CE} - V_{BE}}{I_B}$$

Collector to Base bias-Problems

Design a collector-to-base bias circuit to have $V_{CE} = 5\,V$ and $I_C = 5\,mA$ when the supply voltage is 15 V and the transistor h_{FE} is 100, $V_{BE} = 0.7\,V$.

$V_{CE} = 5\,V, \quad I_C = 5\,mA, \quad V_{BE} = 0.7\,V$

$V_{CC} = 15\,V, \quad h_{FE} = 100$

$$I_B = \frac{I_C}{h_{FE}} = \frac{5\,mA}{100}$$

$$= 0.05\,mA$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C + I_B}$$

$$= \frac{15\,V - 5\,V}{5\,mA + 0.05\,mA}$$

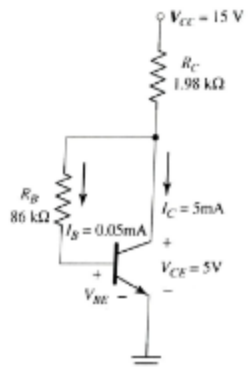
$$= 1.98\,k\Omega$$

$$R_B = \frac{V_{CE} - V_{BE}}{I_B}$$

$$= \frac{5\,V - 0.7\,V}{0.05\,mA}$$

$$= 86\,k\Omega$$

The circuit with designed component values is shown below.



Collector to Base bias-Problems

- A collector-to-base bias circuit has $V_{CC} = 30\,V$, $R_C = 8.2\,k\Omega$ and the transistor $h_{FE} = 100$. Calculate the required base resistance value to give $V_{CE} = 7\,V$. Take $V_{BE} = 0.7\,V$.

Voltage-divider- Approximate analysis

1. **Voltage divider bias also known as emitter current –bias gives the most stable operating point when compared to base bias & collector-to-bias circuits**

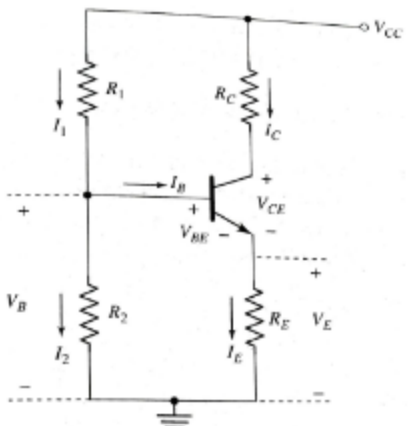
2. **In this circuit the levels of I_C and V_{CE} are almost independent of h_{FE} value.**

3. **In approximate analysis the base current is assumed to be much smaller than the voltage divider I_2.**

Resistors R_1 and R_2 constitute a voltage divider that divides the supply voltage to produce the base bias voltage V_B.

$$I_1 = I_2 + I_B \tag{3.45}$$

Voltage divider bias circuits are normally designed to have the voltage divider current I_2 very much larger than the transistor base current I_B. i.e., $I_2 >> I_B$. From equation 3.45 we get $I_2 \simeq I_1$. Note that same current flows through R_1 and R_2.



Voltage-divider- Approximate analysis

Voltage across R_2 is, $V_B = I_2 R_2$

$$V_B = \frac{V_{CC} R_2}{R_1 + R_2}$$

Note that V_B is a constant quantity

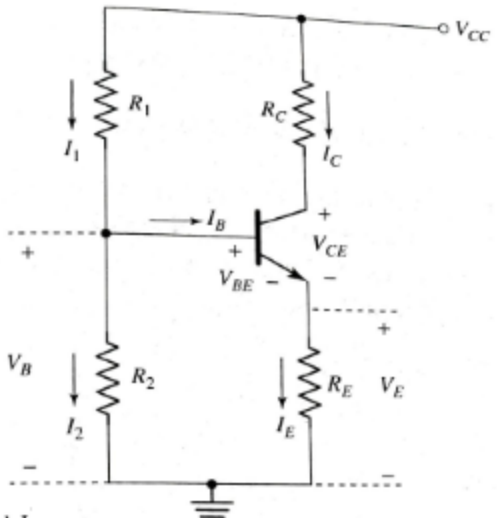
$$V_B = V_{BE} + V_E$$

$$V_E = V_B - V_{BE}$$

But $V_E = I_E R_E$. Using this relation in equation

$$I_E R_E = V_B - V_{BE}$$

$$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{V_E}{R_E}$$



$I_E = I_B + I_C \simeq I_C$, since base current is small. Since V_B is a constant quantity, I_C and I_E are held at constant level.

Voltage-divider- Approximate analysis

Applying Kirchhoff's Voltage Law to the collector emitter circuit we have

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

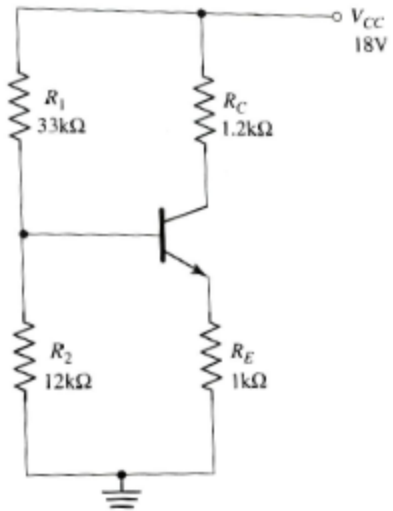
Since $I_E \simeq I_C$, we can write

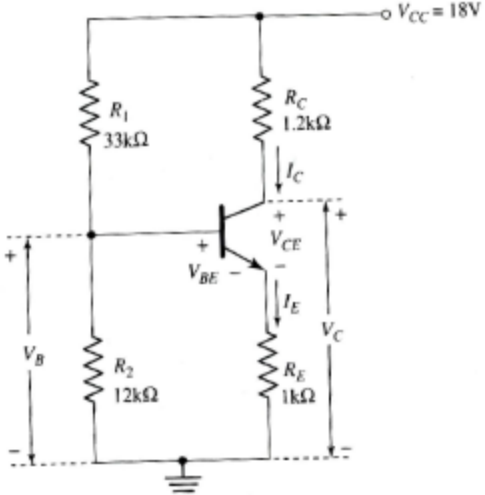
$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Clearly, with I_C and I_E constant, the transistor collector-emitter voltage remains at a constant level. Note that transistor β value is not involved in any of the above equations!!!!!!!

Voltage-divider- Approximate analysis

Analyse the voltage divider bias circuit shown below to determine emitter voltage V_E, collector voltage V_C, base voltage V_B, collector current I_C and collector to emitter voltage V_{CE}. Assume Silicon transistor with $V_{BE} = 0.7\,V$. Draw the DC load line and mark the Q point.





$$V_B = \frac{V_{CC}R_2}{R_1 + R_2} = \frac{18\,V \times 12\,k\Omega}{33\,k\Omega + 12\,k\Omega} = 4.8\,V$$

$$V_E = V_B - V_{BE}$$
$$= 4.8\,V - 0.7\,V$$
$$= 4.1\,V$$

$$I_E = \frac{V_E}{R_E}$$
$$= \frac{4.1V}{1k\Omega}$$
$$= 4.1\,mA$$

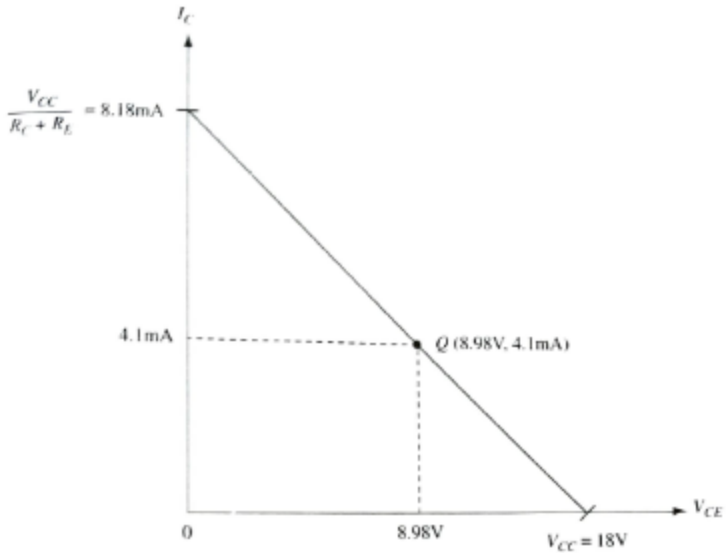
$$I_C \simeq I_E = 4.1\,mA$$

Voltage-divider- Approximate analysis

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$= 18\,\text{V} - (4.1\,\text{mA})(1.2\text{k}\Omega + 1\text{k}\Omega)$$
$$= 8.98\,\text{V}$$

$$V_C = V_{CE} + I_E R_E$$
$$= 8.98\,\text{V} + (4.1\,\text{mA})(1\,\text{k}\Omega)$$
$$= 13.08\,\text{V}$$

$$Q(V_{CE},\ I_C) = Q(8.98\,\text{V}, 4.1\,\text{mA})$$



Voltage-divider- Approximate analysis

A voltage divider bias circuit has $V_{CC} = 15\,V$, $R_C = 2.7\,k\Omega$, $R_E = 2.2\,k\Omega$ $R_1 = 22\,k\Omega$, $R_2 = 12\,k\Omega$. Calculate V_E, V_C, I_C and V_{CE}. Draw the DC load line and mark the Q point. Take $V_{BE} = 0.7\,V$.

Voltage-divider- Approximate analysis-Design

(a) $I_2 = \dfrac{I_C}{10}$ This gives reasonably large value for R_1 and R_2 while still keeping $I_2 >> I_B$. Large values of R_1 and R_2 are desirable to achieve high input impedance.

(b) V_E should be selected much larger than V_{BE}, i.e $V_E \gg V_{BE}$. The level of V_E in the range 3 V–5 V is reasonable.

(c) R_E is calculated using

$$R_E = \frac{V_E}{I_C}$$

(d) R_2 is calculated using

$$R_2 = \frac{V_B}{I_2}$$

where $V_B = V_{BE} + V_E$

(e) R_1 is calculated from the relation

$$V_{CC} = I_1 R_1 + I_2 R_2 = I_2 R_1 + V_B \quad (\because I_1 \simeq I_2)$$

$$\Longrightarrow R_1 = \frac{V_{CC} - V_B}{I_C}$$

(f) R_C is obtained from the relation

$$V_{CC} = I_C R_C + V_{CE} + V_E$$

$$\Longrightarrow R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C}$$

Voltage-divider- Approximate analysis-Design

Design the voltage divider bias circuit to have $V_{CE} = V_E = 5\,V$ and $I_C = 5\,mA$, when the supply voltage is 15 V. Assume the transistor h_{FE} as 100 and $V_{BE} = 0.7\,V$.

$$R_E = \frac{V_E}{I_E} \simeq \frac{V_E}{I_C}$$

$$= \frac{5\,V}{5\,mA}$$

$$= 1\,k\Omega$$

$$I_2 = \frac{I_C}{10} = \frac{5\,mA}{10} = 0.5\,mA$$

$$V_B = V_{BE} + V_E$$

$$= 0.7\,V + 5\,V$$

$$= 5.7\,V$$

$$R_2 = \frac{V_B}{I_2}$$

$$= \frac{5.7\,V}{0.5\,mA}$$

$$= 11.4\,k\Omega$$

$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C}$$

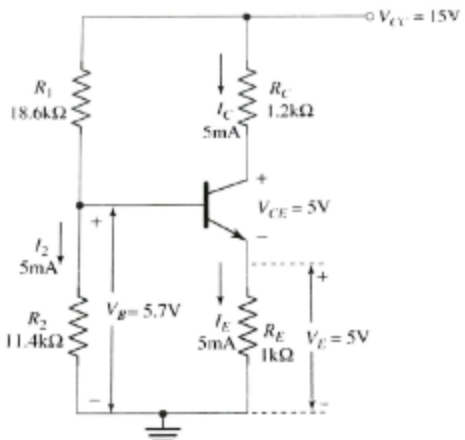
$$= \frac{15\,V - 5\,V - 5\,V}{5\,mA}$$

$$= 1\,k\Omega$$

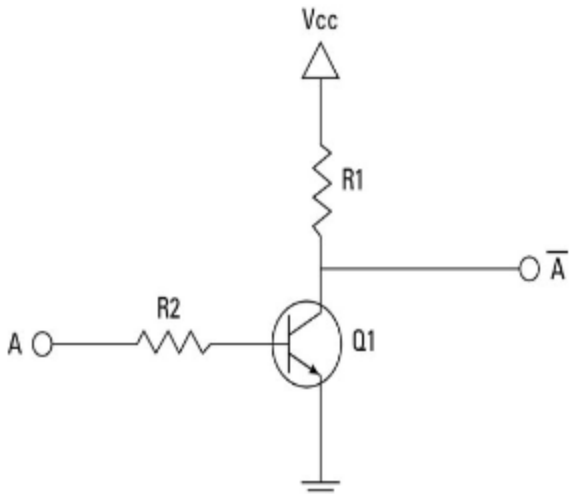
$$R_1 = \frac{V_{CC} - V_B}{I_2}$$

$$= \frac{15\,V - 5.7\,V}{0.5\,mA}$$

$$= 18.6\,k\Omega$$

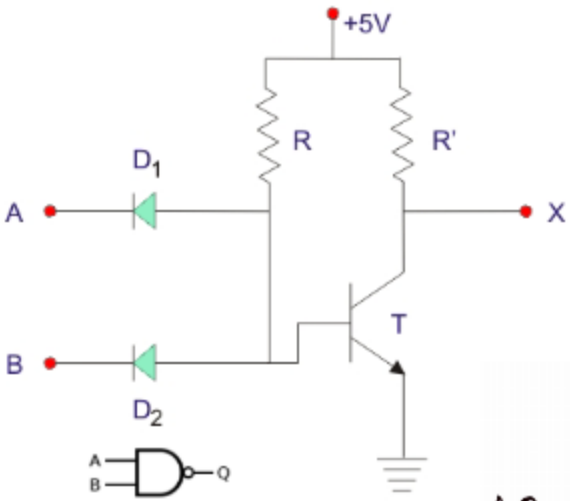


Transistor as a switch: NOT Gate



1. A NOT gate simply inverts its input. If the input is HIGH, the output is LOW, and if the input is LOW, the output is HIGH.
2. The input is connected through resistor R2 to the transistor's base.
3. When no voltage is present on the input, the transistor turns off. When the transistor is off, no current flows through the collector-emitter path. (Cut-off region)
4. Thus, current from the supply voltage (Vcc in the schematic) flows through resistor R1 to the output. In this way, the circuit's output is HIGH when its input is LOW.
5. When the input voltage is more than cut-in voltage, the transistor turns on (Saturation region). The output will be LOW when the input is high.

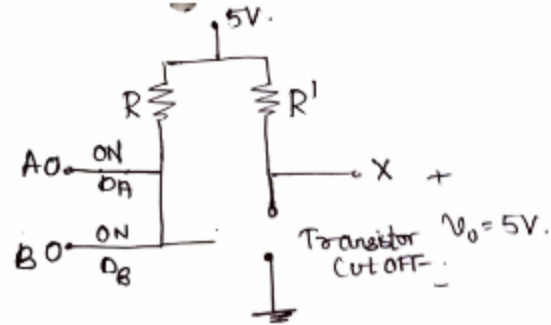
DTL NAND Gate

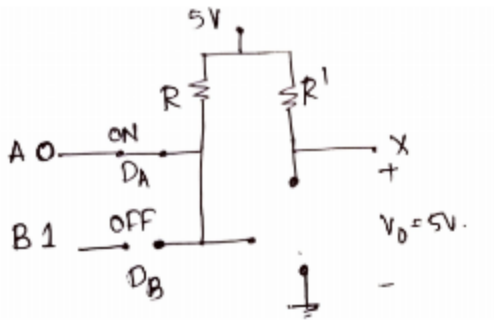


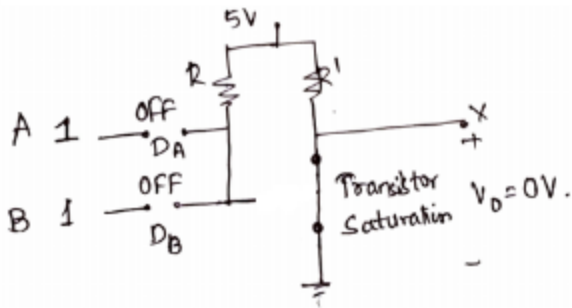
Q = A NAND B

Truth Table

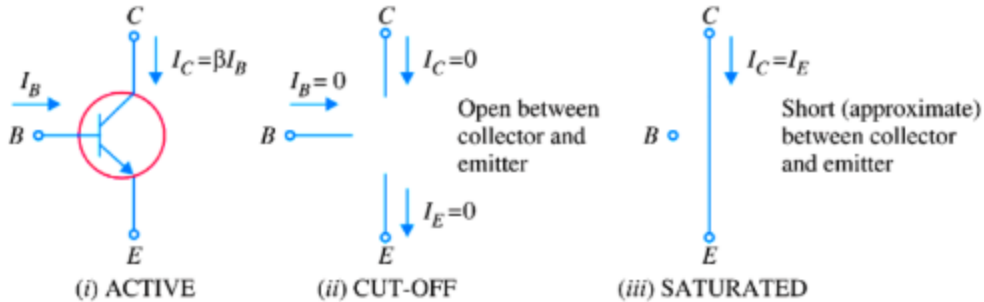
Input A	Input B	Output Q
0	0	1
0	1	1
1	0	1
1	1	0







Regions of operation



In the **active state**, collector current is β times the base current.

If the transistor is **cut-off,** there is no base current, so there is no collector or emitter current. That is collector emitter pathway is open

In **saturation**, the collector and emitter are, in effect, shorted together. That is the transistor behaves as though a switch has been closed between the collector and emitter

Topic Learning Outcomes

At the end of the topic, students should be able to:

1. Discuss on the transistor CE configuration.
2. Explain significance of DC load line and operating point.
3. Realize the simple applications using transistor.

CO-2: Describe the characteristics of semiconductor devices and their applications in rectifiers, switches, regulators and gates.

THANK YOU