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KLE Technological University

Creating Value

Leveraging Knowledge

Unit –I

Chapter 3

Transistor

Contents

Session No.	Contents covered
01	BJT, transistor voltages and currents, Signal amplifier (Fixed bias, Collector base bias, Voltage divider bias, CE configuration)
02	DC load line (Q-point), Voltage, current and power gains
03	Transistor as a switch: NOT Gate, Basic (DTL) NAND gate.

Topic Learning Outcomes

At the end of the topic, students should be able to:

- 1.Discuss on the transistor CE configuration.
- 2.Explain significance of DC load line and operating point.
- 3.Realize the simple applications using transistor.

CO-2: Describe the characteristics of semiconductor devices and their applications in rectifiers, switches, regulators and gates.

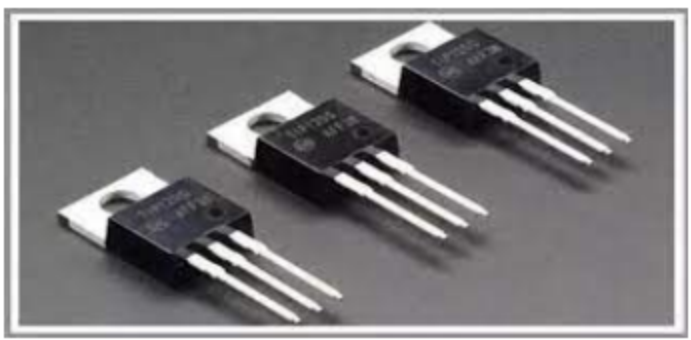
Key concepts

1. Transistor construction and operation
2. Transistor voltages and currents
3. Common emitter input and output characteristics
4. DC Load line & Q Point
5. Transistor biasing
6. Base bias circuit
7. Collector base circuit
8. Voltage divider circuit
9. Transistor as switch: NOT gate and DTL NAND gate

Transistor Definition

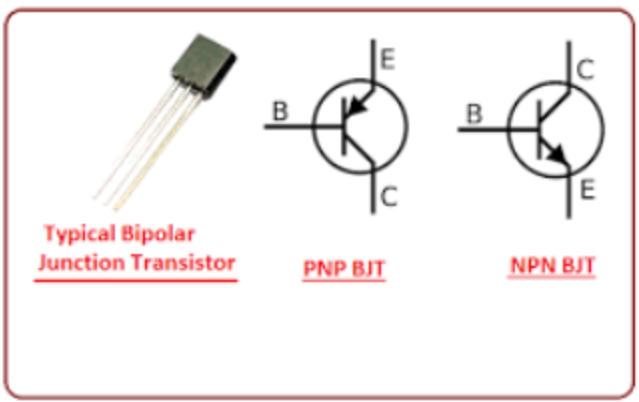
- Transistor is an electronic device made of three layers of semiconductor material that can act as insulator and a conductor.

- The three layered transistor is also known as the bipolar junction transistor.



Bipolar Junction Transistors(BJT's)

- It can be used as amplifier and logic switches.
- BJT consists of three terminals:
  - Collector: C
  - Base: B
  - Emitter: E
- Two types of BJT : npn and pnp



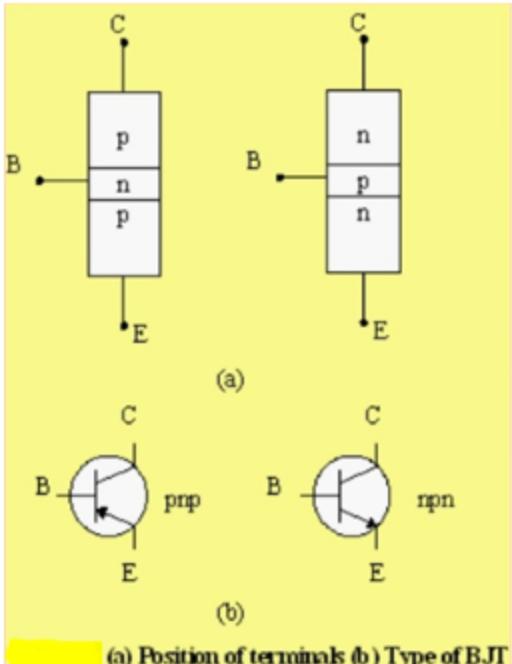
Transistor Construction

- 3 layer semiconductor device consists of :
  - 2 n- and 1 p- type layers of material ->npn transisitor
  - 2 p- and 1 n- type layers of material ->pnp transisitor
- A single pn junction has two different types of bias:
  - Forward bias
  - Reverse bias
- Thus, a two-pn-junction device has four types of bias.

Position of terminals and symbol of BJT

- Base is located at the middle and more thin from the level of collector and emitter.

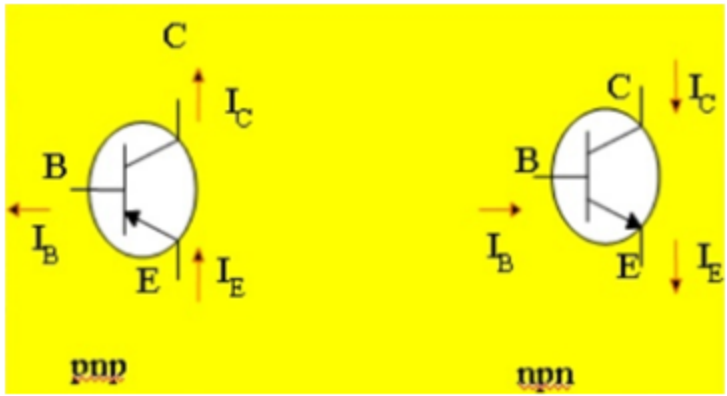
- The collector and emitter terminals are made of the same type of semiconductor material, while the base of the other type material.



(a) Position of terminals (b) Type of BJT

Transistor currents

1. The arrow is always drawn on the emitter
2. The arrow always points toward the n-type.
3. The arrow indicates the direction of emitter current:



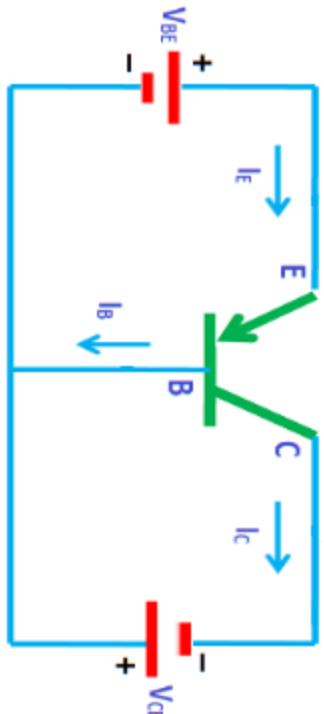
pnp: E->B

npn: B->E

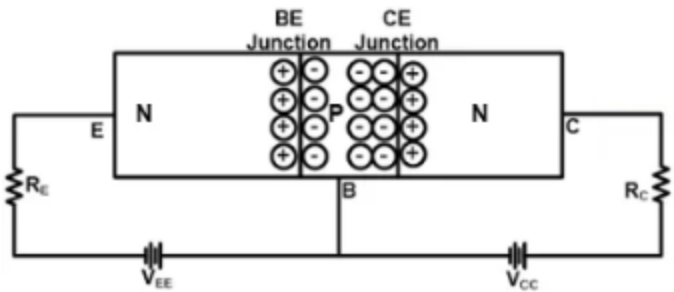
I_C = Collector current
I_B = Base current
I_E = Emitter current

Transistor Voltages

1. The supply voltage between the base and the emitter is denoted by V_{BE}.
2. The supply voltage between the collector and the base is denoted by V_{CB}.
3. The collector is biased to a higher negative level than the base to keep the collector-base junction reverse biased.



NPN Transistor operation



Working of NPN Transistor

1. The base-emitter junction is connected in the forward bias condition by supply voltage V_{EE}.
2. And the collector-base junction is connected in the reverse bias condition by supply voltage V_{CC}.
3. The depletion region of the emitter-base region is thin compared to the depletion region of the collector-base junction

NPN Transistor operation

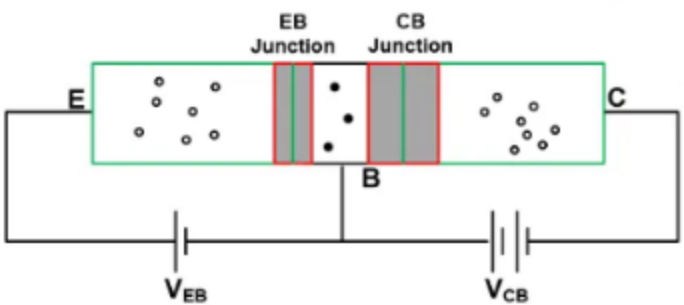
4. In N-type emitter, the majority charge carrier is electrons. the current will start flowing the emitter-base junction. This current is known as emitter current I_E.

5. These electrons move further to the base. The base is a P-type semiconductor. Therefore, it has holes. But the base region is very thin and lightly doped.

6. So, it has a few holes to recombine with the electrons. Hence, most of the electrons will pass the base region and few of them will recombine with the holes.

7. Because of the recombination, the current will flow through the circuit and this current is known as base current IB.

PNP Transistor operation



Working of PNP Transistor

1. The positive terminal of a voltage source (V_{EB}) is connected with Emitter (P-type) and the negative terminal is connected with the Base terminal (N-type). Therefore, the Emitter-Base junction is connected in forward bias.

2. And the positive terminal of a voltage source (VCB) is connected with the Base terminal (N-type) and the negative terminal is connected with the Collector terminal (P-type). Hence, the Collector-Base junction is connected in reverse bias.

PNP Transistor operation

4. The depletion region at Emitter-Base junction is narrow, because it is connected in forward bias. While the Collector-Base junction is in reverse bias and hence the depletion region at Collector-Base junction is wide.

5. The Emitter-base junction is in forward bias. Therefore, a very large number of holes from emitter cross the depletion region and enter the Base. Simultaneously, very few electrons enter in Emitter from the base and recombine with the holes.

6. Because of the movement of holes, the current will flow through the Emitter-Base junction. This current is known as Emitter current (I_E). The holes are majority charge carriers to flow the Emitter current.

7. The remaining holes which do not recombine with electrons in Base, that holes will further travel to the Collector. The Collector current (I_C) flows through the Collector-Base region due to holes.

α_{dc} and β_{dc} for a transistor

α_{dc} is emitter to collector current gain. It is the ratio of collector to emitter current i.e.,

$$\alpha_{dc} = \frac{I_C}{I_E}$$

Where Ic is dc collector current and IE is dc emitter current.

β_{dc} is base to collector current gain. It is the ratio of collector to base current i.e.,

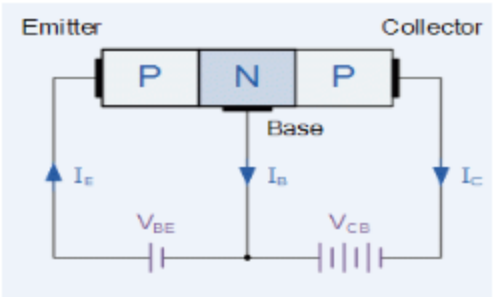
$$\beta_{dc} = \frac{I_C}{I_B}$$

Where IB is dc Base current.

β_{dc} is commonly known as h_{FE} based on h-parameter analysis of transistor.

$$h_{FE} = \frac{I_C}{I_B}$$

Equation for collector current



From figure $I_E = I_C + I_B$ 1

By definition $\alpha_{dc} = \frac{I_C}{I_E}$ 2

or $I_C = \alpha_{dc} I_E$ 3

From equations 1 & 2 $I_C = \alpha_{dc}(I_C + I_B)$

Or $I_C = \alpha_{dc} I_C + \alpha_{dc} I_B$

$$Ic = \frac{\alpha_{dc}}{1 - \alpha_{dc}} I_B$$

Relationship between αdc and βdc

$$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}}$$

βdc in terms of αdc

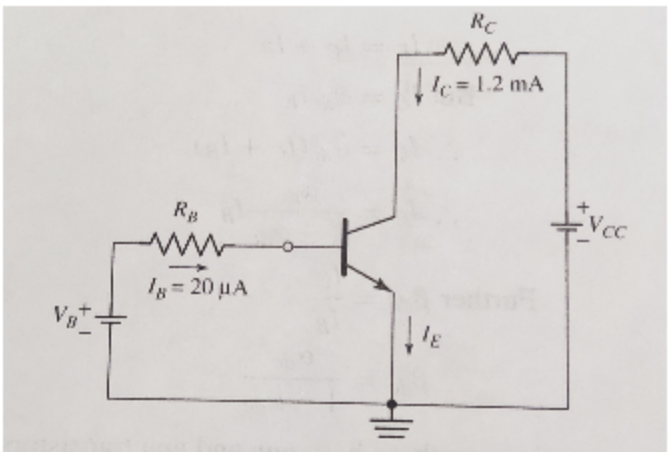
$$\alpha_{dc} = \frac{\beta_{dc}}{1 + \beta_{dc}}$$

Problem 1

For the circuit shown below find:

a) Values of α_{dc} and β_{dc} of the transistor

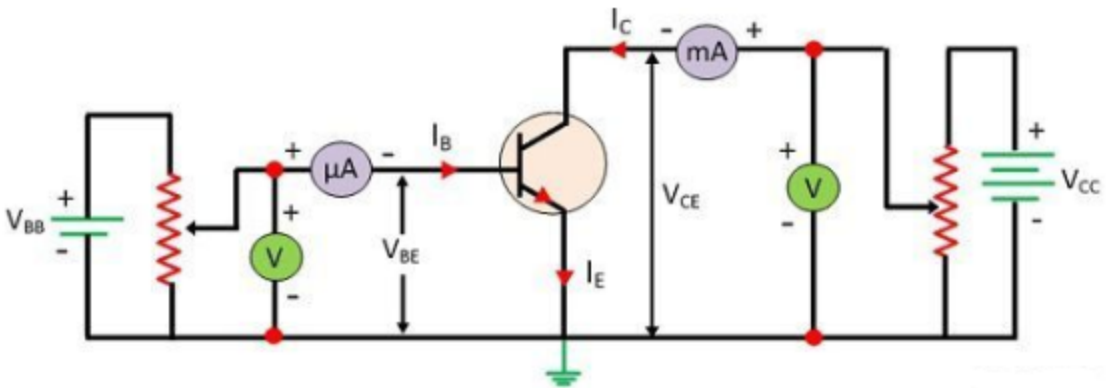
b) Value of I_B for a desired I_C of 5mA



Problem 2

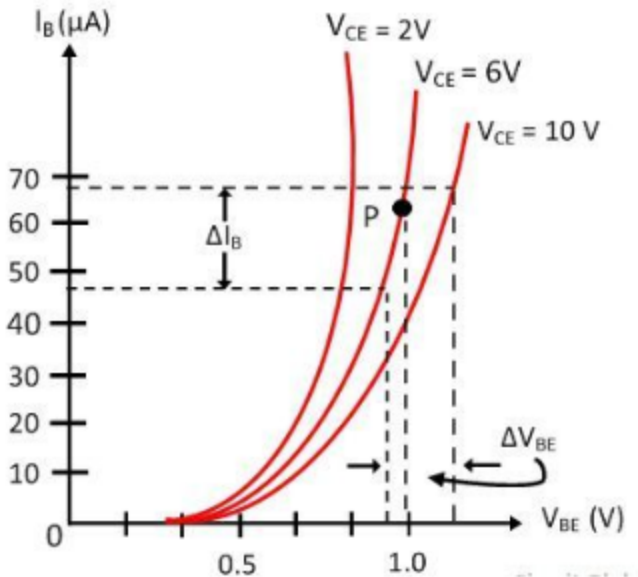
Find the values of I_C and I_E for a transistor with α_{dc}=0.97 and I_B =50μA. Find β_{dc} of transistor used.

Common-emitter input characteristics



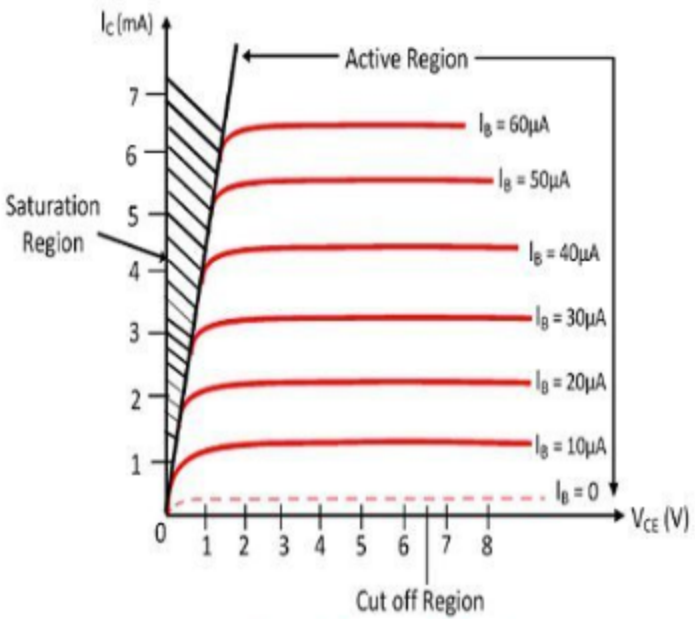
1. The base to emitter voltage varies by adjusting the potentiometer R_1. And the collector to emitter voltage varied by adjusting the potentiometer R_2.
2. For the various setting, the current and voltage are taken from the milliammeters and voltmeter. On the basis of these readings, the input and output curve plotted on the curve

Common-emitter input characteristics



1. The curve plotted between base current I_B and the base-emitter voltage V_{EB} is called Input characteristics curve.
2. For drawing the input characteristic the reading of base currents is taken through the ammeter on emitter voltage V_{BE} at constant collector-emitter current.
3. The base current I_B increases with the increases in the emitter-base voltage V_{BE}.

Common-emitter output characteristics



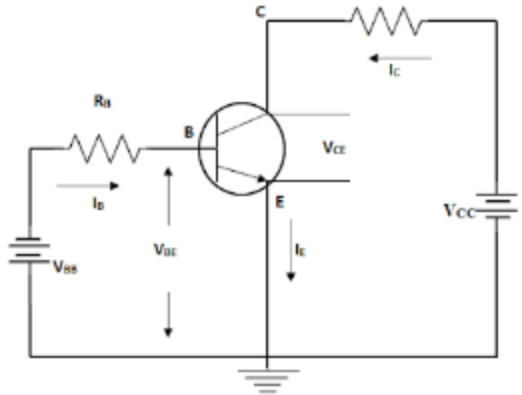
1. The curve draws between collector current I_C and collector-emitter voltage V_{CE} at a constant base current I_B is called output characteristic.
2. In the active region, the collector current increases slightly as collector-emitter V_{CE} current increases. The slope of the curve is quite more than the output characteristic of CB configuration.
3. When the V_{CE} falls, the I_C also decreases rapidly. The collector-base junction of the transistor always in forward bias and work saturate.

DC Load line

1. DC Load line for a transistor circuit is a straight line drawn on transistor output characteristics.

2. For a common emitter(C_E) circuit, the load line is a graph of collector current(I_C) versus collector-emitter voltage (V_{CE}), for a given value of collector resistance(R_C) and a given supply voltage(V_{CC}).

Procedure for drawing DC Load line



The dc supply voltage VCC forward biases base-emitter and reverse biases collector-base junction.

Apply KVL to base-emitter circuit

$$V_{CC}=I_B R_B+V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

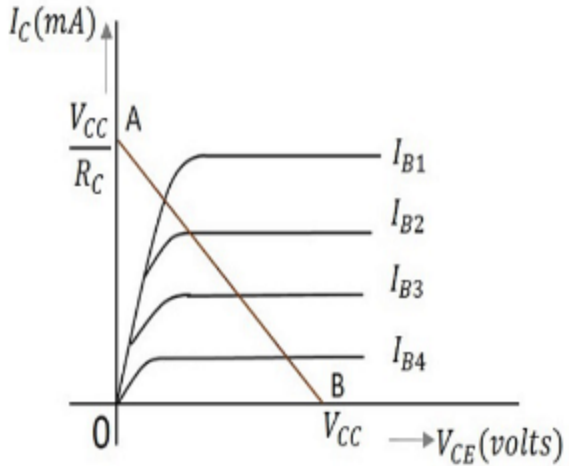
Procedure for drawing DC Load line

The collector current is given by,

$$I_C = h_{FE} I_B$$

Apply KVL to collector-emitter circuit

$$V_{CC} = I_C R_C + V_{CE}$$



To obtain A

When $V_{CE} = 0$, the I_C is maximum and is equal to V_{CC}/R_C.

This gives the maximum value of V_{CE}. This is shown as

$$V_{CE} = V_{CC} - I_C R_C \quad V_{CE} = V_{CC} - I_C R_C$$
$$0 = V_{CC} - I_C R_C \quad 0 = V_{CC} - I_C R_C$$
$$I_C = V_{CC} R_C \quad I_C = V_{CC} R_C$$

This gives the point A ($OA = V_{CC}/R_C$) on I_C axis, shown in the figure.

Procedure for drawing DC Load line

To obtain B

When the $I_C = 0$, then V_{CE} is maximum and will be equal to the V_{CC}.

This gives the maximum value of I_C.

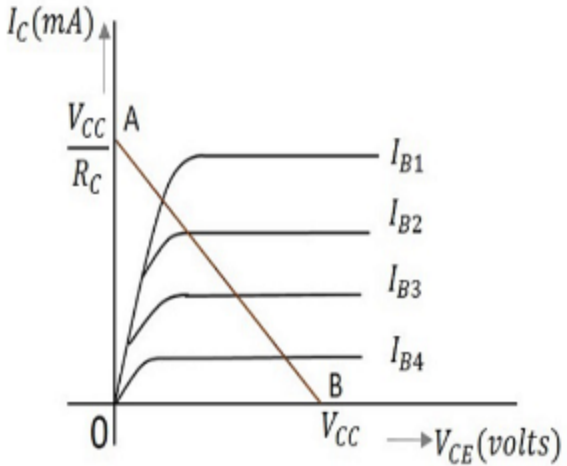
This is shown as

$V_{CE}=V_{CC}-I_CR_CV_{CE}=V_{CC}-I_CR_C$

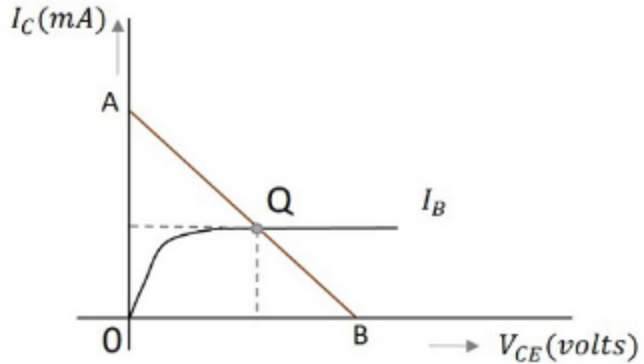
$=V_{CC}=V_{CC}$

(As $I_C = 0$)

This gives the point B, which means (OB = V_{CC}) on The collector voltage axis shown in the above figure.



Q-Point



1. The dc bias point or Q point also known as dc operating point.
2. It identifies the transistor collector current and collector-emitter voltage when there is no input signal at base terminal.
3. The intersection of dc load line with output characteristics curve gives the coordinates of the Q point

Transistor biasing

1. Transistor needs to be operated in an appropriate region based on the application of circuit.

2. When transistor is used as amplifier it must be in active region i.e., base-emitter is forward biased and collector-base junction is reverse biased.

3. The dc voltages and currents in circuit are established by using resistance network .

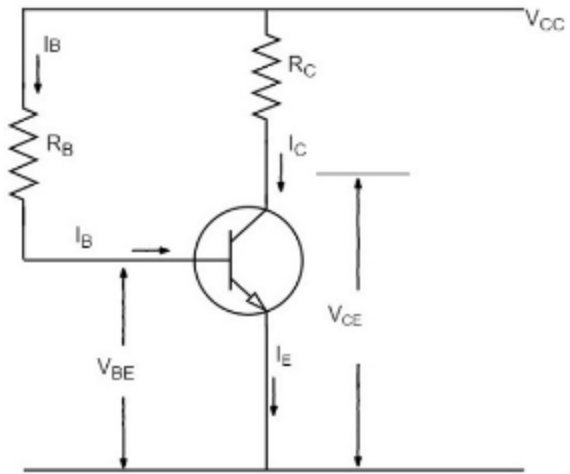
4. This process is called biasing and resistance network is called bias circuit.

Transistor biasing

Three biasing circuits

1. Base bias circuit
2. Collector-base bias circuit
3. Voltage divider bias circuit

Base bias circuit



Apply KVL to base emitter circuit

$V_{CC}=I_B R_B+V_{BE}$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \qquad \text{.....1}$$

As V_{BE}=0.7V for SI and 0.3V for GE $V_{CC}>>V_{BE}$

Therefore eqn 1 will be

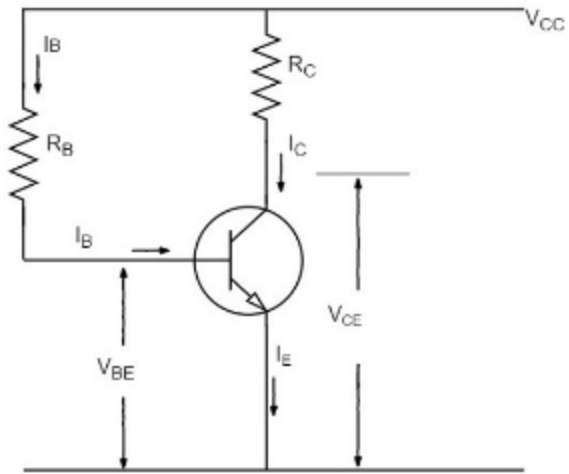
$$I_B = \frac{V_{CC}}{R_B} \qquad I_C = h_{FE} I_B$$

Apply KVL to collector emitter circuit

$V_{CC} = I_C R_C + V_{CE}$

$V_{CE} = V_{CC} - I_C R_C$

Procedure for design of Base bias circuit



The values of V_{CC}, V_{CE}, V_{BE}, I_C and h_{FE} will be given.
The design steps are as follows

1. Calculate RC using the relation

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} \quad \text{.....1}$$

2. Then calculate I_B using relation

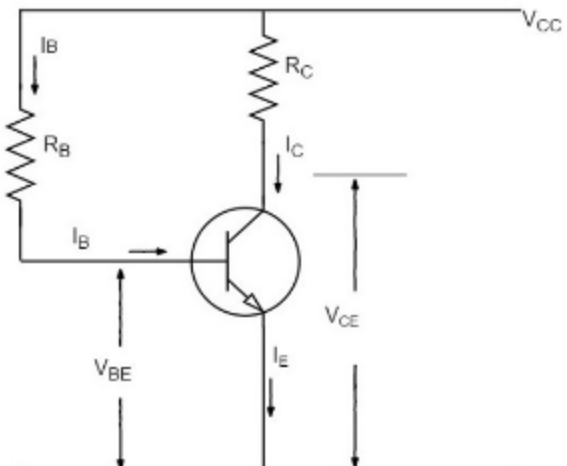
$$I_B = \frac{I_C}{h_{FE}}$$

3. Finally calculate R_B using relation

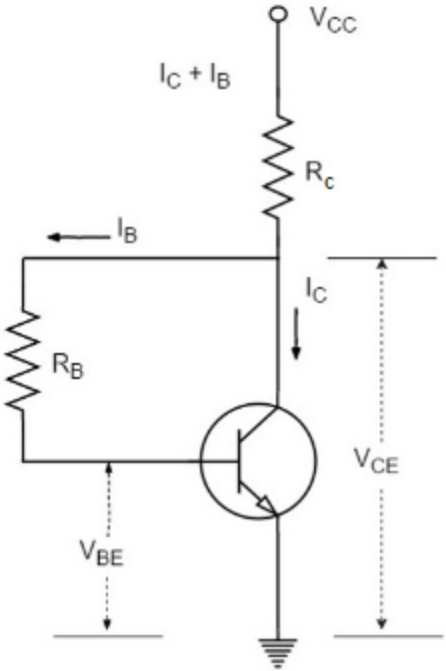
$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

Problem 2

For the base bias circuit shown below, find I_B,I_C and V_{CE} if R_C=2.2kΩ, R_B=470KΩ, V_{CC}=18V, h_{FE}=100, V_{BE}=0.7V. Draw DC load line and indicate the Q point.



Collector-to-base bias circuit



Apply KVL to path V_{CE}, I_BR_B and V_{BE}

$$V_{CE} - I_B R_B - V_{BE} = 0 \quad \text{.....1}$$

$$V_{CE} = I_B R_B + V_{BE} \quad \text{.....2}$$

$$I_B = \frac{V_{CE} - V_{BE}}{R_B}$$

Apply KVL to collector-emitter circuit,

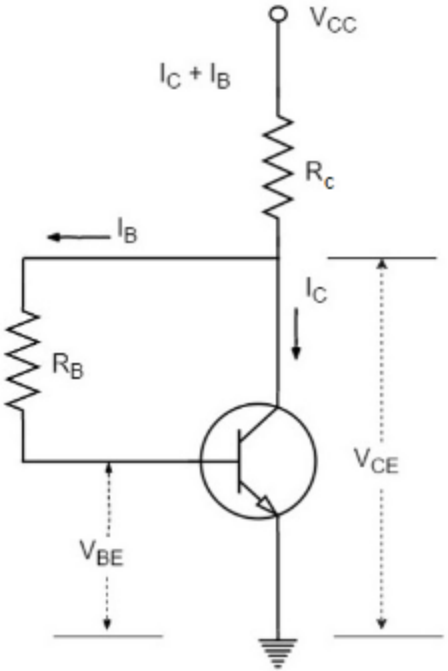
$$V_{CC} - R_C(I_B + I_C) - V_{CE} = 0$$

$$V_{CE} = V_{CC} - R_C(I_B + I_C) \quad \text{.....3}$$

Substitute V_{CE} from eqn 1 in eqn 3,

$$I_B R_B + I_B R_C + I_C R_C = V_{CC} - V_{BE}$$

Collector-to-base bias circuit



Using $I_C = h_{FE} I_B$

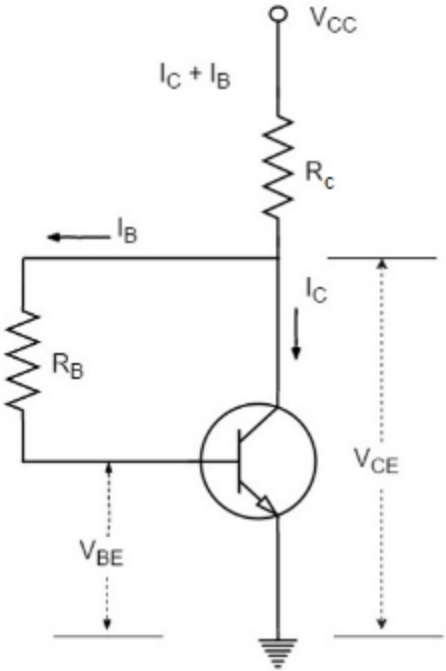
$$I_B R_B + I_B R_C + h_{FE} I_B R_C = V_{CC} - V_{BE} \quad \text{.....1}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + h_{FE}) R_C} \quad \text{.....2}$$

Stability of the operating point
If IC increases above design level,

- $I_C R_C$ increases
- V_{CE} decreases
- I_B decreases
- $I_C = h_{FE} I_B$ decreases

Design procedure of Collector-to-base bias circuit



The values of V_{CC}, V_{CE}, V_{BE}, I_C and h_{FE} will be given.
The design steps are as follows

1. Calculate IB using the relation

$$I_B = \frac{IC}{h_{FE}}$$

2. Then calculate RC using relation

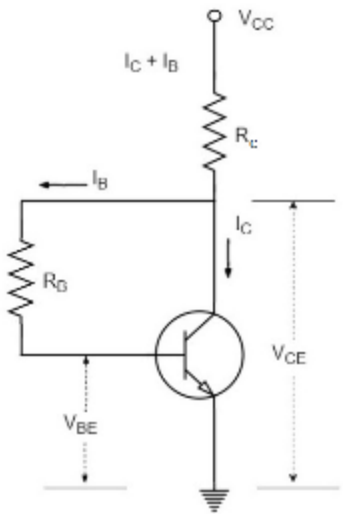
$$R_C = \frac{V_{CC} - V_{CE}}{I_C + I_B}$$

3. Then calculate RC using relation

$$R_B = \frac{V_{CE} - V_{BE}}{I_B}$$

Problem 3

For the collector-to-base bias circuit shown below, Determine the V_{CE} and I_C levels. The circuit has V_{CC} =15V, R_C=1.8kΩ, R_B=39KΩ, V_{BE}=0.7V, h_{FE}=50, V_{BE}=0.7V. Draw DC load line and indicate the Q point.



Voltage divider bias circuit(approximate analysis)

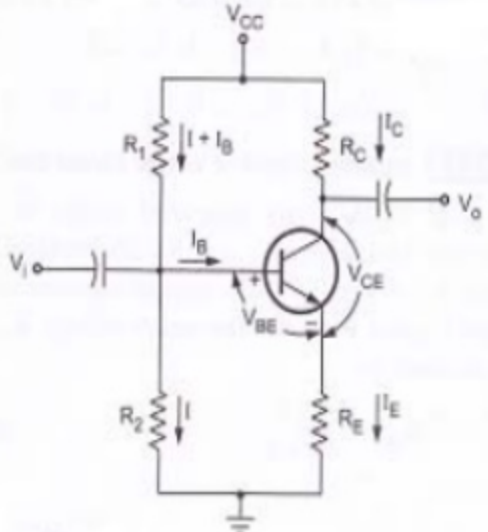


Fig. Voltage divider bias circuit

Also known as emitter current bias

From fig:

$I_1 = I_2 + I_B$

As I_B is very small $I_2 >> I_B$, hence $I_2 \approx I_1$

$$V_{CC} = I_1 R_1 + I_2 R_2$$

$$I_2 = \frac{V_{CC}}{R_1 + R_2}$$

Voltage across R2 is VB=I2R2,

$$V_B = \frac{V_{CC} R_2}{R_1 + R_2}$$

$$V_B = V_{BE} + V_E$$

$$V_E = V_B - V_{BE}$$

VB is constant

Voltage divider bias circuit(approximate analysis)

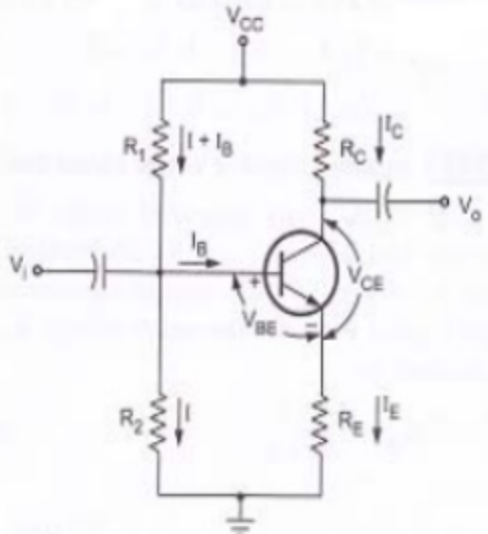


Fig. Voltage divider bias circuit

But $V_E = I_E R_E$

$$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{V_E}{R_E}$$

$I_E = I_B + I_C \approx I_C$, since base current is small

Apply KVL to collector emitter circuit,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

Since $I_E \approx I_C$,

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Problem 4

A voltage divider bias circuit has V_{CC}=18V, R_1=33kΩ, R_2=12kΩ, R_E=1KΩ, R_C=1.2kΩ, h_{FE}=50. Taking V_{BE}=0.7V, find V_E,V_{CE},I_C and V_C. Draw the DC load line and locate Q point

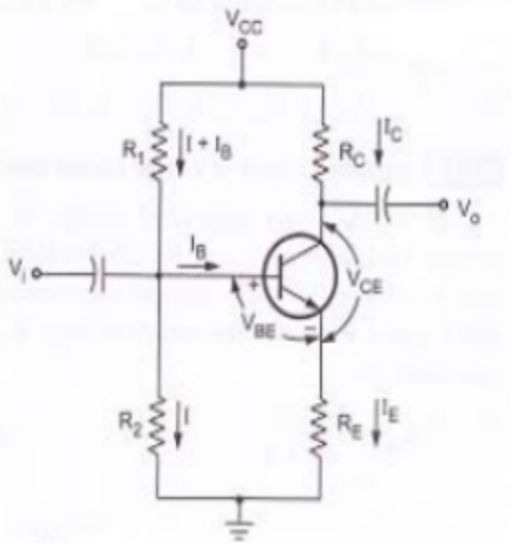
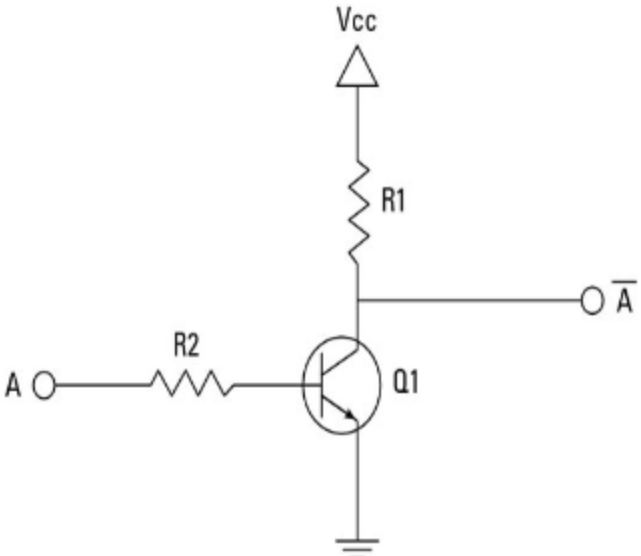


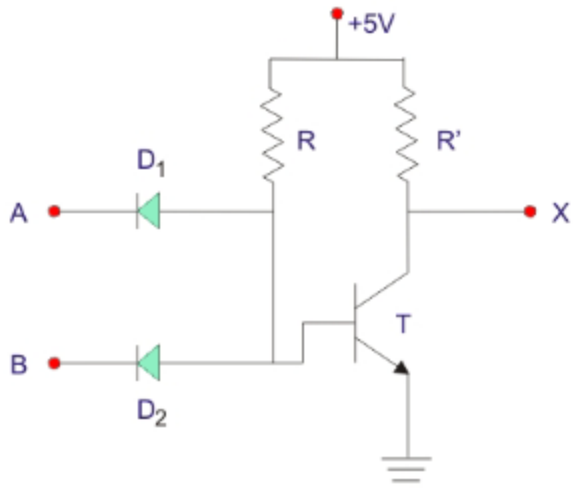
Fig. Voltage divider bias circuit

Transistor as a switch: NOT Gate



1. A NOT gate simply inverts its input. If the input is HIGH, the output is LOW, and if the input is LOW, the output is HIGH.
2. The input is connected through resistor R2 to the transistor's base.
3. When no voltage is present on the input, the transistor turns off. When the transistor is off, no current flows through the collector-emitter path.
4. Thus, current from the supply voltage (Vcc in the schematic) flows through resistor R1 to the output. In this way, the circuit's output is HIGH when its input is LOW.

DTL NAND Gate



1. When both input A and B are given with 0 V, both of the diodes are in forward biased condition that is in ON condition.
2. Supply voltage will get path to the ground through diode D_1 and D_2.
3. When both of the inputs are given with +5 V that is logical 1, both of the diodes are in OFF condition and hence supply voltage will appear at the base terminal of the transistor T which makes it switched ON and supply voltage gets a path to the ground through this transistors.

References

1. https://www.tutorialspoint.com/amplifiers/methods_of_transistor_biasing.htm
2. https://www.britannica.com/technology/transistor

Thank You