

1. Description

1.1. Project

Project Name	STM32F411-adc
Board Name	custom
Generated with:	STM32CubeMX 6.6.1
Date	09/29/2022

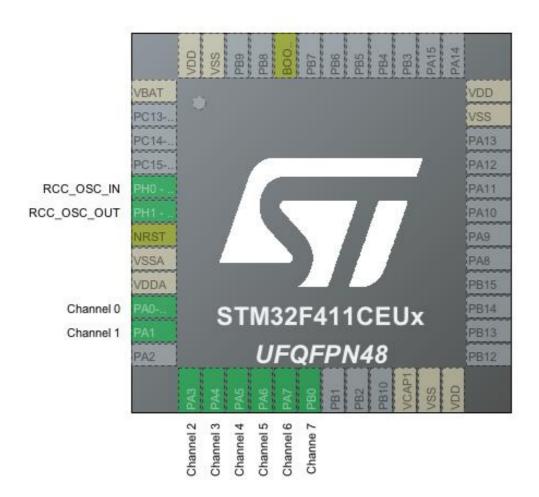
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F411
MCU name	STM32F411CEUx
MCU Package	UFQFPN48
MCU Pin number	48

1.3. Core(s) information

Core(s)	Arm Cortex-M4

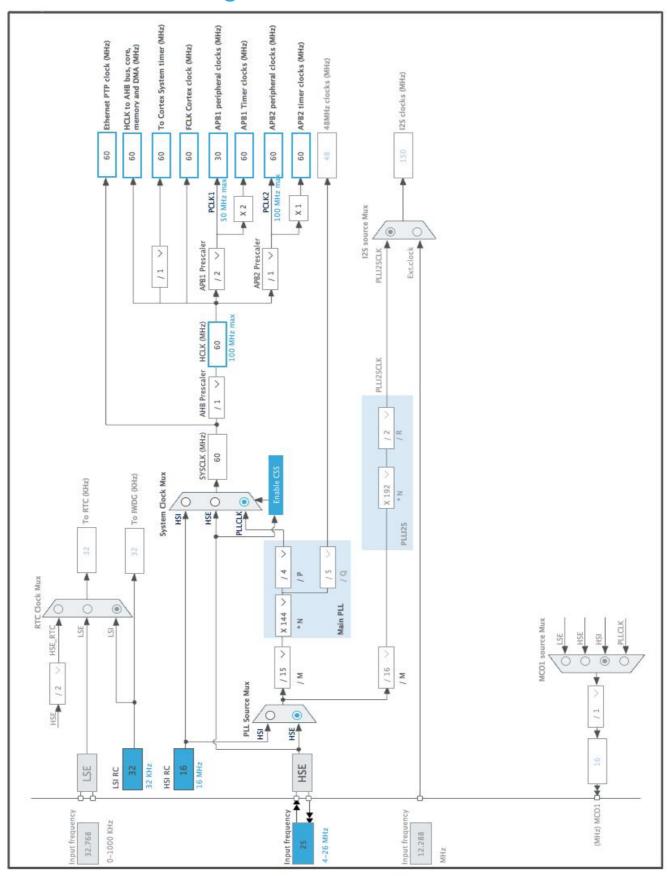
2. Pinout Configuration



3. Pins Configuration

Pin Number UFQFPN48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PH0 - OSC_IN	I/O	RCC_OSC_IN	
6	PH1 - OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0-WKUP	I/O	ADC1_IN0	Channel 0
11	PA1	I/O	ADC1_IN1	Channel 1
13	PA3	I/O	ADC1_IN3	Channel 2
14	PA4	I/O	ADC1_IN4	Channel 3
15	PA5	I/O	ADC1_IN5	Channel 4
16	PA6	I/O	ADC1_IN6	Channel 5
17	PA7	I/O	ADC1_IN7	Channel 6
18	PB0	I/O	ADC1_IN8	Channe 7
22	VCAP1	Power		
23	VSS	Power		
24	VDD	Power		
35	VSS	Power		
36	VDD	Power		
44	воото	Boot		
47	VSS	Power		
48	VDD	Power		

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value	
Project Name	STM32F411-adc	
Project Folder	/Users/pschatzmann/Documents/Projects/STM32CubeIDE/STM32F411-adc	
Toolchain / IDE	STM32CubeIDE	
Firmware Package Name and Version	STM32Cube FW_F4 V1.27.1	
Application Structure	Advanced	
Generate Under Root	Yes	
Do not generate the main()	Yes	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_ADC1_Init	ADC1
5	MX_TIM3_Init	TIM3

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F411
MCU	STM32F411CEUx
Datasheet	DS10314_Rev6

6.2. Parameter Selection

Temperature	25
Vdd	1.7

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

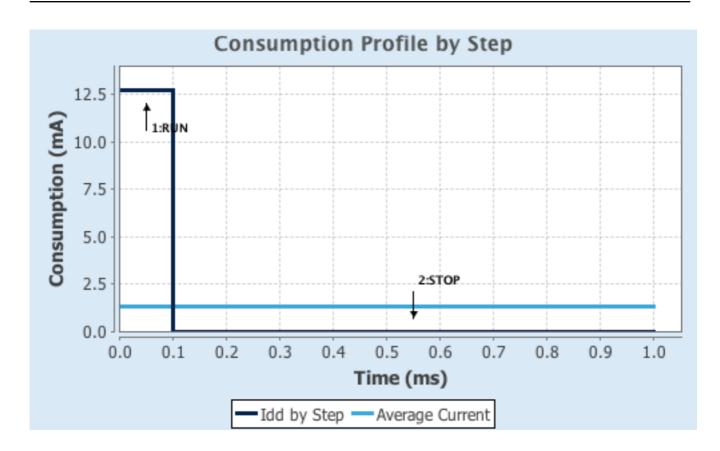
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	1.7	1.7
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	SRAM	n/a
CPU Frequency	100 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LPLV Flash- PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	12.7 mA	9 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	125.0	0.0
Ta Max	104.31	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	1.28 mA
Battery Life	3 months, 19	Average DMIPS	125.0 DMIPS
	days, 6 hours		

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1 mode: IN0 mode: IN1 mode: IN3 mode: IN4 mode: IN5 mode: IN6 mode: IN7 mode: IN8

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC Settings:

Clock Prescaler PCLK2 divided by 2

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Enabled Scan Conversion Mode Continuous Conversion Mode Disabled Discontinuous Conversion Mode Disabled **DMA Continuous Requests**

Enabled *

End Of Conversion Selection EOC flag at the end of all conversions *

ADC_Regular_ConversionMode:

Number Of Conversion 8 *

External Trigger Conversion Source Timer 3 Trigger Out event *

External Trigger Conversion Edge Trigger detection on the rising edge

Rank 2 *

Channel 0 Channel Sampling Time 3 Cycles Rank 3 *

Channel 0 Channel Sampling Time 3 Cycles Rank 4 *

Channel Channel 0 Sampling Time 3 Cycles Rank 5 *

Channel 0 Channel

Sampling Time 3 Cycles

<u>Rank</u> 6 *

Channel Channel 0
Sampling Time 3 Cycles
Rank 7 *

Channel Channel 0
Sampling Time 3 Cycles

<u>Rank</u> **8** *

Channel Channel 0
Sampling Time 3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 1 WS (2 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

TIM Prescaler Selection Disabled

HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

7.3. SYS

Timebase Source: SysTick

7.4. TIM3

mode: Clock Source

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 600 *
Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 44100 *

Internal Clock Division (CKD) No Division auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Enable (Trigger delayed for master/slaves simultaneous start)

*

Trigger Event Selection Update Event *

^{*} User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max Speed	User Label
ADC1	PA0-WKUP	ADC1 IN0	Analog mode	No pull-up and no pull-down	n/a	Channel 0
/.20.	PA1	ADC1 IN1	Analog mode	No pull-up and no pull-down	n/a	Channel 1
	PA3	ADC1 IN3	Analog mode	No pull-up and no pull-down	n/a	Channel 2
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	Channel 3
	PA5	ADC1_IN5	Analog mode	No pull-up and no pull-down	n/a	Channel 4
	PA6	ADC1_IN6	Analog mode	No pull-up and no pull-down	n/a	Channel 5
	PA7	ADC1_IN7	Analog mode	No pull-up and no pull-down	n/a	Channel 6
	PB0	ADC1_IN8	Analog mode	No pull-up and no pull-down	n/a	Channe 7
RCC	PH0 - OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1 - OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	High *

ADC1: DMA2_Stream0 DMA request Settings:

Mode: Circular *

Use fifo: Enable *

FIFO Threshold: Full
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Half Word
Memory Data Width: Half Word

Peripheral Burst Size: 4 Increment *
Memory Burst Size: 4 Increment *

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	15	0	
DMA2 stream0 global interrupt	true	0	0	
PVD interrupt through EXTI line 16	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
ADC1 global interrupt	unused			
TIM3 global interrupt	unused			
FPU global interrupt	unused			

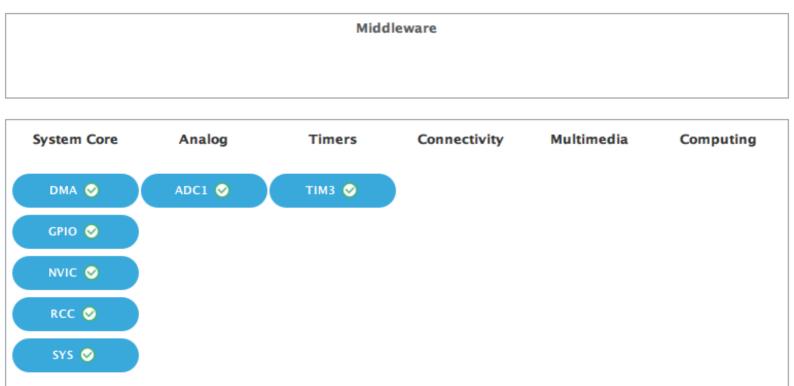
8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA2 stream0 global interrupt	false	true	true

* User modified value

9. System Views

- 9.1. Category view
- 9.1.1. Current



10. Docs & Resources

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