RTL Report

Testbench	Pass (Pass/Failed)
Clock Cycle	50 (ns)
Total Time	13850 (ns)

Synthesis Report

Testbench	Pass (Pass/Failed)
Clock Cycle	50 (ns)
Cell Area	2125747.459873 (Please report **Total cell area**)
Total Time	13850 (ns)
Area*Time^2	29441602321

APR Report

Testbench	Pass (Pass/Failed)
Clock Cycle	50 (ns)
Cell Area	220096.766 (Please report **Total area of Core)**
Total Time	13850 (ns)
Area*Time^2	42219511896035

How to report area in Design Vision?

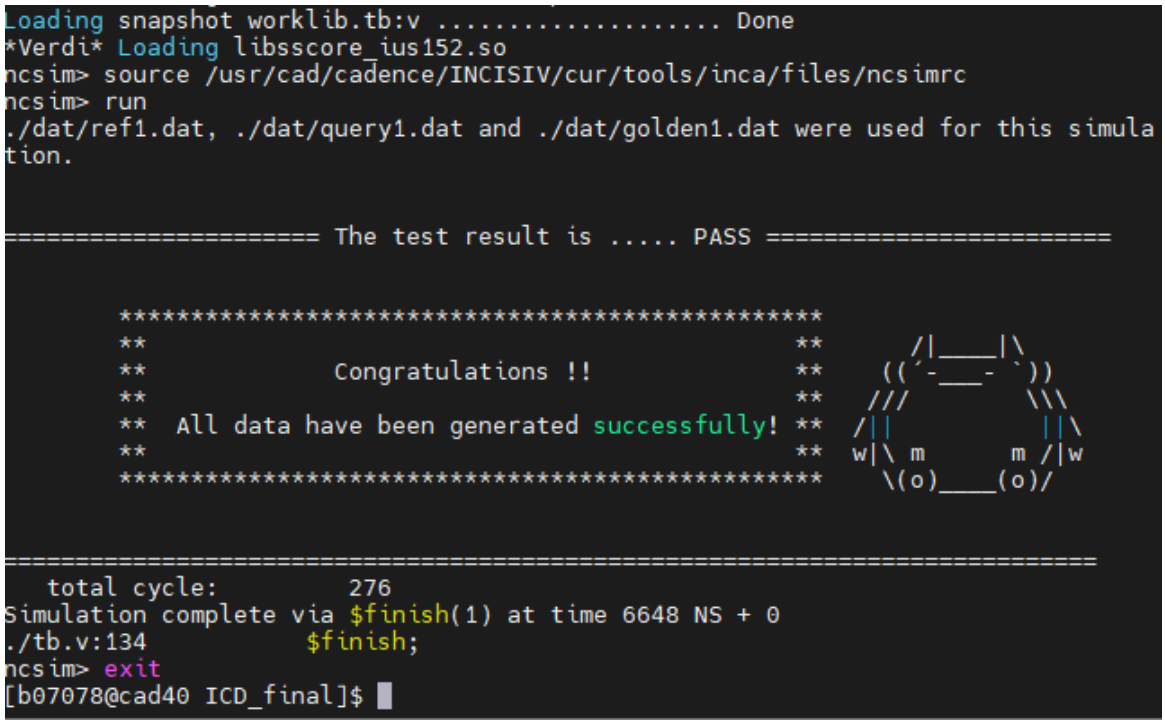
➔ report_area > autoseller_area.txt, find **Total cell area.**

How to report area in Innovus?

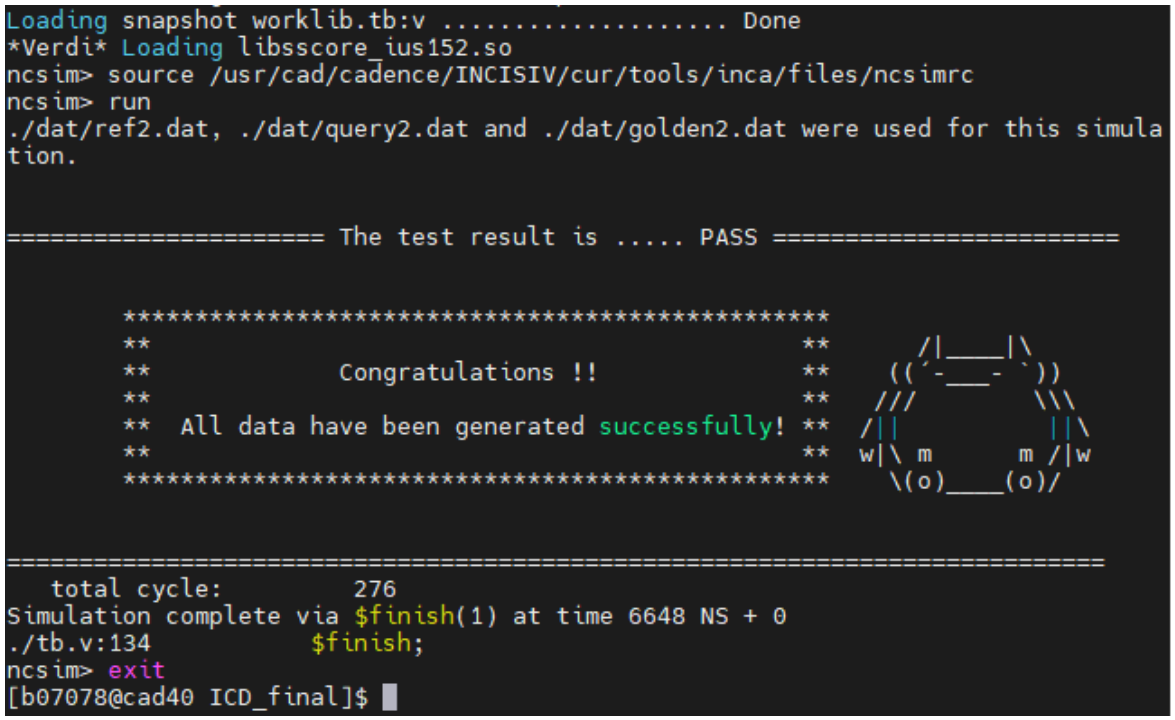
➔ File > Report > Summary > choose Text only, file name: **summaryReport.rpt**>OK, find **Total area of Core.**

RTL Simulation Result (截圖)

tb1



tb2



Synthesis Simulation Result (截圖)

tb1

```
Loading snapshot worklib.tb:v ..................... Done
*Verdi* Loading libsscore_ius152.so
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
./dat/ref1.dat, ./dat/query1.dat and ./dat/golden1.dat were used for this simula
tion.


====================== The test result is ..... PASS ========================


        ************************************************
        **                                            **      /|____|\
        **             Congratulations !!             **    ((´-___-`))
        **                                            **   ///        \\\
        **  All data have been generated successfully! **  /||          ||\
        **                                            **  w|\ m      m /|w
        ************************************************    \(o)____(o)/


================================================================================
   total cycle:         276
Simulation complete via $finish(1) at time 6648 NS + 0
./tb.v:134           $finish;
ncsim> exit
[b07078@cad40 ICD_final]$
```

tb2

```
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
./dat/ref2.dat, ./dat/query2.dat and ./dat/golden2.dat were used for this simula
tion.


====================== The test result is ..... PASS ========================


        ************************************************
        **                                            **      /|____|\
        **             Congratulations !!             **    ((´-___-`))
        **                                            **   ///        \\\
        **  All data have been generated successfully! **  /||          ||\
        **                                            **  w|\ m      m /|w
        ************************************************    \(o)____(o)/


================================================================================
   total cycle:         276
Simulation complete via $finish(1) at time 6648 NS + 0
./tb.v:134           $finish;
ncsim> exit
[b07078@cad40 ICD_final]$
```

Synthesis Timing Report

```
PE1/U171/Y (NAND2BX1)                   0.27      9.58 r
PE1/U175/Y (AND2X1)                     0.24      9.82 r
PE1/U176/Y (OAI211X1)                   0.13      9.95 f
PE1/U178/Y (AOI31X1)                    0.21     10.16 r
PE1/U183/Y (AOI211X1)                   0.13     10.28 f
PE1/U184/Y (NOR3BXL)                    0.34     10.63 r
PE1/U20/Y (CLKINVX1)                    0.14     10.77 f
PE1/U187/Y (AOI31X1)                    0.18     10.94 r
PE1/U188/Y (CLKINVX1)                   0.11     11.05 f
PE1/U294/Y (NAND3BX1)                   0.27     11.32 r
PE1/U23/Y (INVX3)                       0.22     11.54 f
PE1/U17/Y (AOI31XL)                     0.37     11.91 r
PE1/U14/Y (NAND4X2)                     0.34     12.25 f
PE1/U3/Y (OAI221X1)                     0.57     12.82 r
PE1/H[4] (PE_0)                         0.00     12.82 r
U6382/Y (NAND2BXL)                      0.24     13.06 f
U13358/Y (OAI222XL)                     0.58     13.64 r
U13359/Y (OAI222XL)                     0.25     13.89 f
U13369/Y (AO22X1)                       0.29     14.18 f
U6380/Y (OAI21X1)                       0.30     14.48 r
U7132/Y (NOR3X1)                        0.28     14.76 f
U6373/Y (NOR3BX1)                       0.27     15.03 f
U7136/Y (NOR3BX1)                       0.26     15.29 f
U7055/Y (AND4X1)                        0.25     15.54 f
U6378/Y (NOR3BX1)                       0.22     15.76 f
U7135/Y (NOR3BX1)                       0.28     16.03 f
U7149/Y (AOI31X1)                       0.56     16.59 r
U7148/Y (CLKBUFX3)                      0.46     17.05 r
U9524/Y (OAI22XL)                       0.17     17.22 f
U9523/Y (AOI221XL)                      0.37     17.59 r
U7688/Y (NAND4X1)                       0.15     17.74 f
pos_query_r_reg[3]/D (DFFRX1)           0.00     17.74 f
data arrival time                                17.74

clock clk (rise edge)                  24.00     24.00
clock network delay (ideal)             1.00     25.00
clock uncertainty                      -0.10     24.90
pos_query_r_reg[3]/CK (DFFRX1)          0.00     24.90 r
library setup time                     -0.11     24.79
data required time                               24.79
-----------------------------------------------------------
data required time                               24.79
data arrival time                               -17.74
-----------------------------------------------------------
slack (MET)                                      7.05
```

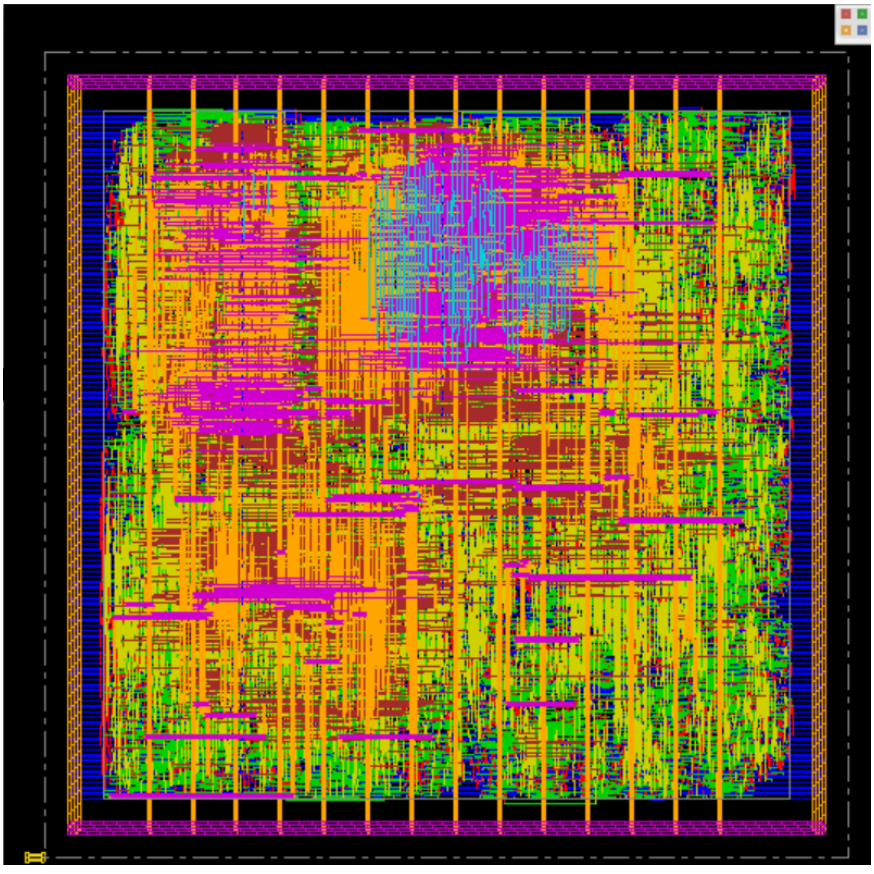
Synthesis Area Report

```
Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:                         1371
Number of nets:                         16236
Number of cells:                        14254
Number of combinational cells:          12203
Number of sequential cells:              2018
Number of macros/black boxes:               0
Number of buf/inv:                       1646
Number of references:                     118

Combinational area:             104588.696209
Buf/Inv area:                     8203.534067
Noncombinational area:           71462.239006
Macro/Black Box area:                0.000000
Net Interconnect area:         1949696.524658

Total cell area:                176050.935215
Total area:                    2125747.459873
```

Synthesis Power Report

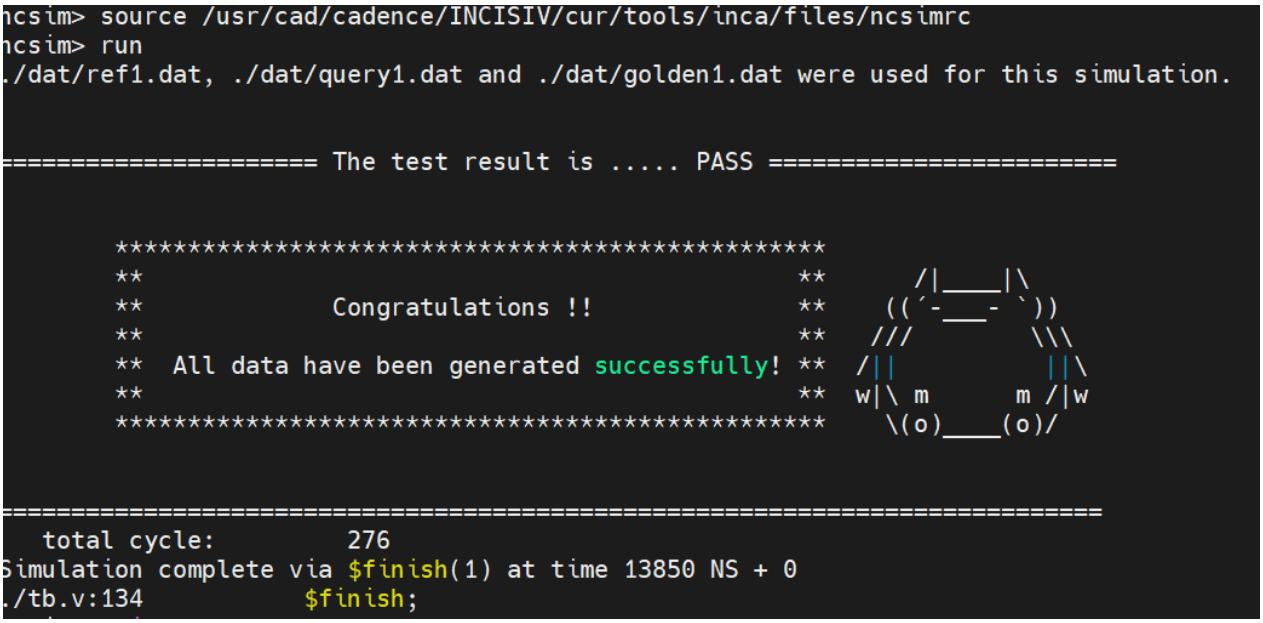
```
Design        Wire Load Model            Library
------------------------------------------------
SW                    tsmc13_wl10       slow


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   2.1885 mW   (98%)
  Net Switching Power  =  48.3596 uW    (2%)
                         ---------
Total Dynamic Power    =   2.2369 mW  (100%)

Cell Leakage Power     =  31.9993 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000             0.0000  (   0.00%)
register           2.1827        4.5407e-03        1.4578e+07             2.2018  (  97.04%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational   5.8309e-03        4.3819e-02        1.7422e+07         6.7071e-02  (   2.96%)
--------------------------------------------------------------------------------------------------
Total              2.1885 mW     4.8359e-02 mW     3.1999e+07 pW          2.2689 mW
```

APR NanoRoute Innovus Result (截圖)

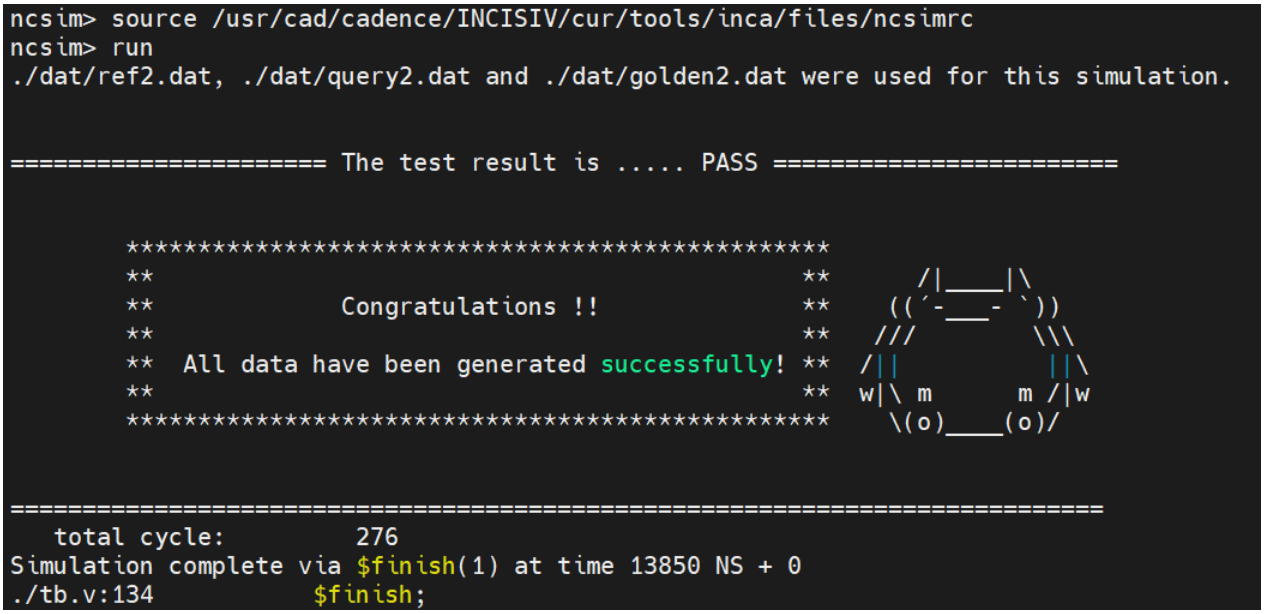


APR Simulation Result (截圖)

tb1



tb2



Report

(If you don’t pass APR, the score will be determined by the completeness of the report below)