EE201C 2017 Spring
Project 2 & 3

Project 2: Due by 11:55pm, May/28/2017
Project 3: Due by 11:55pm, June/18/2017

Contact Information

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- Email subject with [EE201C]

Projects Plan

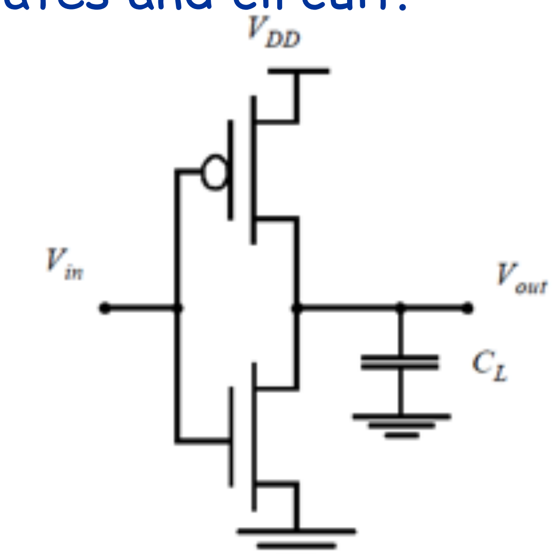
2 students per team.

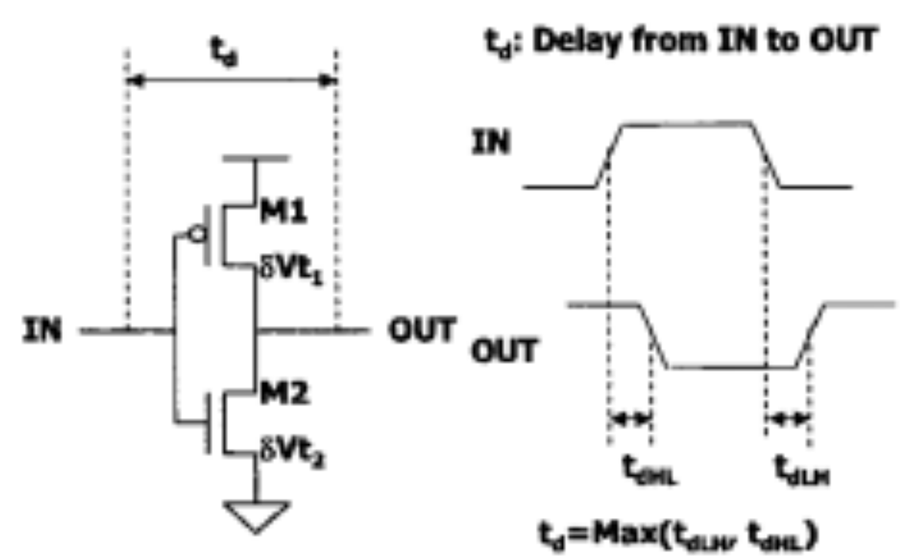
Project 2: SPICE-driven table-based stochastic modeling.

Project 3: high-sigma modeling.

Inverter Delay Variations

In nano-scaled CMOS devices, the random variations of dopant atoms in the channel region cause random variations in the transistor threshold voltage (Vt), known as "random (or discrete) dopant effect".
Result in threshold voltage mismatch between transistors on die and significant delay variation of logic gates and circuit.





As the delay distribution of a gate strongly depends on the device geometry and doping profile.

Hence, a statistical modeling and analysis of the delay of logic gate is necessary.
Considering random variation in transistors. Apply stochastic modeling to estimate distribution of propagation delay in given circuit.

Project 2

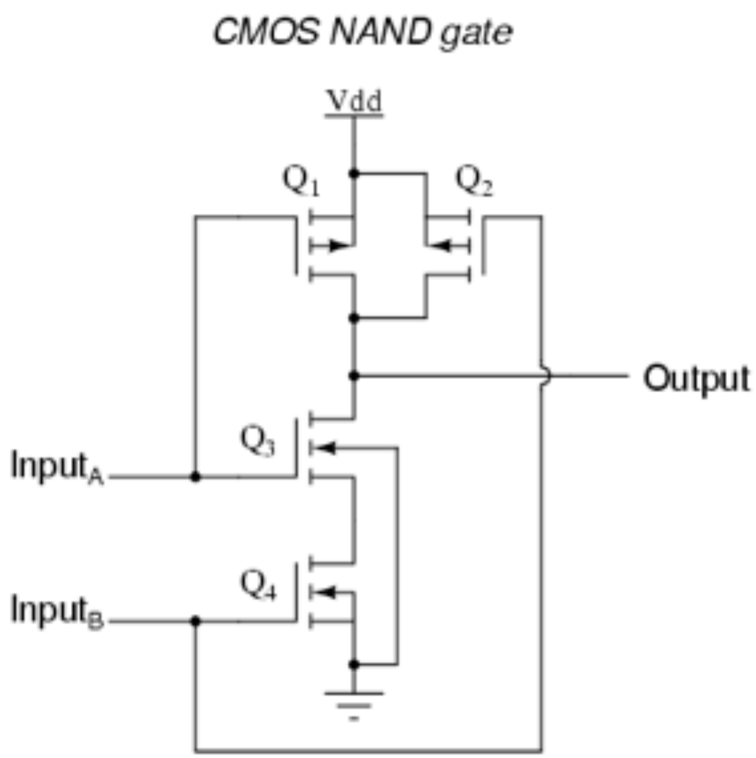
SPICE-driven table-based stochastic modeling

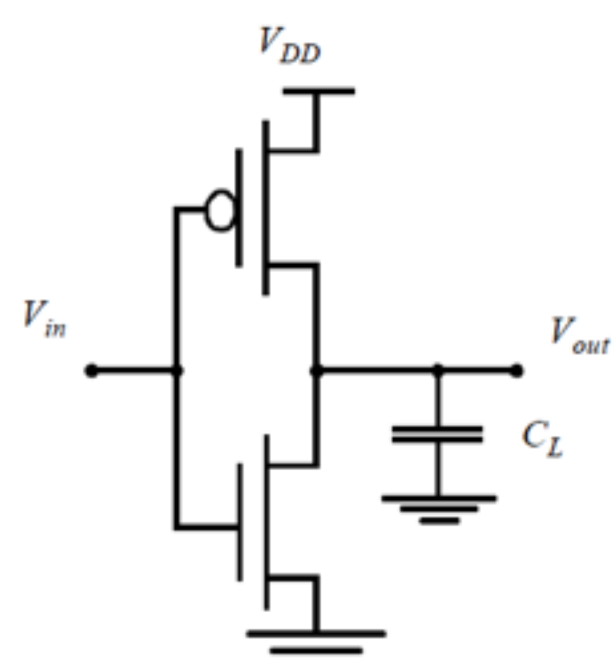
- Given the variations of threshold voltages in inverter and NAND, try to estimate the propagation delay of the circuit: the time delay between input side and output side.

- We calculate the CDF truncated between 3 sigma

- The schematic of one inverter and one NAND are shown as below. The whole circuit consists of 5 of both in cascade.

- The variations are modeled as below.





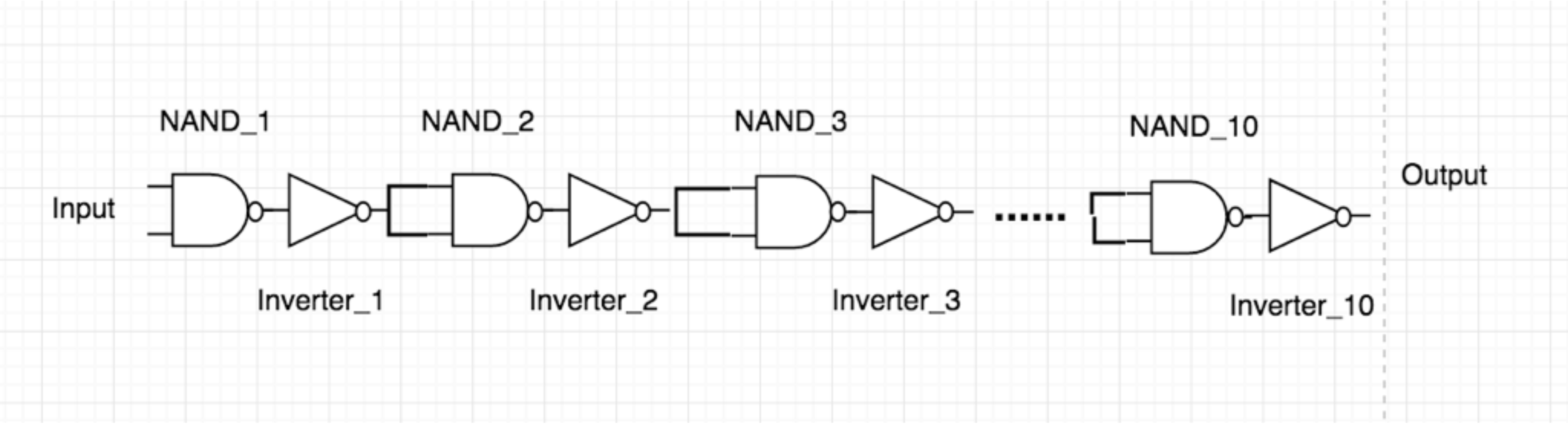
Variation Source:
V_{th} (threshold voltage) of Qi.

12 random variables in one inverter:
24 random variables in one NAND:
each Gaussian variable models the process variation on one threshold voltage;
NMOS:
nominal: 0.466
standard deviation: 0.0466
PMOS:
nominal: -0.4118
standard deviation: 0.04118

Device Model:
Use BSIM3 model for all MOSFETs

Project 2

Circuit Schema



Initial Table

	V1	V2	....	V360
1				
2				
3				
...				
500,000				

Project 2

SPICE-driven table-based stochastic modeling

- Given an initial tables of SPICE simulations regarding the circuit.
  - Find out the table at: (folder called data)
  - https://drive.google.com/drive/folders/0ByYz0oNQ5qYWOHp5dTlZNEdIUmM?usp=sharing

- Build a propagation delay model with required accuracy in terms of mean delay and PDF up to 3-sigma.
- Modeling with interpolation, extrapolation.
- Maybe need SPICE run for new samples that are not in the table.
  - Find out SPICE at: (file inside path_delay.rar)
  - https://drive.google.com/drive/folders/0ByYz0oNQ5qYWOHp5dTlZNEdIUmM?usp=sharing

- Reduce the total number of new SPICE runs for required accuracy (report your new runs in presentation and report)
- Store the new SPCIE simulations in non text-rich form here:
  - https://www.dropbox.com/sh/rpp7rhv1apfm6so/AACJfafbSAF8qP6VIMqDf8Jpa?dl=0
  - Will send an edit invitation later today to class.
  - Save your data in the format as the given table.

Project 3

High-sigma modeling (PDF for at least 6 sigma)

- Same problem settings (schema, variations distribution, etc.) as in project 2.
- Estimate the propagation delay of circuit with required accuracy in terms of mean delay up to 6-sigma. (High-sigma modeling)

- Goal: reduce overall SPICE runs (including those runs to build table).
- Using table from 2 to replace SPICE, i.e., we reduce the overall table lookup times

Submission List

- The values of mean delay time;

- The number & config. of tables lookups and simulations;

- The figures of delay time distribution;

- The matlab code to generate samples and write them into data file.

- The samples points (along with simulation results) that are not include in given table.

Grading Policy

Homework 1: 10
Homework 2: 10
Homework 3: 10 (to be released)
Project 1: 20
Project 2: 25
Project 3: 25

Timeline

May 16:
  Project spec and code release
May 18:
  Presentation on high-sigma modeling
May 21 (due at 11:55pm):
  Project proposal presentation sign up
May 23:
  Project proposal presentation part 1 (6 teams)
May 25:
  Project proposal presentation part 2 (10 teams)
May 28 (due at 11:55pm):
  Due of project 2 (code, report)
June 4 (due at 11:55pm):
  Final project presentation sign up
June 6:
  Project final presentation part 1 (6 teams)
June 8:
  Project final presentation part 1 (10 teams)
June 18:
  Due of project 3 (code, final report)

Sign-ups

2 students per team.
Sign up before the dues.

May 21 (due at 11:55pm):
Project (2 & 3) proposal presentation sign up:

https://docs.google.com/spreadsheets/d/1-mx8t2QgTLDW_bHf4kU8AsMlruwptgp7ARJRYPMSNfo/edit?usp=sharing

June 4 (due at 11:55pm):
Final project presentation sign up:

https://docs.google.com/spreadsheets/d/1Xbvib3ULK-erZzYd63TropHy2-vRZaex0Mqh1H8mqpI/edit?usp=sharing

Project Presentations

- Project proposal presentation:
  - 10min per group
  - Methods you plan to use, for both project 2 and project 3

- Final presentation:
  - 10 min per group
  - Methods you used for project 2 and project 3
  - Results you obtain at the time
  - What can be expected from your final report
  - Any other ideas

Reading Lists

Also upload on:
http://eda.ee.ucla.edu/EE201C/index.php?n=Spring2017.ReadingMaterials

R. Kanj, R. Joshi, S. Nassif, "Mixture Importance Sampling and its Application to the Analysis of SRAM Designs in the Presence of Rare Failure Events", Proc. DAC, 2006.

L. Dolecek, M. Qazi, D. Shah, and A. Chandrakasan, "Breaking the simulation barrier: SRAM evaluation through norm minimization," in ICCAD, 2008, pp. 322–329.

A. Singhee and R. A. Rutenbar, "Statistical blockade: a novel method for very fast monte carlo simulation of rare circuit events, and its application," in DATE, 2008, pp. 235–251.

W. Wu, W. Xu, R. Krishnan, Y.-L. Chen, and L. He, "REscope: High-dimensional statistical circuit simulation towards full failure region coverage," in Proceedings of the 51st DAC, 2014.

W. Wu, F. Gong, G. Chen, and L. He, "A fast and provably bounded failure analysis of memory circuits in high dimensions," in 19th ASP-DAC, 2014, pp. 424–429.

Wei Wu, Srinivas Bodapati, and Lei He, "Hyperspherical Clustering and Sampling for Rare Event Analysis with Multiple Failure Region Coverage", International Symposium on Physical Design (ISPD), 2016.