LAB2. BOOLEAN ALGEBRA AND, OR, AND NOT

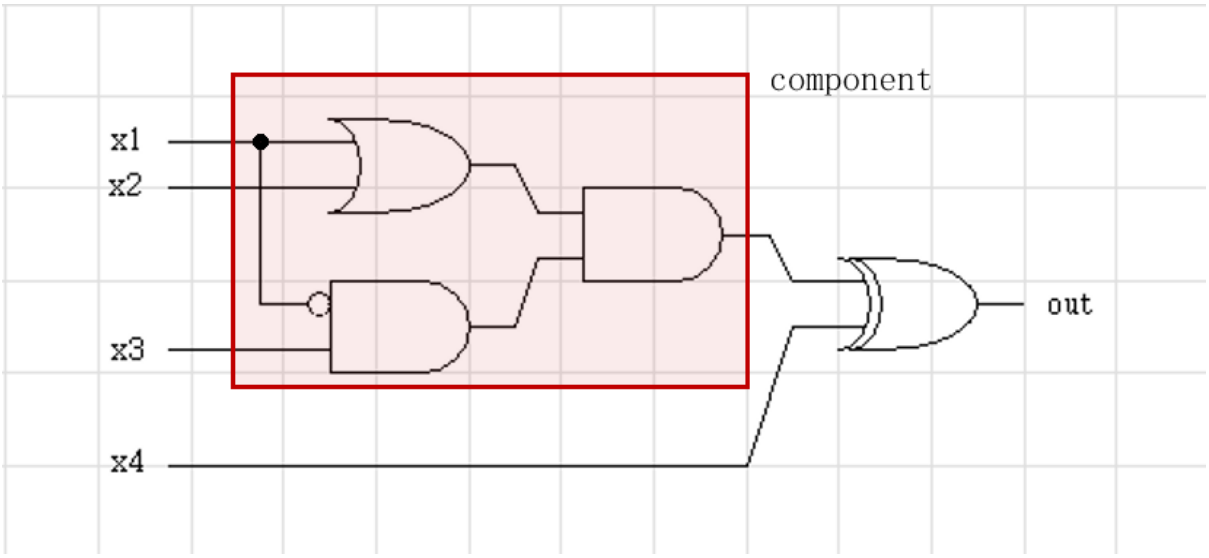
Lab. Hour: 7:00~10:00pm. 14th and 16th Mar. 2017
TA in charge: Jonguk kim (jrcforever@kaist.ac.kr,)

1. INTRODUCTION

In this lab, you will implement simple Boolean algebra circuit using Quartus2. You will implement the component and use it on the main architecture.

2. PROBLEM SPECIFICATION

You will implement the circuit below



You should make a red box component. You can use AND, OR, NOT and XOR logical operators defined in Quartur2. If you want, you can implement those logical operators. You must use "component" to implement circuits in red box.

Here are a few examples of truth table entities of the given circuit.

x1	x2	x3	x4	out
1	1	0	0	**0**
0	0	1	0	**0**
1	0	0	0	**0**
0	0	0	1	**1**
0	1	1	0	**1**

You can use inputs and an output as any ports in the board or recommend to use ports below.

- Input

Input	Meaning
sw 3	x4
sw 2	x3
sw 1	x2
sw 0	x1

- Output

Output	Meaning
Ledr0	out

3. REPORTS EVALUATION CRITERIA

Each item listed below will be checked when we evaluate your report and we take off some points if they do not exist or are improper.

PRELIMINARY REPORT

Please study about,

- What the VHDL is.
- What the the VHDL structure is. (explain components below)
  - Package, use clause, entity, architecture, process statements, sequential statements, etc.
- What the VHDL syntax is.
  - Explain data types (numeric, bit, bit_vector, etc.), operators (logical, relational, arithmetic).
  - Explain signal, constant, function, component, and variable statements.

FINAL REPORT

Please express your results into,

- Source code you implemented. You should explain how the code generally works. If your explanation is line-by-line comment, you might get minus.
- Function simulation and timing simulation result. Compare the difference between timing simulation and function simulation.
- RTL diagram of your lab and explain it
  (you can check the diagram at Tools > Netlist Viewers > RTL Viewer).
- Advantage of using component.

4. NOTE

TAs are very strict on copying and plagiarizing. You can refer to books, papers and internet pages. However, you cannot borrow them 'as is' if you do not explicitly indicate the source that you have cited. Also, it is strongly recommended that to write down what you've understood in your words.

Your report does not need to include a cover page and you can format it freely. (Because TA do not evaluate how beautifully you format it.) However, the content of the report should be precise.

We receive the report using the *KLMS*.

When you upload your compressed project file, you must follow the format described below.

Lab#_studuentid_name.zip / ex) Lab2_20113673_GildongHong.zip