COL215 - Assignment 2

Design overview of Digital clock

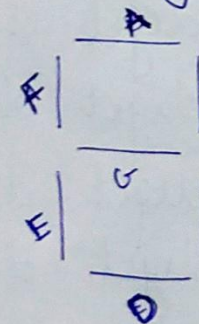
Inputs: 1) Clock (10 MHz, 10^7 cycles per sec)
2) 5-push buttons of different functions / features

Output: 4 seven-segment displays, each one displaying 4 out of 6 digits of time in 24 hr format i.e. hh:mm:ss, probably with a decimal point for denoting mode of display

Denote displays as d1, d2, d3, d4 and push-buttons as b1, b2, b3, b4, b5

User interface:

① Seven-segment display:

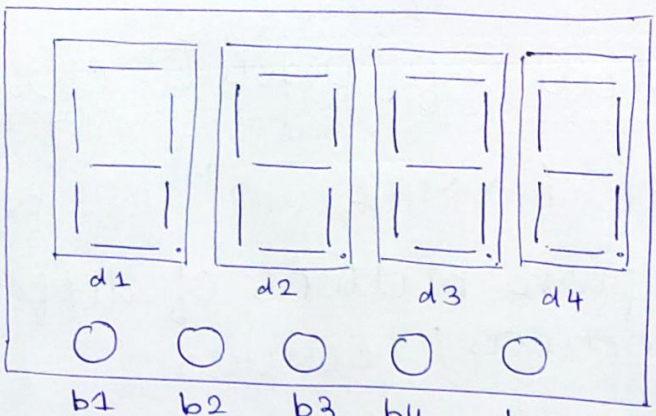


. ← optional decimal point

single digit display

A, B, C, D, E, F, G → segments (in bits)
P → decimal point (bit)

② Digital Clock



In display mode of digital clock,

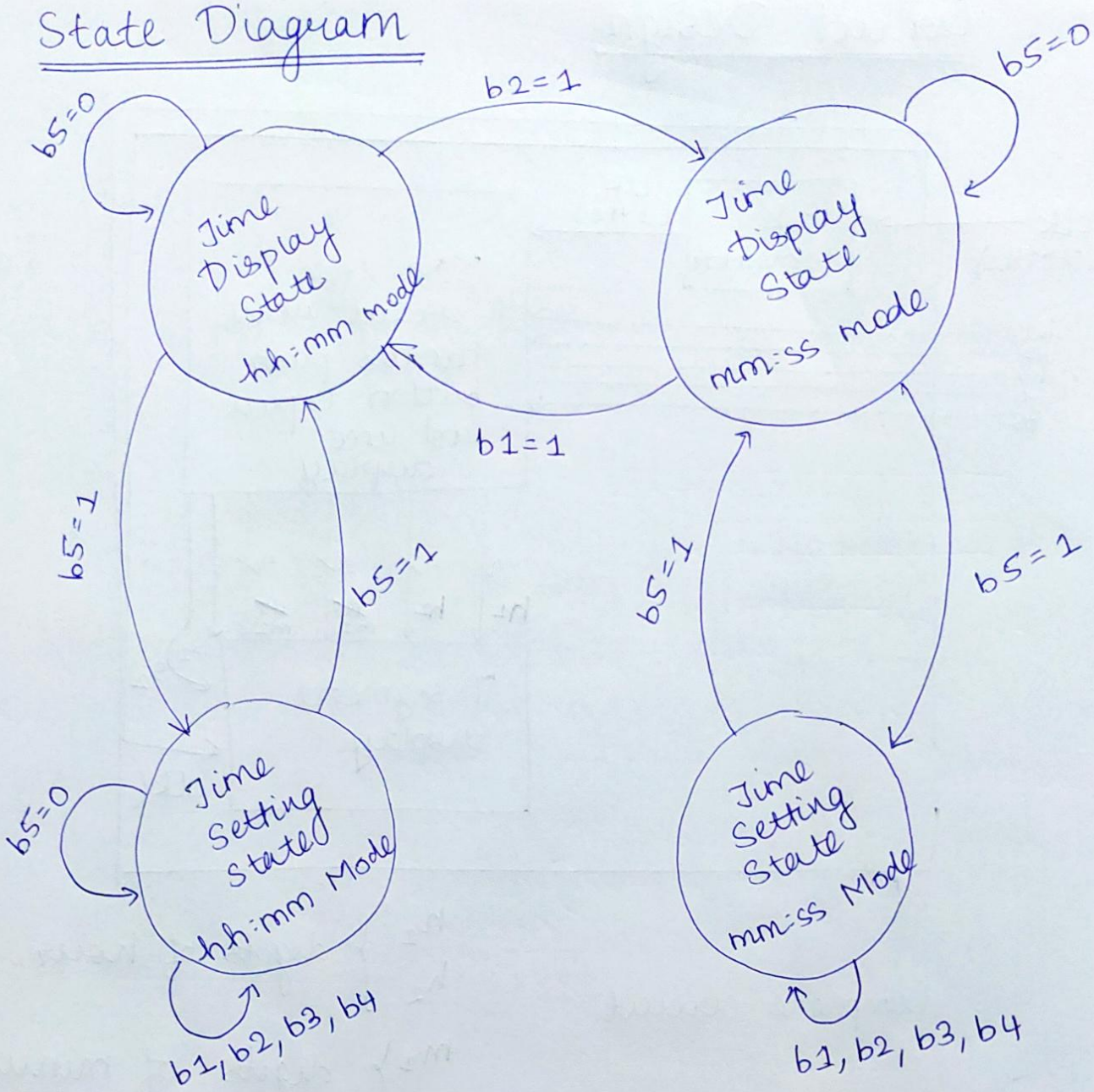
b1 → button for hh:mm display format
b2 → button for mm:ss display format
b3 → reset button (resets the clock to 00:00:00)

In time setting / time selecting mode,

b1 → up-counter button for digit d1
b2 → up-counter button for digit d2
b3 → up-counter button for digit d3
b4 → up-counter button for digit d4

The max count of these digits depends upon the format of display i.e. whether the digit represents hour, minute or second

State Diagram



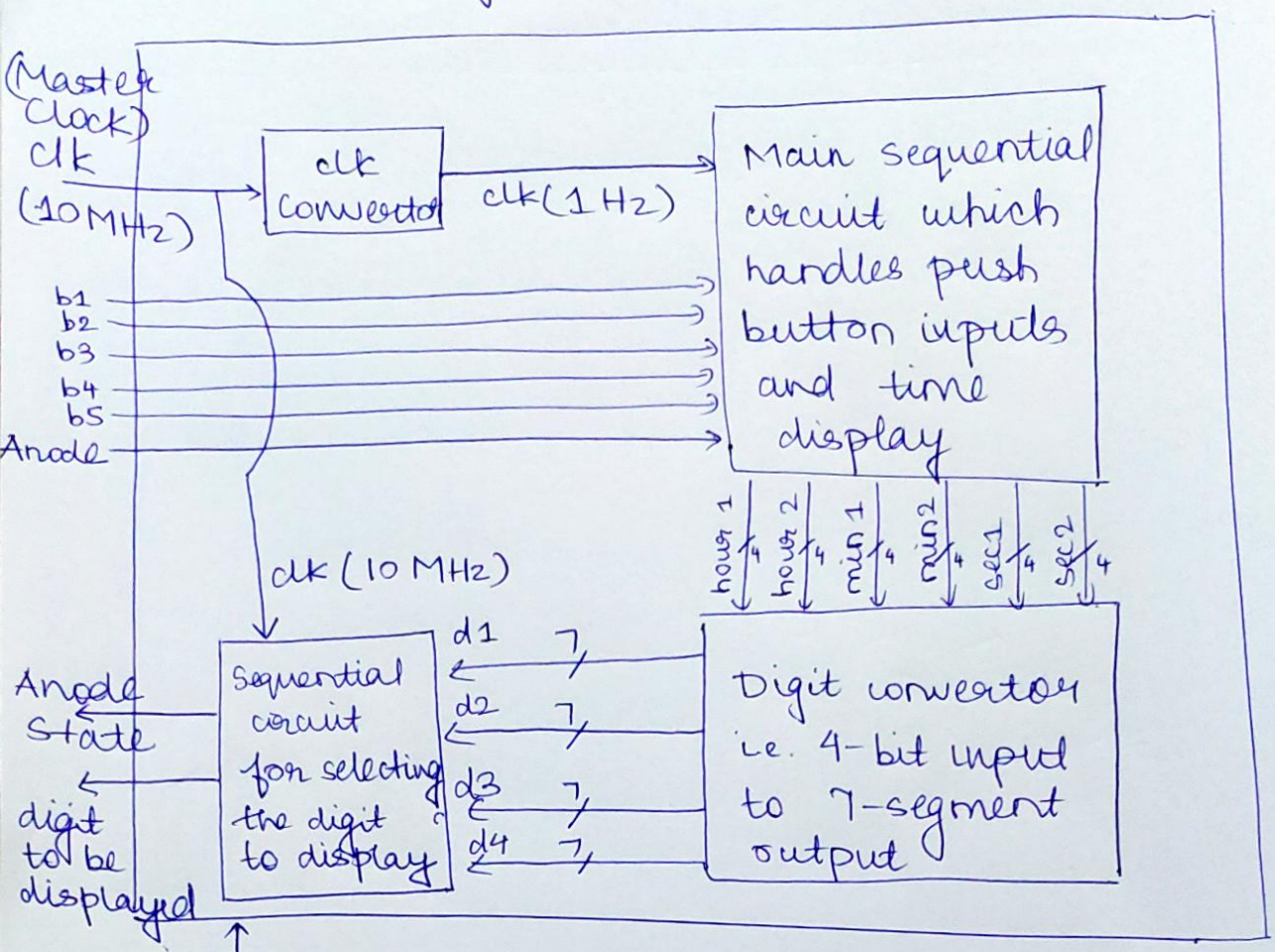
→ Note that **b5 is a toggle button**

→ Status of all buttons is checked at rising edge of master clock

→ But time is changed at rising edge of converted clock of frequency 1 Hz

→ b1, b2, b3, b4 are time setting buttons ~~for time~~ ~~d~~

Circuit Design



Complete circuit of digital clock

→ Note the final digit displayed as output has a refresh period of