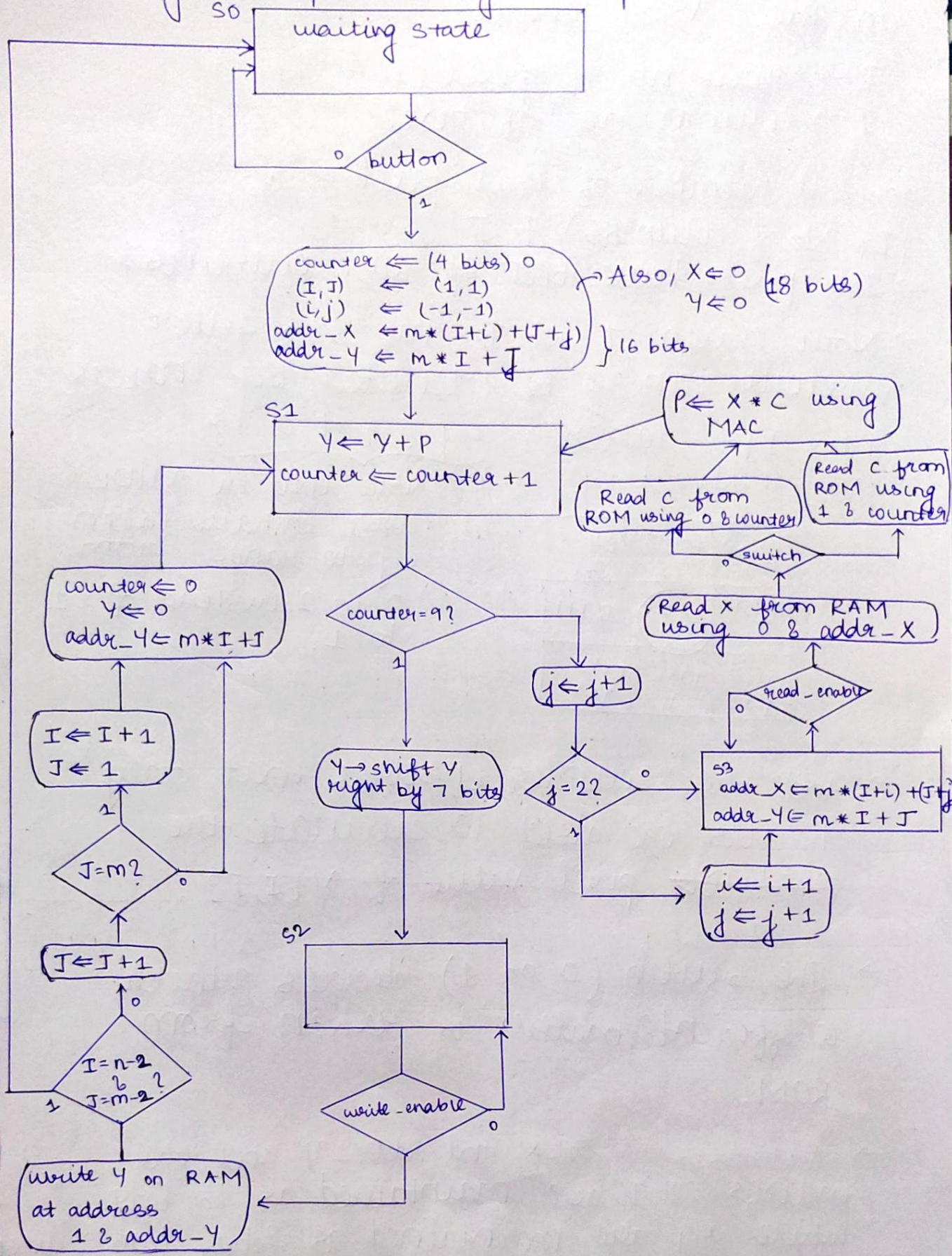
ASM chart for Central Block (2)

Assuming m×n pixel array as input



~~Note that~~

In the ASM chart,

I → row no. of pixel
J → column no. of pixel

So, cell number of that pixel =
(I * No. of columns) + J

→ The pixels have been stored row-wise

→ Now, given I and J, the 3×3 filter window can be denoted by indices I+i, J+j where $i, j \in \{-1, 0, 1\}$

Note that in VHDL code, I have taken i, j to range from 0 to 2 instead of -1 to 1.

I-1, J-1	I-1, J	I-1, J+1
I, J-1	(I, J)	I, J+1
I+1, J-1	I+1, J	I+1, J+1

→ And the counter ensures that only 9 cells are used to calculate the ~~product~~ pixel value of Y[I, J].

→ The switch (0 or 1) decides which co-efficient matrix is taken from ROM.

→ Addresses addr_x and addr_y and the indices I, J are maintained as 16 bits while i, j are maintained as 2 bits with 0-index