ASM chart for Central Block (2 Assuming mxn pixel array as input maiting state button counter (4 bits) 0 7 Also, X & 0 (18 bits) (I, J) (1, 1) (i,i) = (-1,-1) adds:  $X \leftarrow m*(I+i)+(J+j)$  | 16 bits addr-4 = m\*I+J PEX\*C using MAC Y= Y+P Read C from counter = counter +1 ROM using Read c from ROM using 0 & wunter, 1 & country switch counter = 0 read x from RAM using 0 8 adds-X 400 courter=97 addy\_4= m\*I+I j € j+1) gread - enable I ← I + 1 Y-shift Y J = 1 (j=22) adde X = m \*(I+i) +(J+i) right by 7 bits adde-4= m\*I+J J=m2 J=J+1) I=n-2 J=m-2 weite enable write 4 on RAM at address 1 & addr-4

Note that In the ASMI chart, I - nou no of pixel J-s wumn no of pixel So, cell number of that pixel = (I\* No. of columns) + J The pixels have been stored new-wish -> Now, guen I and I, the 3x3 fitter mindout can g be denoted by indices Iti, Itj mhere ijt 1-1,0,13 Note that in VHOL code, I have taken i, j to range from I-1, I-1, I-1, J+1

I,J-1 (I,J) I,J+1 0 to 2 inestead of -1 - And the counter ensures that only

- q cells one used to calculate the product pixel value of Y[I,I].
- → The suitch (0 or 1) decides ruhich w-efficient matrix is taken from ROM.
- -> Addresses addr-x and addr-y and the indices I, I ame maintained as 16 bits while i, i are maintained as 2 bits with o-indes