

CMS pixel module test procedures

*A. Starodumov,
IPP, ETH Zurich*

Silicon Detector Workshop
Split, Croatia, October 8-10, 2012

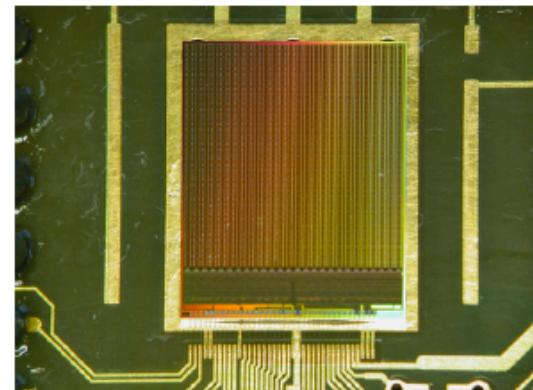
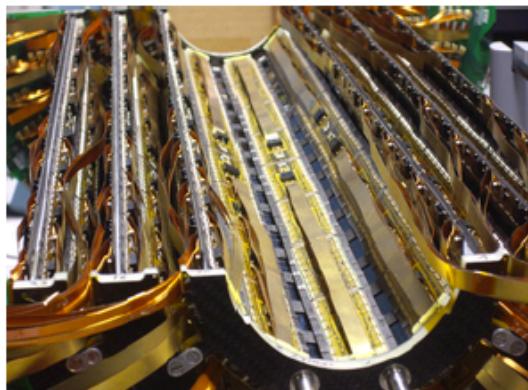
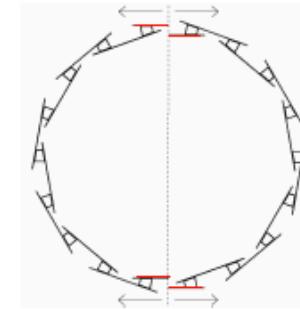
Outline

- PSI46 analog readout chip
- Initial DAC optimization
- Tests procedures of the analog ROC
- Tests of the digital ROC
- Construction of the present CMS pixel barrel detector

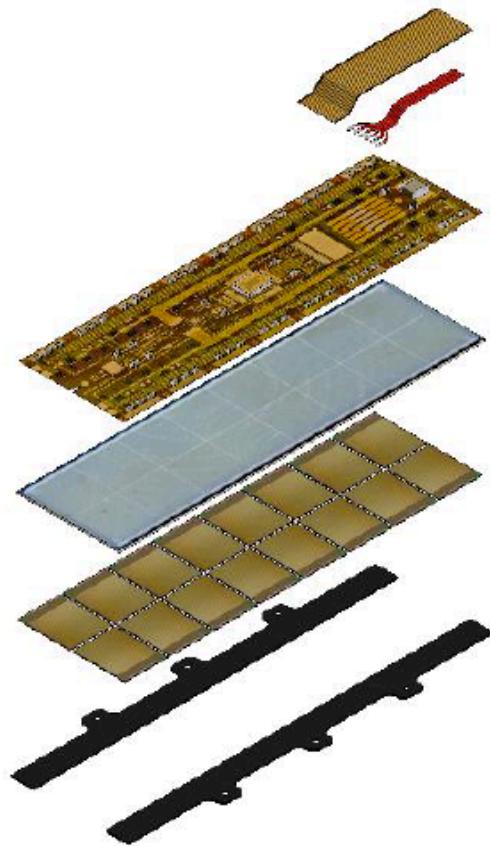
*Slides used in the presentation from:
H.-Ch. Kaestli, S. Streuli, B. Meier, Ph. Eller,
F. Bahmair, M. Rossini, P. Trueb, Ch. Eggel,
S. Dambach*

CMS barrel pixel detector

- ▶ Barrel pixel detector is built of 768 modules:
 - ▶ full modules (16 ROCs): $672 = 128 + 224 + 320$
 - ▶ half modules (8 ROCs): $96 = 3 \times 32$
- ▶ Read Out Chip:
 - ▶ Each ROC is segmented in 4160 pixels
 - ▶ Pixels in a ROC organized in 26 double columns (z) and 80 rows ($r - \phi$)
 - ▶ Pixel size: 100μ in $r - \phi$ and 150μ in z
 - ▶ 29 DACs are used to tune a ROC



Break-up of analog module



Cables:
signal&power

HDI print

Si sensor

16 ROCs

Base strips:
 Si_3N_4

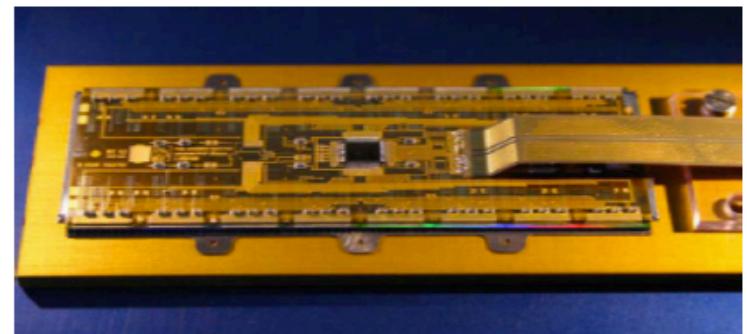
Module parameters:

Size: 66.6 mm × 26 mm

Weight: 3.5 g

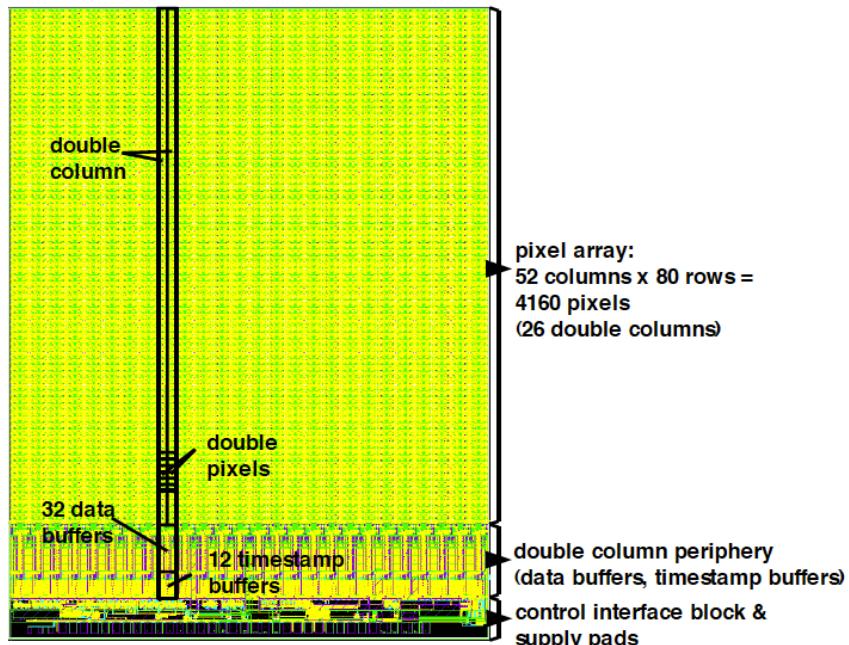
Segmentation: 66560 pixels

Si sensor thickness: 285μ

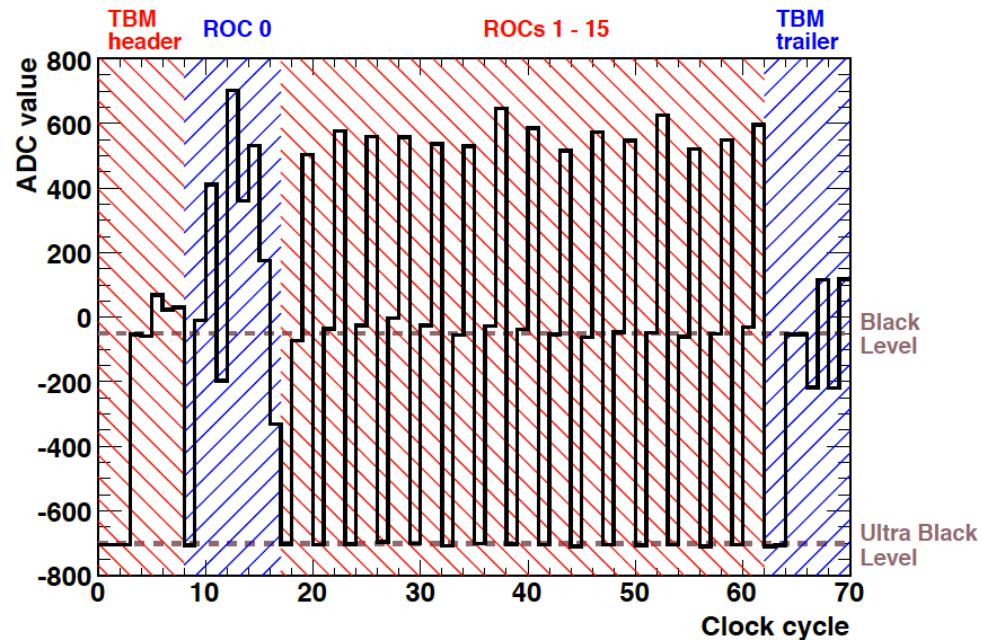


PSI46 pixel chip

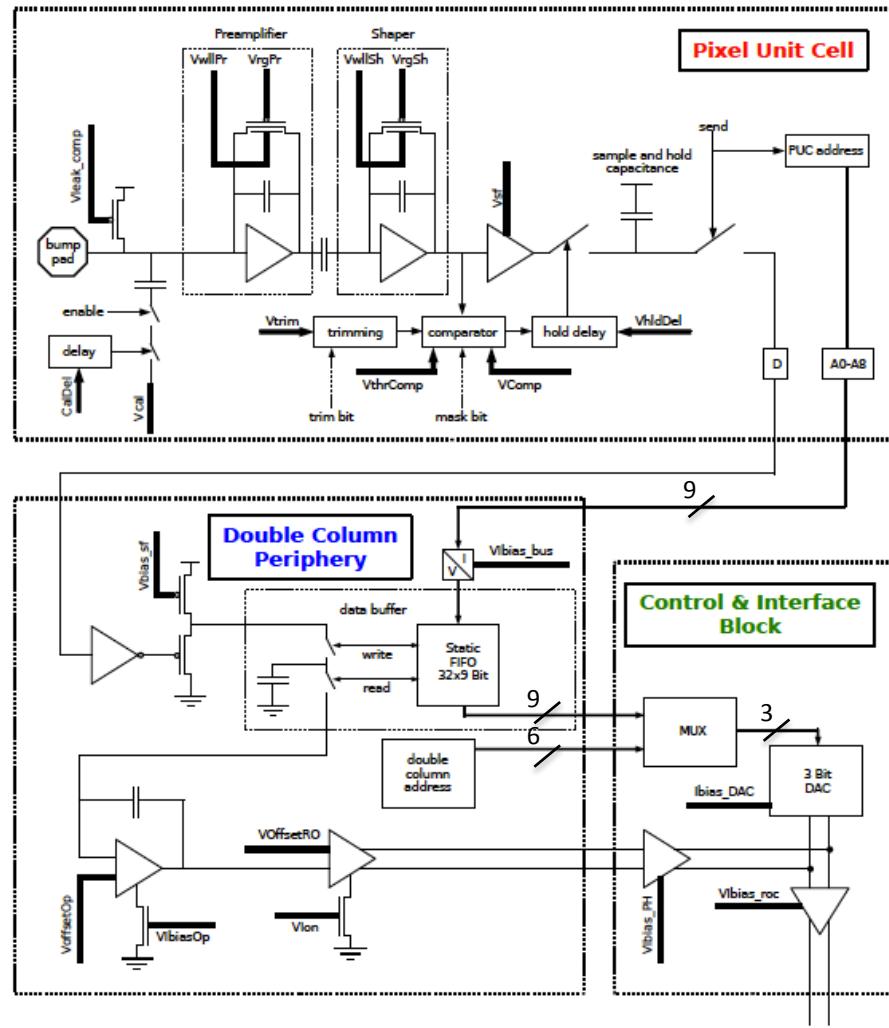
Layout



Module readout



Schematic view of the readout chain



ROC is divided in two parts:

- Active area: one PUC per sensor pixel; the active area is organized in 26 double-columns and 80 rows
 - Periphery: control interfaces and data buffers to store the hit information

Behavior of the ROC controlled by

- 26 DACs (digital to analog converters)
 - and 3 registers:
 - ✓ *CtrlReg*: switches between high and low Vcal range, full speed (40 MHz) and half speed and to disable a whole ROC.
 - ✓ *WBC* sets the bunch crossing in which data is read out
 - ✓ *RangeTemp*: switches between different ranges of the ROC internal temperature sensor

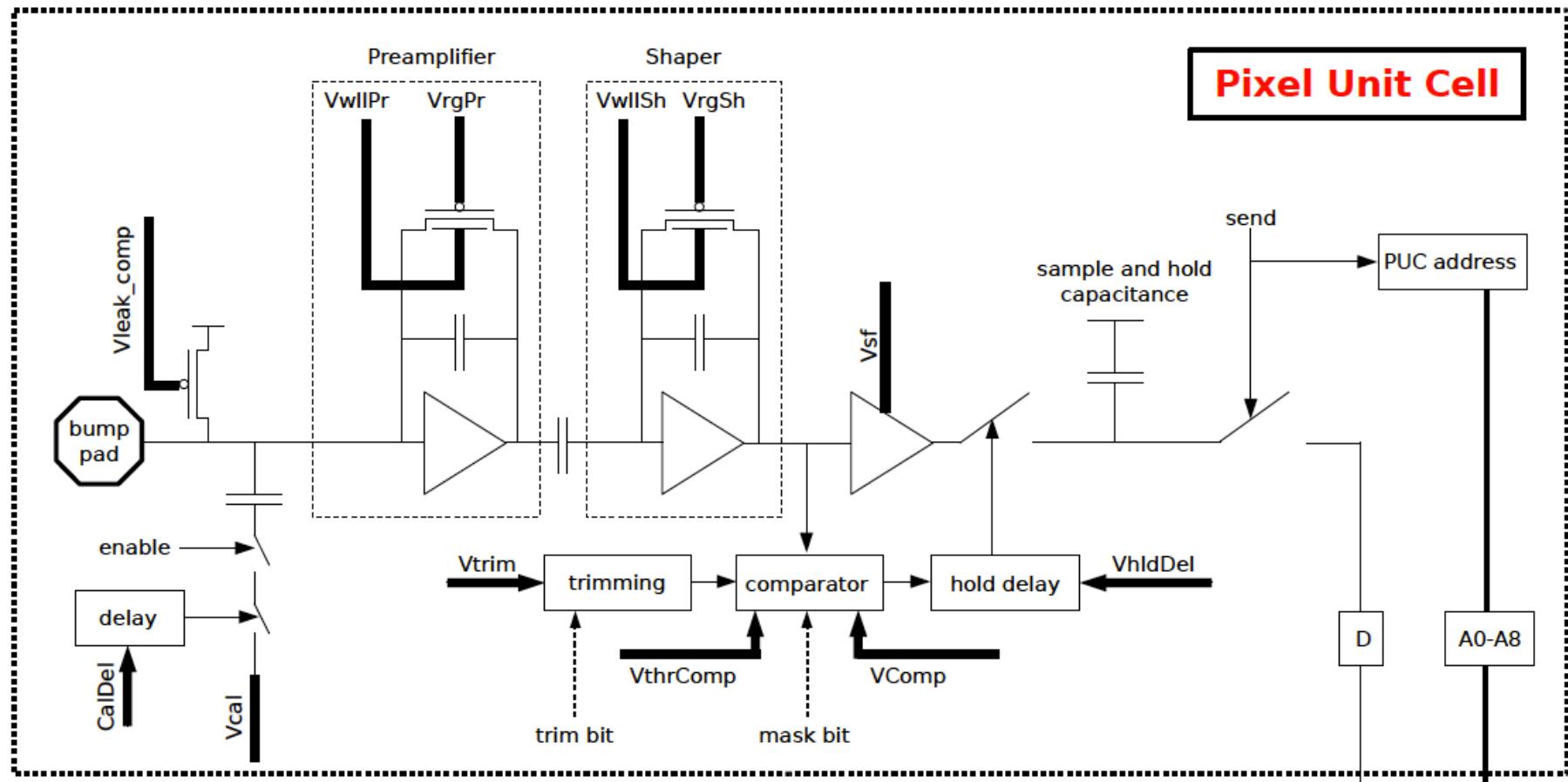
ROC DACs and registers

Name	addr	unit	# bits	Min Value	Max Value	Recomm. DAC Value	Keyword
Voltage Regulators							
Vdd	1	mV	4	1700	2100	6	Voltage regulator
Vana	2	mV	8	800	1300	140	Voltage regulator
Vsf	3	mV	8	1000	2100	255	Voltage regulator
Vcomp	4	mV	4	1800	2100	15	Voltage regulator
Analog PUC							
Vleak	5	mV	8	-700	0	0	Sensor leakage current compensation
VrgPr	6	mV	4	0	500	0	Preamplifier feedback
VwlIPr	7	mV	8	500	1300	35	Preamplifier feedback
VrgSh	8	mV	4	0	500	0	Shaper feedback
VwlISh	9	mV	8	500	1300	35	Shaper feedback
VHldDel	10	mV	8	-1500	-500	117	Hold delay
Vtrim	11	mV	8	-710	-400	29	Pixel trimming
VcThr	12	mV	8	-1500	-600	60	Comparator threshold
Pixel Readout							
Vlbias_bus	13	µA	8	0	12	30	
Vlbias_sf	14	µA	4	0	50	6	Source follower

ROC DACs and registers, cont.

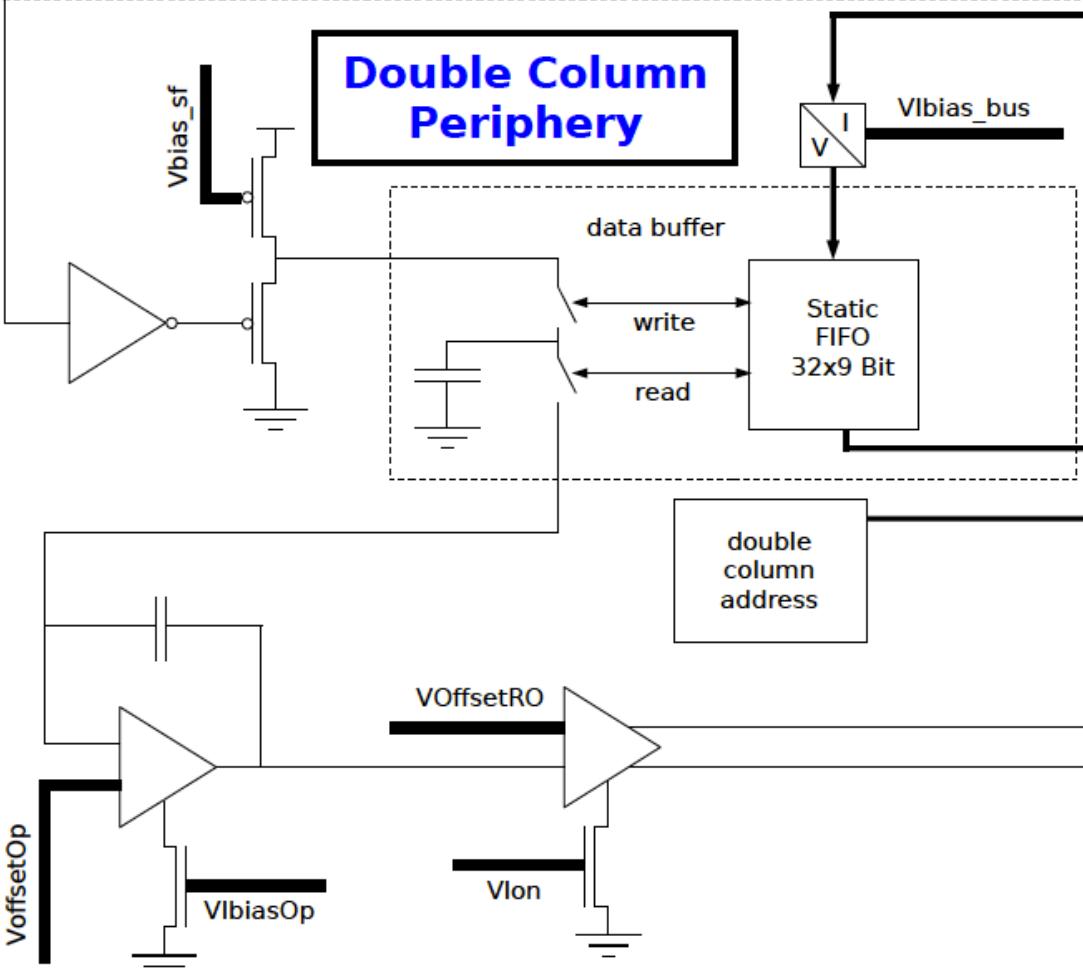
Double Column Readout							
VOffsetOp	15	mV	8	1000	1500	90	
VbiasOp	16	µA	8	0	20	115	
VOffsetRO	17	mV	8	1000	1500	76	
Vlon	18	µA	8	0	100	115	
Chip Readout							
Vlbias_PH	19	µA	8	0	30	100	Pulse height
Vlbias_DAC	20	µA	8	0	20	160	Pixel address range
Vlbias_roc	21	µA	8	0	30	150	Adjust single ended output level
Multiplicity Trigger							
VIColOr	22	µA	8	0	200	99	
Vnpix	23	µA	8	0	70	0	
VsumCol	24	µA	8	0	150	0	
Others							
Vcal	25	mV	8	0	260/1800	150	Calibrate pulse height, see also section 5.3.5
CalDel	26	nsec	8	55	205		See chapter 7
WBC	254	clocks	8	0	255	>70	Trigger latency
Chip Control Register	253		8				See section 5.3.5

Pixel Unit Cell



Adjustable DACs: $CalDel$, $VthrComp$, $Vtrim$, Vsf

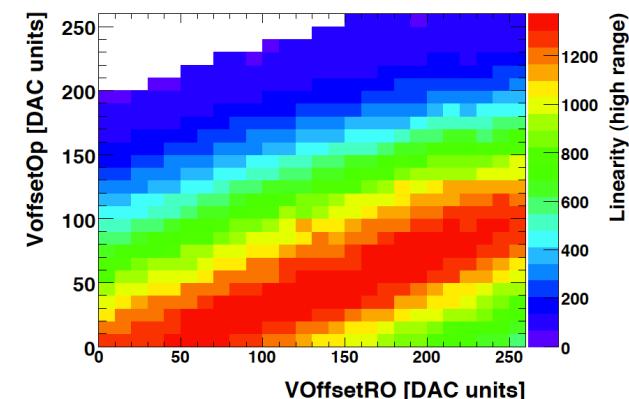
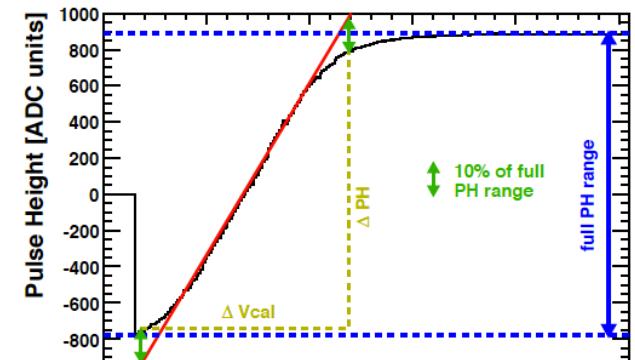
Double column periphery



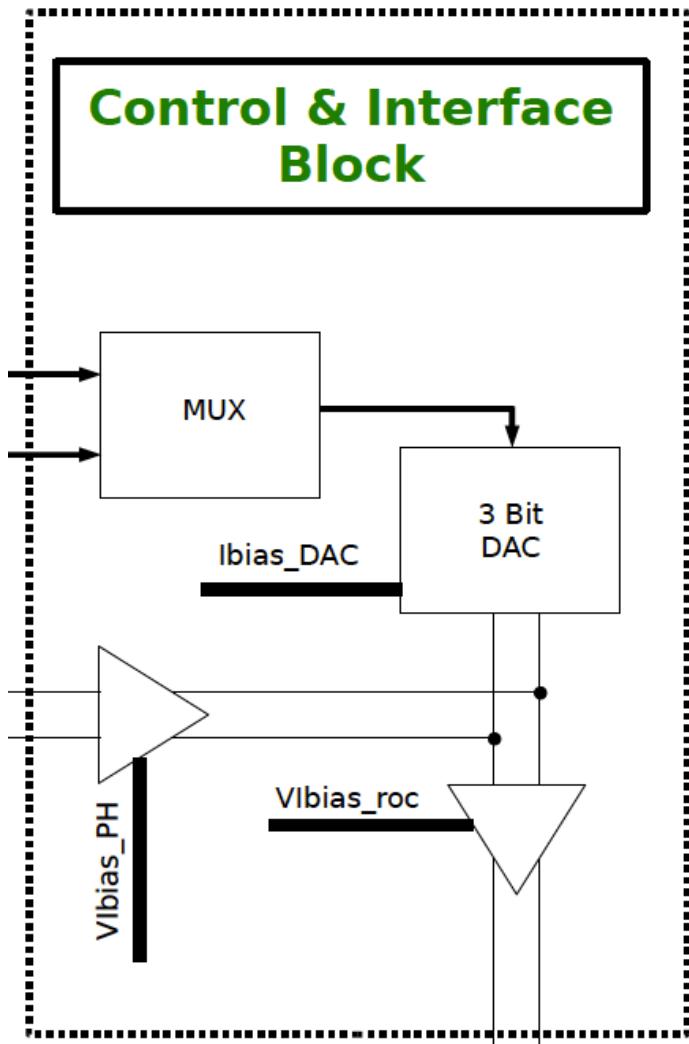
Adjustable DACs:

$V_{offsetOp}$, $V_{offsetRO}(=120)$

These DACs shift the pulse height curve and have an influence on the linear range.



Control and Interface Block



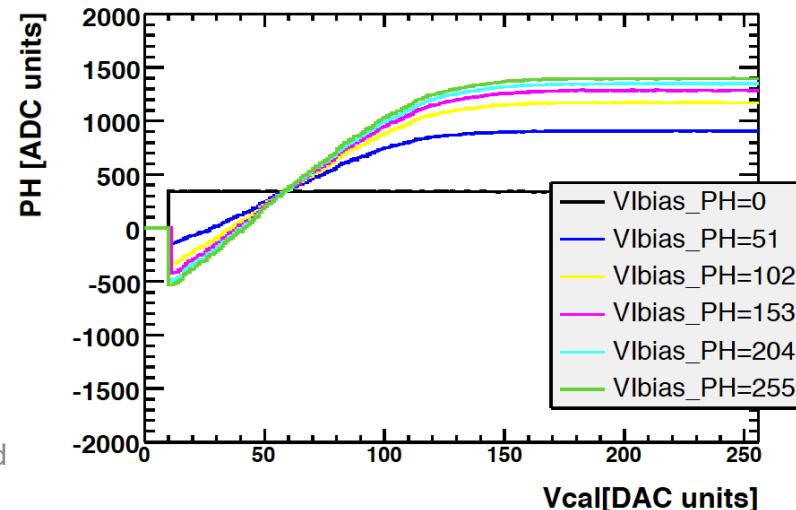
08/10/2012

Adjustable DAC:

Ibias_DAC, Vibias_PH

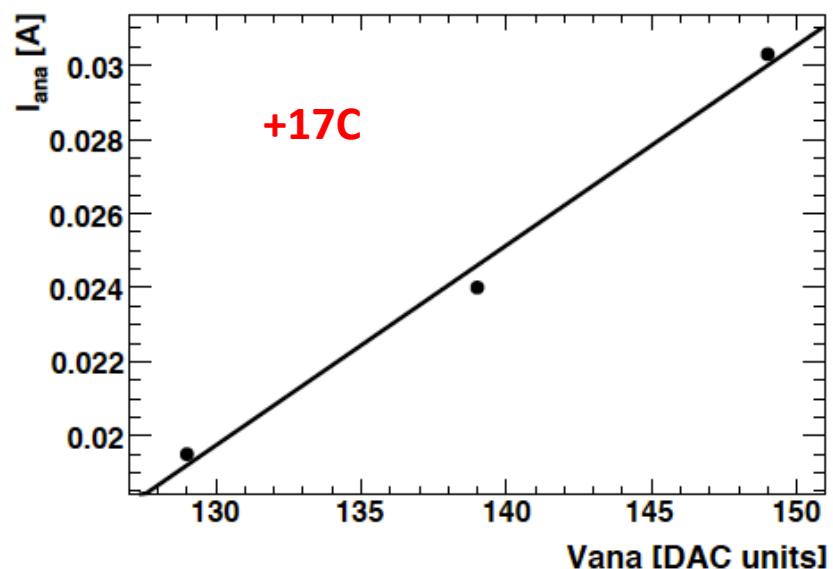
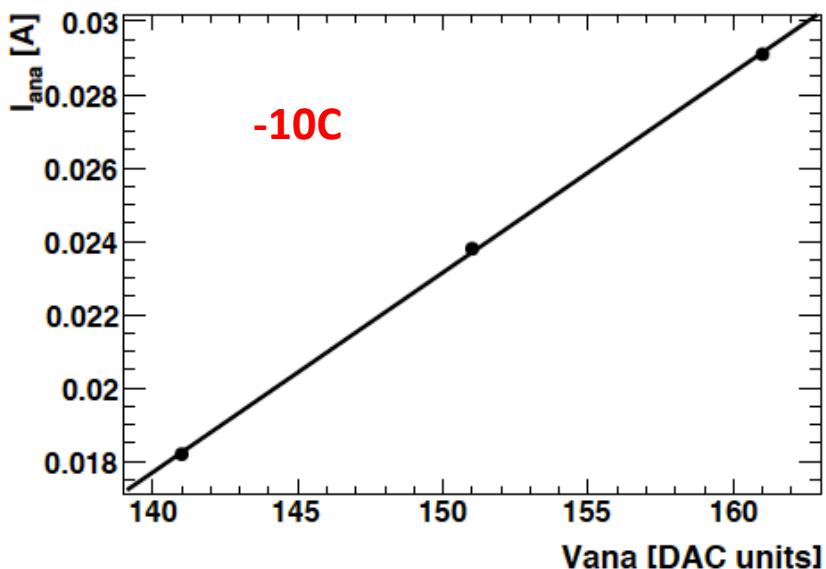
Ibias_DAC used to set the ultrablack of all ROCs to the same value as the TBM ultrablack. In the same way as for the TBM this also fixes the position of the ROC address levels.

Vbias_PH used to stretch/squeeze pulse height curve to fit in desirable range.



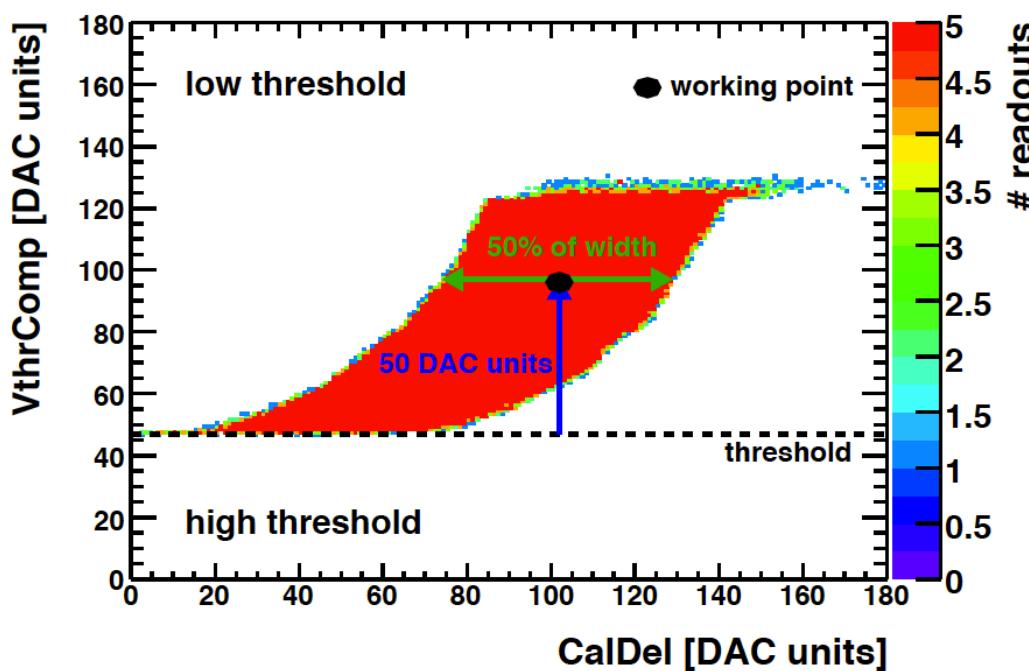
Vana DAC setting

- The first DAC to be set is *Vana* which defines the analog current of a ROC
- All other optimized DAC values depend on analog current, hence to have reproducible results one should set always the same analog current
- In the previous module testing campaign the analog current set to 24mA per ROC



VthrComp vs CalDel

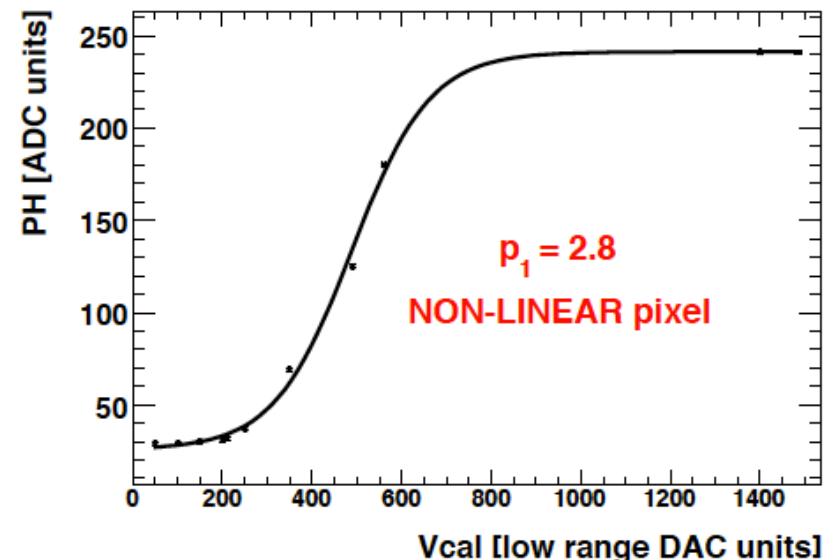
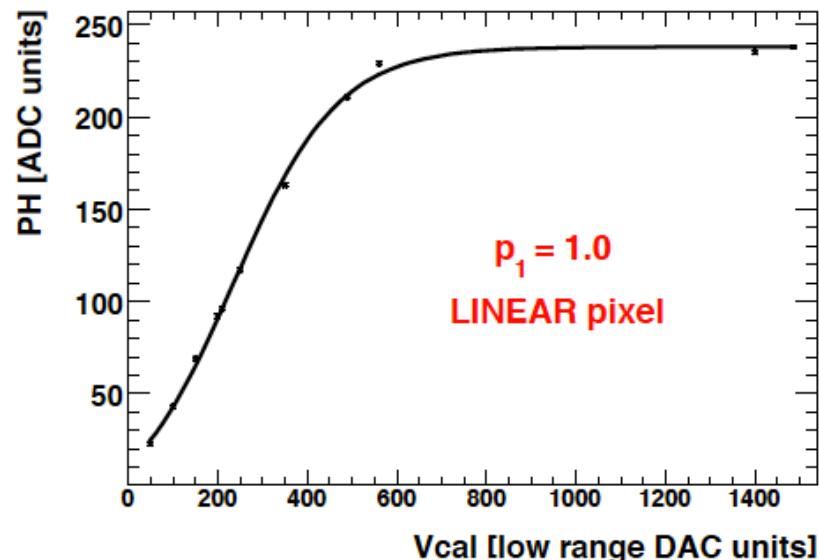
- For fixed V_{cal} DAC value (strength of internal calibrate signal) ROC works in a certain region of $V_{thrComp}$ - $CalDel$ DAC values
- To perform further ROC tests one has to find a stable working point



- Since variation between pixels in a ROC relatively small, the working point found for one pixel is valid also for all other pixels in the same ROC
- Algorithm: for each point in $V_{thrComp}$ - $CalDel$ plane, five internal calibrate signals sent and readout
- Working point selection shown on the figure

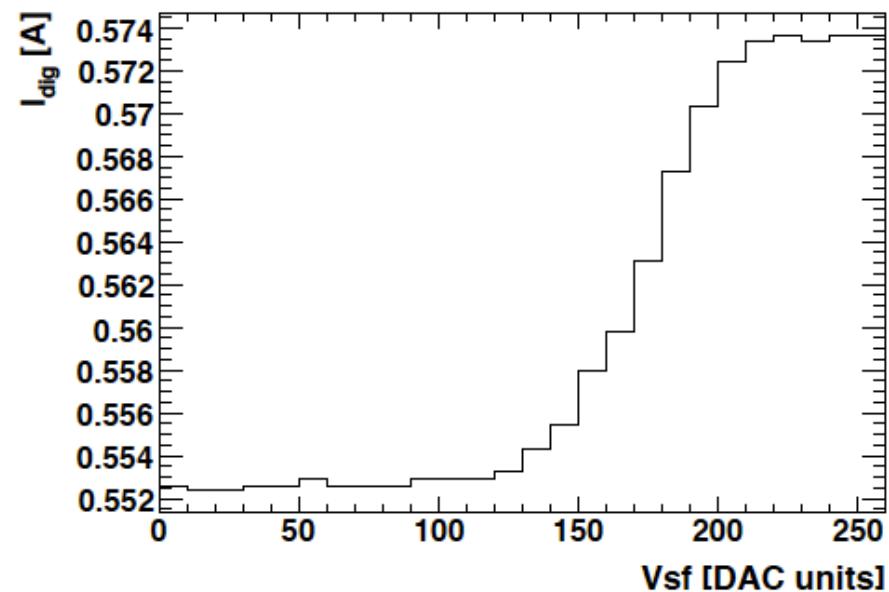
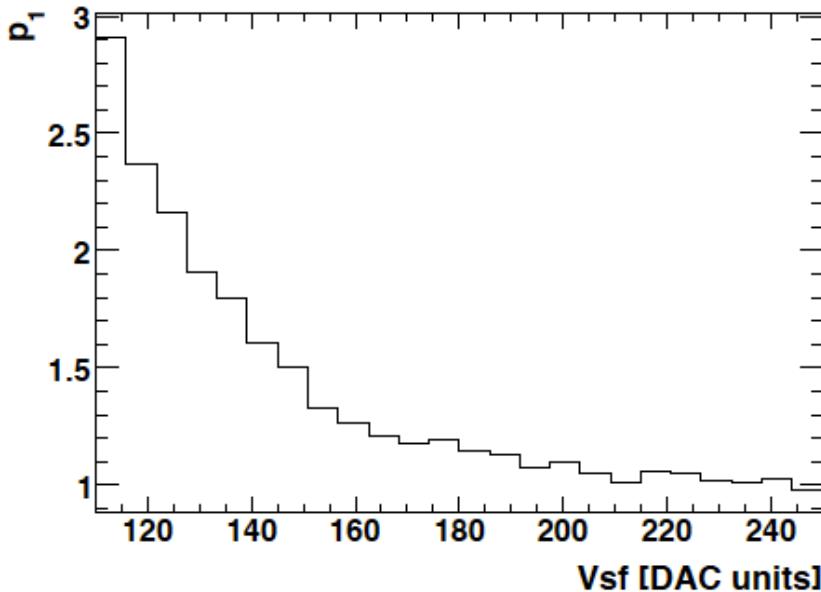
Pulse Height linearity

- Charge deposited in Si sensor and collected by PUC is measured in ADC units (PH)
- To convert charged measured in PH one needs to make two calibrations:
 - ✓ Convert PH into V_{cal} units: so-called **gain calibration** (see later)
 - ✓ and calibrate V_{cal} units to charge in electrons: **V_{cal} X-ray calibration** (see later)
- PH vs V_{cal} curve may be not linear in the low V_{cal} range (small charges)
- PH iv V_{cal} curve fitted with $y = p_3 + p_2 \cdot \tanh(p_0 \cdot x - p_1)$ and p_1 is tuned to 1 using V_{sf} DAC



Vsf DAC optimization

- *Vsf* DAC value influences the linearity of gain curve
- Higher the *Vsf* DAC value more linear is the curve but at certain value the digital current increase dramatically, that increases the power consumption of a ROC
- Optimization algorithm:
 - increases *Vsf* DAC in steps of 5 units
 - check I_{dig} and check p_1 value: until $p_1 < 1.4$ or $I_{dig}(Vsf) - I_{dig}(Vsf=0) = 5\text{mA}$

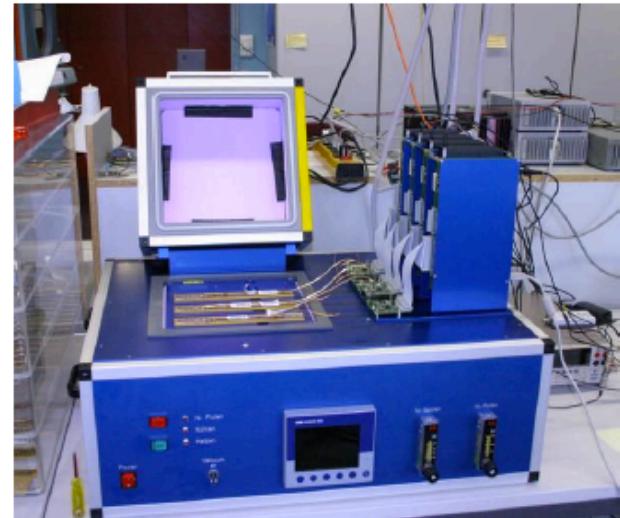


Module test classification

- Start-up adjustment
 - ✓ analog current setting: tune V_{ana} DAC for $I_{ana}=24\text{mA}$
 - ✓ threshold and delay settings: tune V_{thrCom} vs $CalDel$ DACs
 - ✓ DACs optimization
- Functionality tests
 - ✓ verification pixel readout: dead, noisy pixels, mask defects
 - ✓ address decoding: find separation between the analog levels
 - ✓ bump bonding quality test: verify connections between ROC and Si sensor
 - ✓ trim bits test: check functionality of 4 trim bits for each pixel
- Performance tests
 - ✓ noise measurements: check noise for each pixel
 - ✓ leakage current measurements of Si sensor: IV curve
- Calibrations
 - ✓ pulse height calibration: PH(ADC) vs V_{cal} DAC
 - ✓ trimming: all pixels threshold unification (V_{thrCom} , V_{trim} DACs, trim bits)
 - ✓ internal calibrate signal calibration (V_{cal} DAC) with X-rays

Testing setup

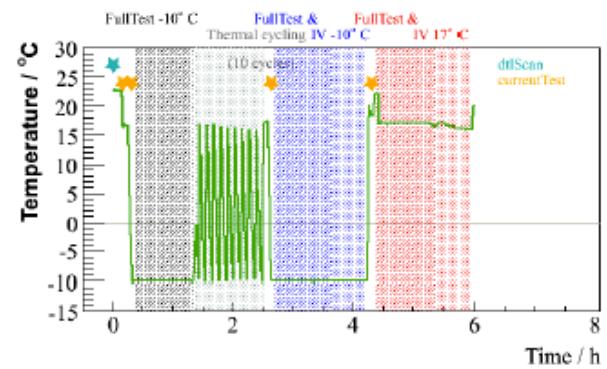
- ▶ A desktop PC with Linux operating system
- ▶ Four electronics test-boards, especially designed to test the barrel pixel modules
- ▶ Four module adaptor boards to connect the modules to the test-board
- ▶ A cool box with space for four modules to keep the modules at constant temperature (+20°C – -20°C) and humidity (<20%)
- ▶ A Keithley 2410 source meter:
 - ▶ supply voltage up to 1100 V
 - ▶ current measurements 1pA – 1A



Framework and procedures

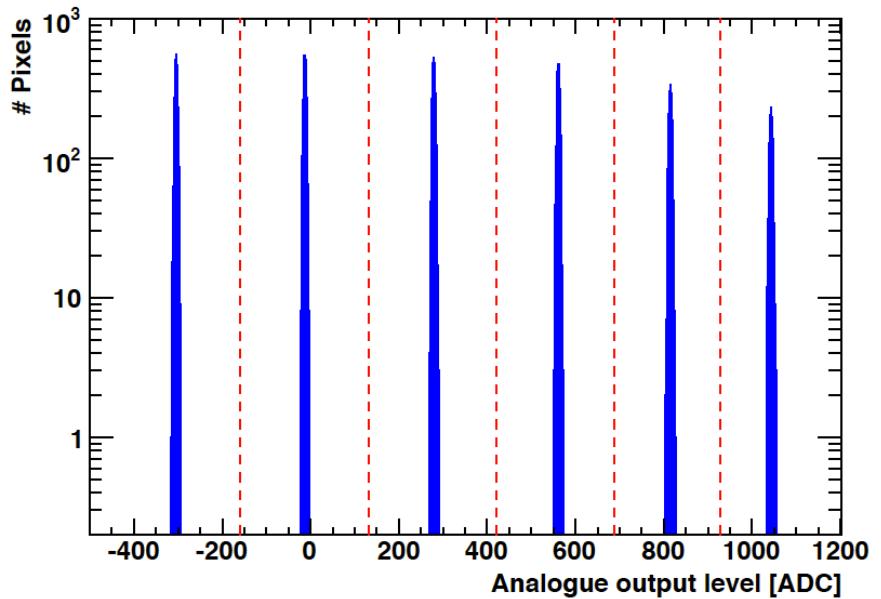
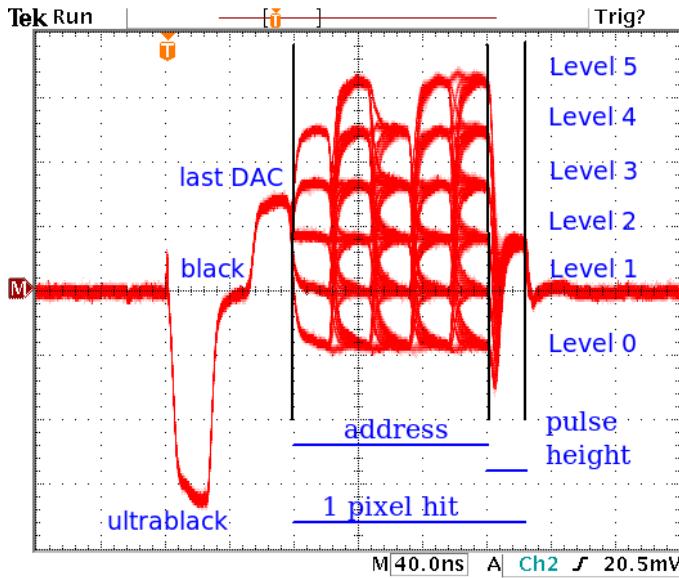
- ▶ Software framework
 - ▶ test algorithms are implemented in C++ software package *psi46expert*
 - ▶ data storage and analysis is done in ROOT framework
 - ▶ tests, analysis and grading are automated with help of Perl scripts
 - ▶ part of test algorithms run directly on test board (FPGA)
- ▶ Test procedure
 - ▶ start-up DAC adjustments and Full Test at -10°C
 - ▶ 10 thermal cycles performed between +17°C and -10°C
 - ▶ Full Test at and I-V measurements at -10°C
 - ▶ Full Test at and I-V measurements at +17°C
 - ▶ run analysis script and transfer results on web-based 'DB' (see later)

Test duration per ROC [s]	PC based code	FPGA based code
Trim Bits Test	145	26
Bump Bonding Test	80	20
Noise Measurements	210	89
Trimming	450	156
Pulse Height Calibration	245	20



Address levels calibration

- Pixel address consists of 5 clock cycles: 2 for double-column index (26) and 3 for the pixel index within a double-column (160)
- Each clock cycle can take 6 different levels, that should be well separated
- Algorithm:
 - ✓ the levels of all pixels in a ROC are measured and overlaid in a histogram
 - ✓ search for separated peaks (exactly 6) and find centers between neighboring peaks
- Test each pixel with a calibrate signal and decode the address



Address level indexes

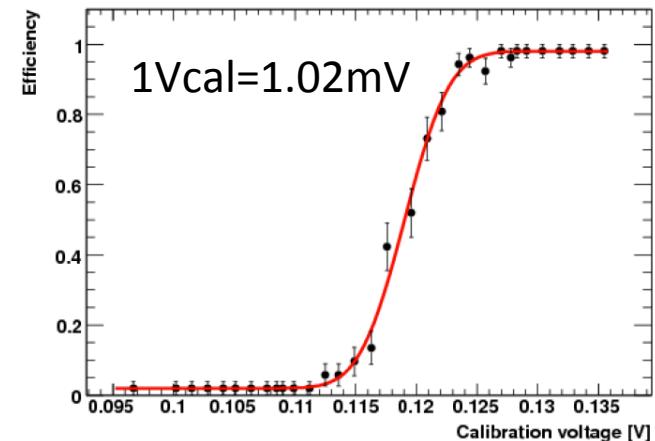
DCOL	Address Levels
0	0 0
1	0 1
2	0 2
3	0 3
4	0 4
5	0 5
6	1 0
7	1 1
8	1 2
9	1 3
10	1 4
11	1 5
12	2 0
13	2 1
14	2 2
15	2 3

Pixel	Address level		Pixel	Address level	
	Left	Right		Left	Right
0	4 2 4	4 2 5	40	2 1 2	2 1 3
1	4 2 2	4 2 3	41	2 1 0	2 1 1
2	4 2 0	4 2 1	42	2 0 4	2 0 5
3	4 1 4	4 1 5	43	2 0 2	2 0 3
4	4 1 2	4 1 3	44	2 0 0	2 0 1
5	4 1 0	4 1 1	45	1 5 4	1 5 5
6	4 0 4	4 0 5	46	1 5 2	1 5 3
7	4 0 2	4 0 3	47	1 5 0	1 5 1
8	4 0 0	4 0 1	48	1 4 4	1 4 5
9	3 5 4	3 5 5	49	1 4 2	1 4 3
10	3 5 2	3 5 3	50	1 4 0	1 4 1
11	3 5 0	3 5 1	51	1 3 4	1 3 5
12	3 4 4	3 4 5	52	1 3 2	1 3 3

Definitions

➤ Generate and read out hit in pixel: “readout the pixel” procedure

- ✓ Enable the double-column of the corresponding pixel
- ✓ Enable the calibration injection to the pixel
- ✓ Enable the readout of the pixel
- ✓ Send a calibration signal to the module
- ✓ Send a trigger signal to the module



➤ Threshold definitions:

- ✓ **Vcal-threshold:** The threshold of the comparator set to a fixed $V_{thrComp}$. The response efficiency measured for increasing V_{cal} . The threshold given by the V_{cal} at which the efficiency reaches 50%.
- ✓ **VthrComp-threshold:** Calibration signal injected with constant V_{cal} . The response efficiency measured for decreasing $V_{thrComp}$ and the threshold determined by the $V_{thrComp}$ at which the efficiency reaches 50%.
- ✓ **In-time threshold:** The previously described thresholds are usually determined by searching for hits in a fixed bunch-crossing and are therefore referred to as in-time thresholds.
- ✓ **Timing independent threshold:** threshold at a given value of V_{cal} defined as the minimum of thresholds measured for different bunch-crossings.

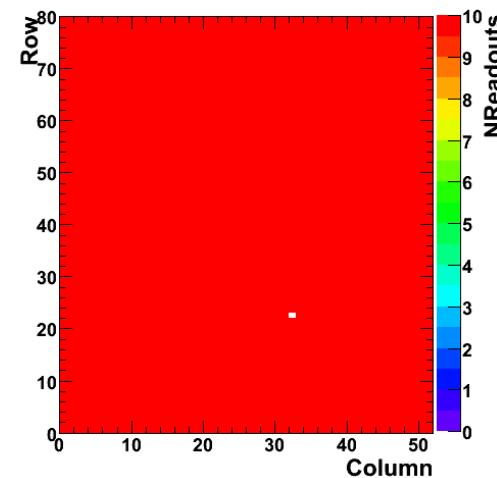
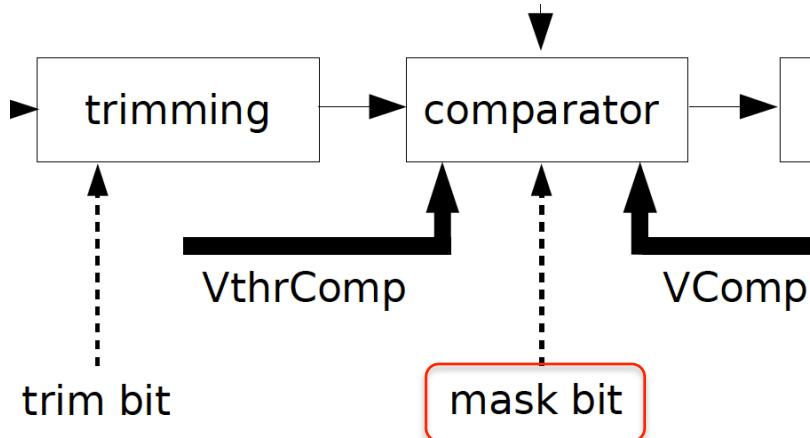
Pixel readout test

➤ Mask bit check (mechanism that disables a single pixel)

- ✓ noisy pixel can prevent a whole double-column from working properly by filling up the buffers in the double-column periphery
- ✓ mask mechanism is checked by enabling the mask bit and trying to read out the pixel
- ✓ if a hit is generated, the mask bit is defective (4 modules out of 1200)

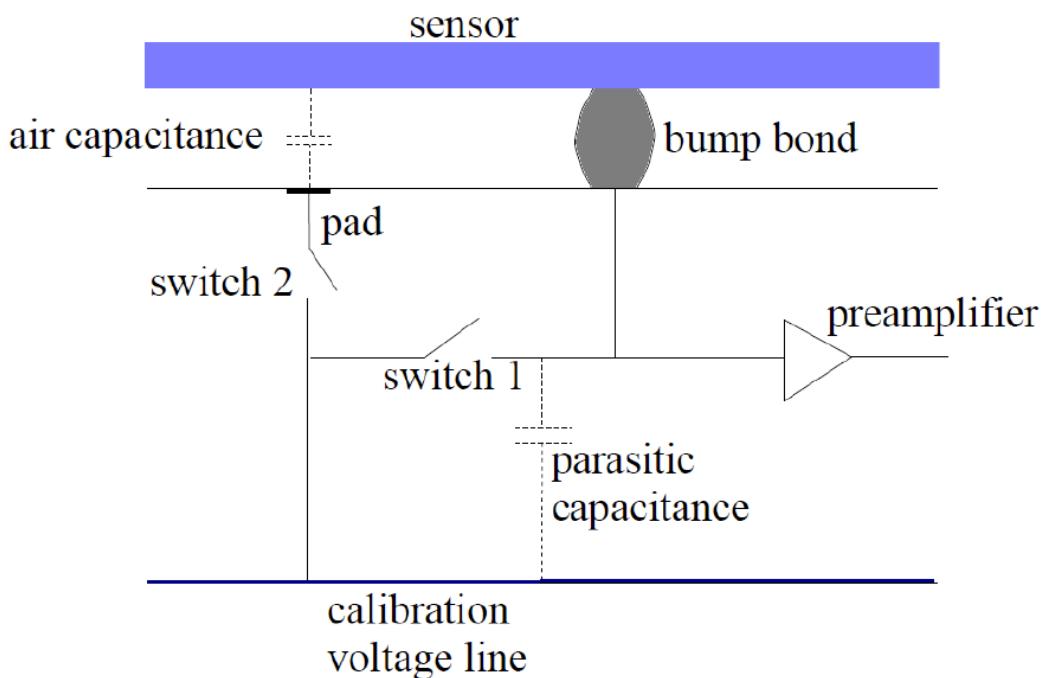
➤ Pixel readout test

- ✓ verifies that sending a calibration pulse to the enabled pixel, results in the corresponding hit information in the analogue signal
- ✓ 10 calibrate signals sent to each pixel, if less than 10 readout received – pixel ‘dead’



Bump bonding test

- Bump bonding test by design
 - ✓ induce calibrate signal (CtrlReg=4) via Si sensor
 - ✓ If no pixel readout – bump bond is missing
- The method does not work for analog ROC due to cross-talk between calibration line and preamplifier

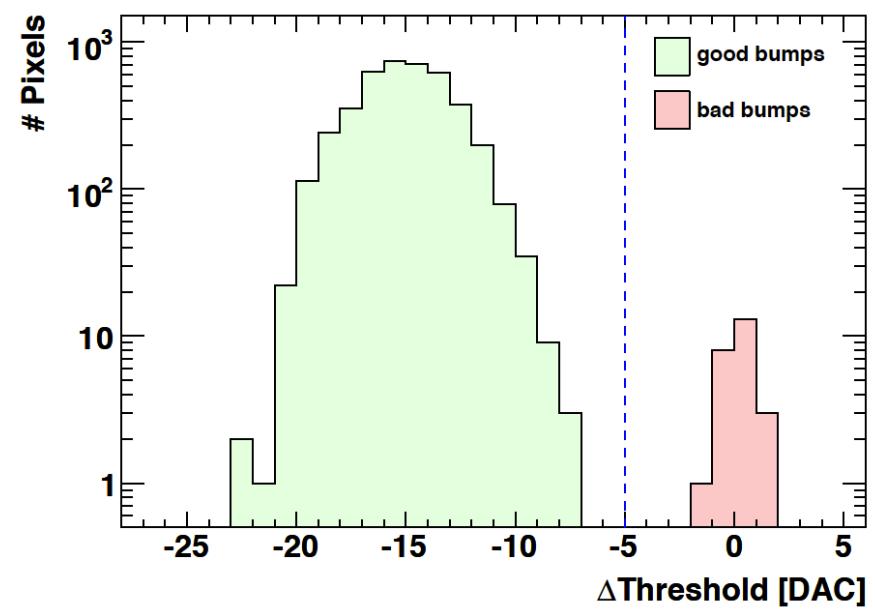
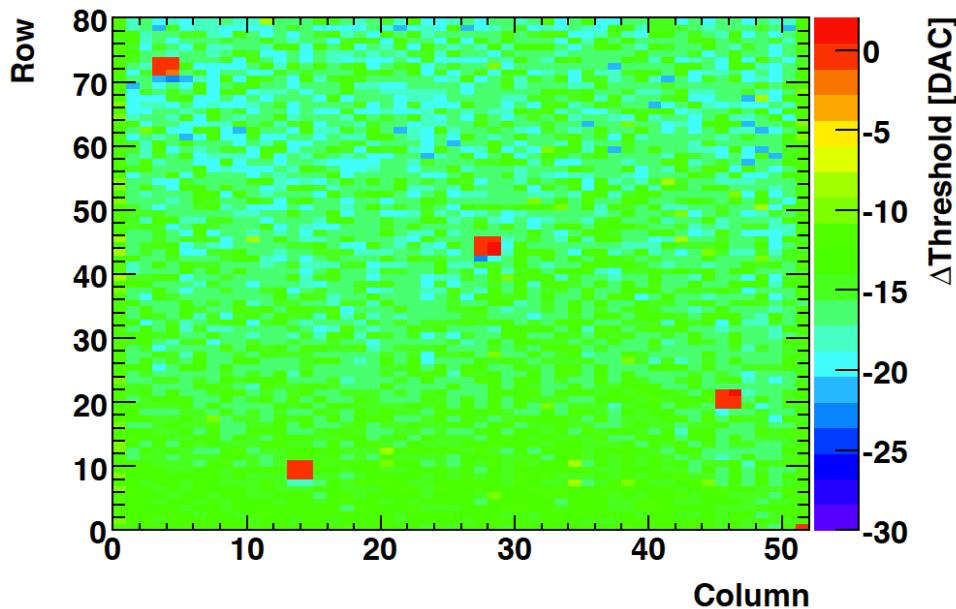


**1. Measurement of 'sensor' threshold:
switch 1 open and 2 closed**

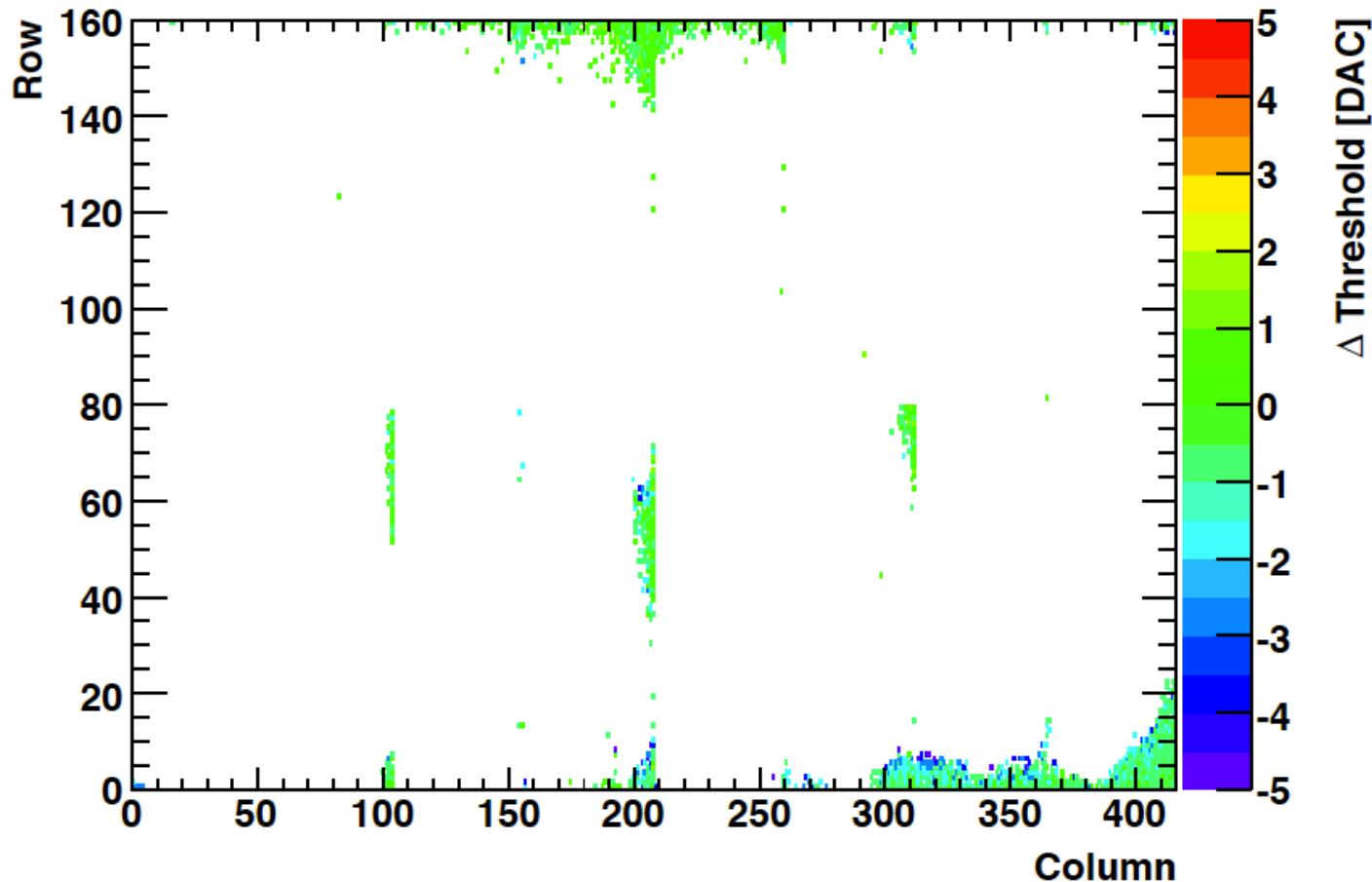
**2. Measurement of cross-talk threshold:
both switches are open**

Bump bonding test, cont.

- Developed method that uses cross-talk feature
 - ✓ set comparator threshold to high value (low $VthrComp$)
 - ✓ measure $Vcal$ -threshold with switch 1 closed and switch 2 open (sensor threshold)
 - ✓ measure $Vcal$ -threshold with both switches 2 open (cross-talk threshold)
 - ✓ make difference of both thresholds for each pixel (better separation with high comparator threshold)



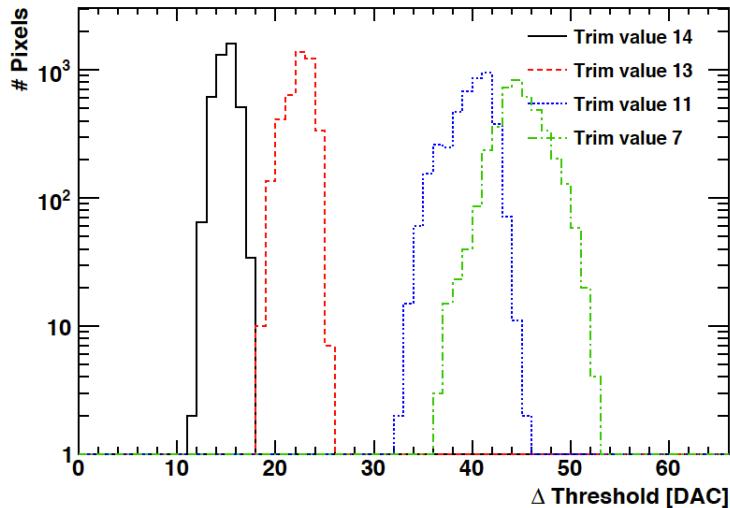
Bump bonding test, cont.



Bump bonding map of the module M0086 with many defects in the corners and along the ROC boundaries. The colored points represent pixels with bad bump bond connections

Trim bits test

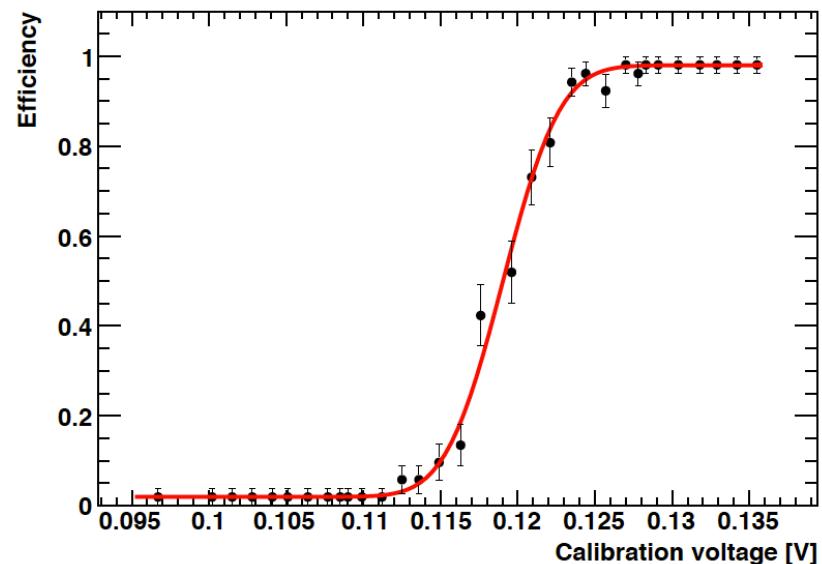
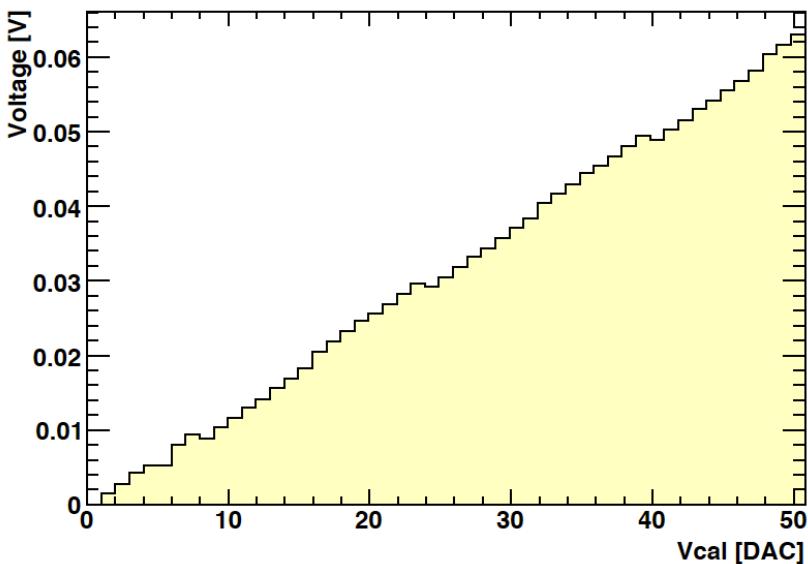
- Each pixel has 4 trim bits to adjust threshold individually ($VthrComp$ is set per ROC)
- By setting them appropriately pixel threshold is **lowered** by an amount depending on the $Vtrim$ DAC value
- Default untrimmed state: all trim bits enabled, the corresponding trim value 15
- Trim bit test algorithm:
 - ✓ measure pixel threshold in untrimmed state
 - ✓ measure pixel threshold with one trim bit at a time disabled
 - ✓ make difference of untrimmed and trimmed thresholds for each pixel
 - ✓ if the threshold difference less than 2 DAC units, the trim bit defective



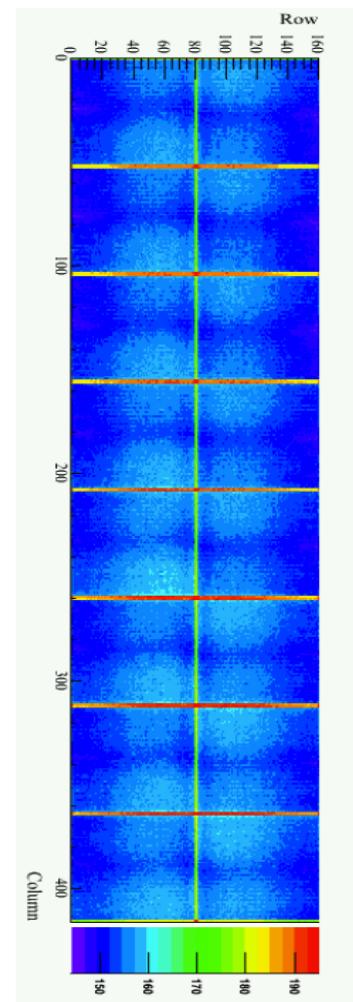
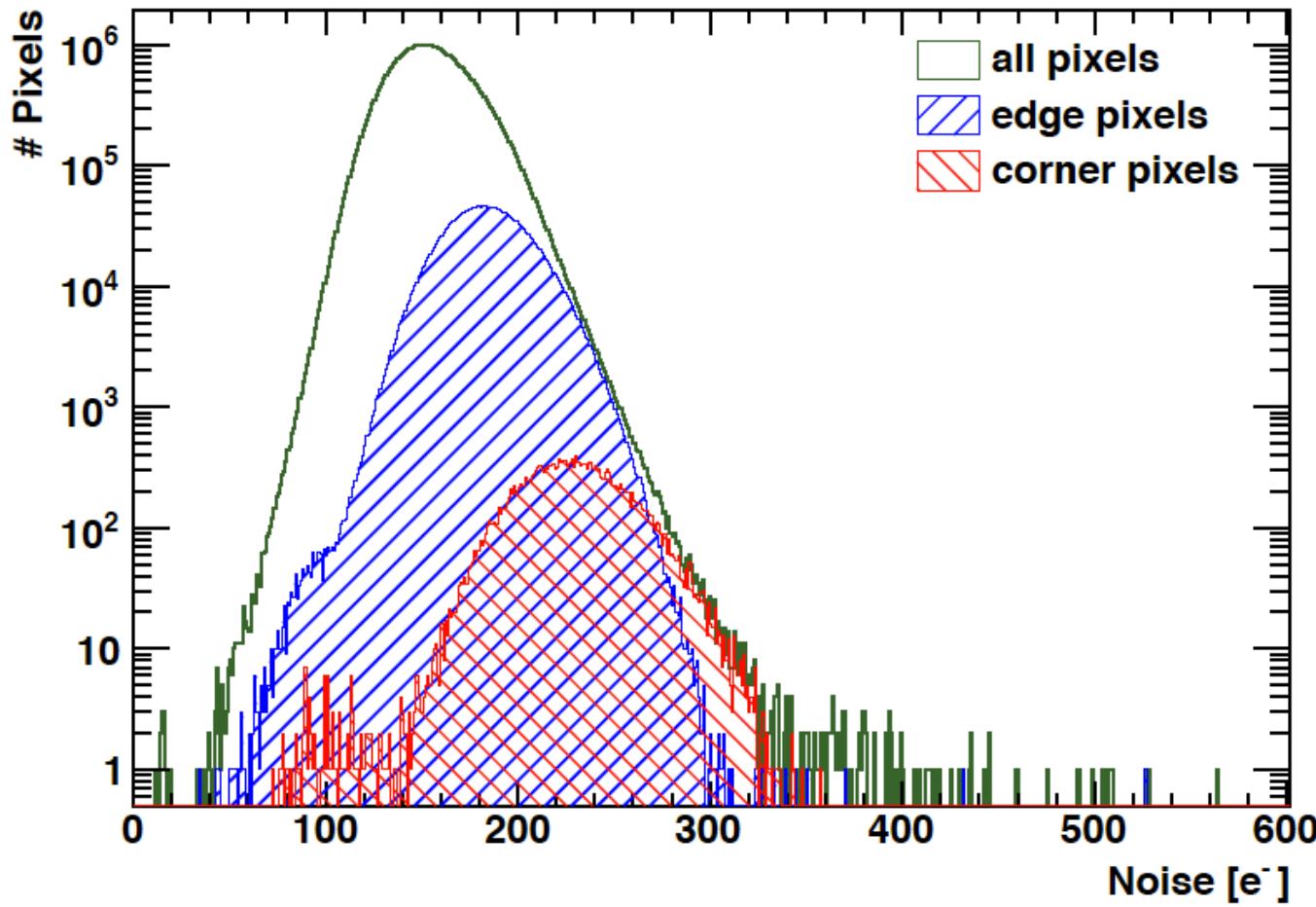
Trim value	$Vtrim$ DAC
15	0
14	250
13	200
11	150
7	100

Noise measurements

- Goal: identify noisy pixels, that have to be masked, noise of each single pixel measured
- Procedure: measure readout efficiency vs calibrate signal (V_{cal}), so-called S-curve
- Ideal (no noise) curve – step function, real curve (Gaussian noise) – error function
- Test algorithm:
 - ✓ fast threshold scan provides rough value for the threshold
 - ✓ around this value the S-curve measured with high precision, i.e. 50 readouts per point
- Complication: voltage of the calibration signal is not a monotonous function of V_{cal}
- Precision of noise measurement – 13 electrons

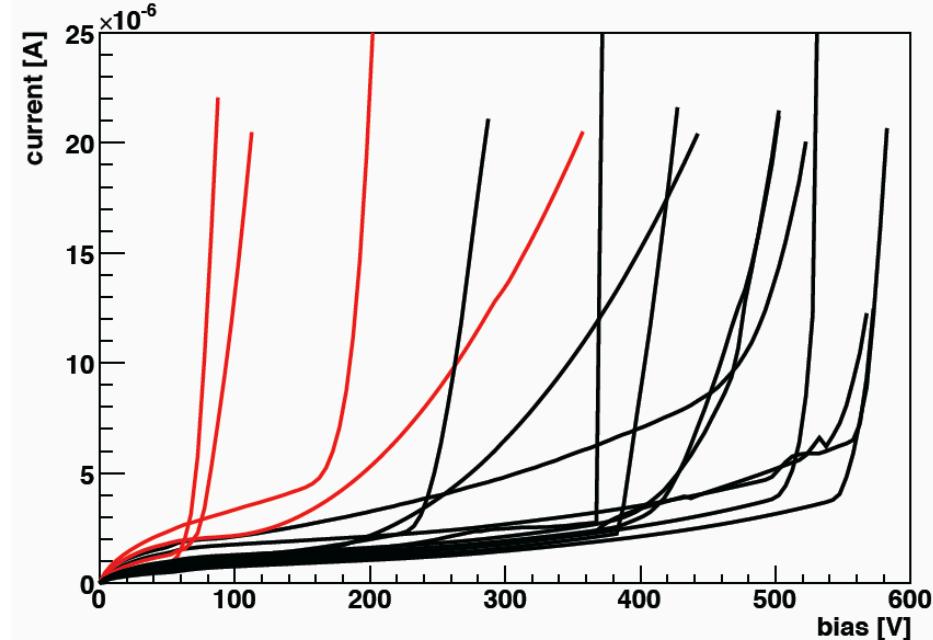
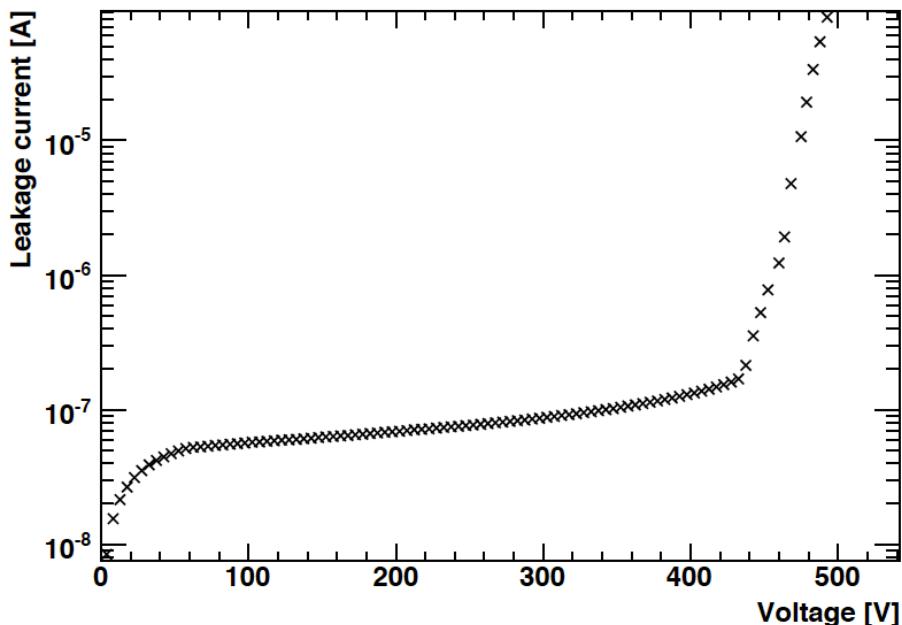


Noise measurements, cont.



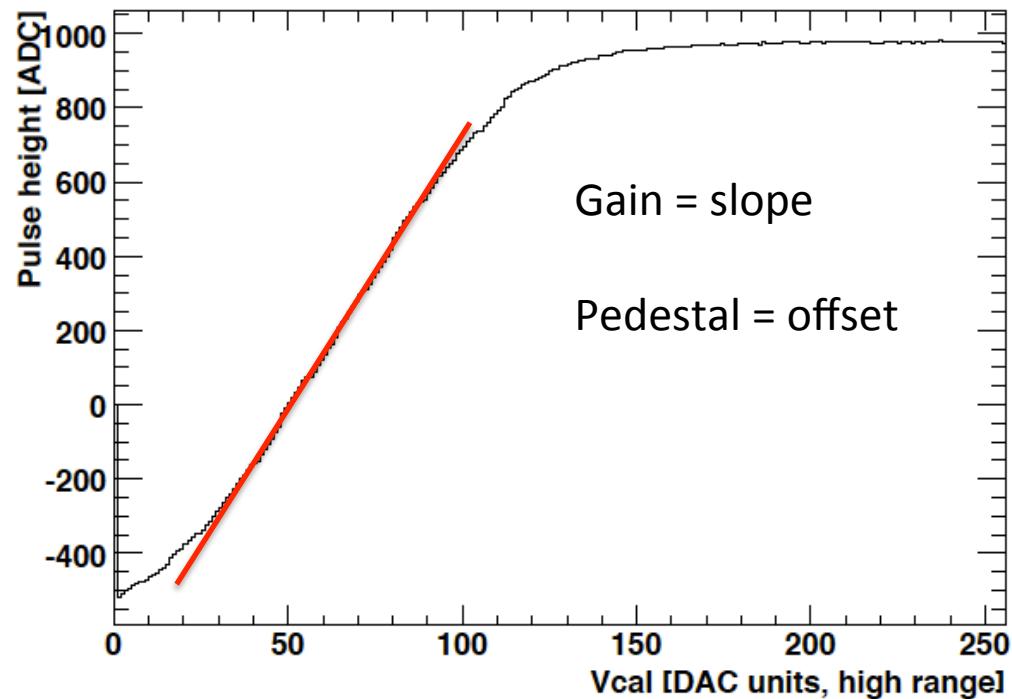
Sensor leakage current

- Goal: find Si sensor defects – high leakage current, not standard shape, early breakdown
- I-V curve: change bias voltage in step of 5V from 0 to 600V(max operation voltage after irradiation) or for $I < 100\mu A$ with 5sec per step
- I-V curve taken several time during production: on wafer, diced (sample), on module
- Qualification criteria:
 - ✓ $I(150V) < 2/10\mu A$ at $+17C$ and $< 3/15\mu A$ at $-10C$ (for grade A/B)
 - ✓ No ‘soft’ breakdown: $I(150)/I(100) < 2$

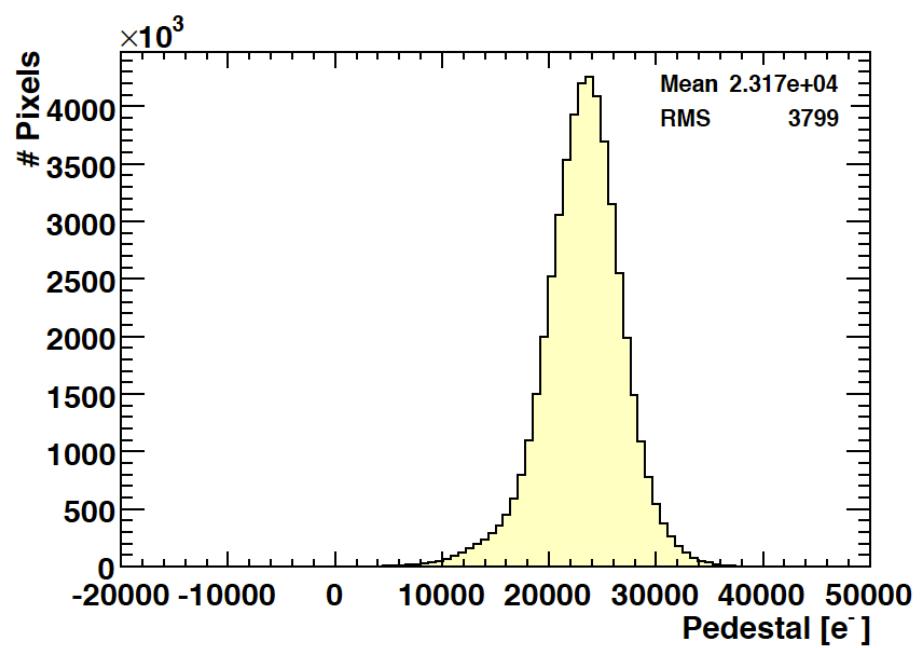
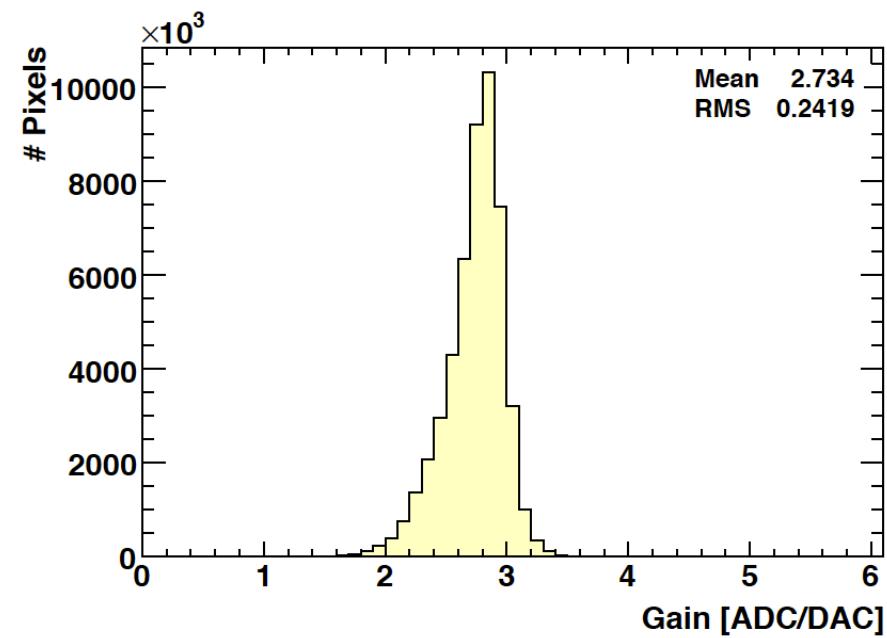


Pulse height (Gain) calibration

- Spatial hit resolution is better for analog (psi46 ROC) instead of binary readout
- To benefit from this fact, the calibration of analog readout is needed
- First step: calibrate the pulse height with internal calibration mechanism in terms of V_{cal} DAC. Second step: V_{cal} DAC calibration in electrons (see later)
- Since the variations between pixels can be large, calibration done for each pixel separately
 - ✓ V_{cal} DAC values for calibration:
50, 100, 150, 200, 250 in **low V_{cal}** range and 30, 50, 70, 90, 200 in **high V_{cal}** range
 - ✓ to measure PH for the low V_{cal} values, threshold and timing of the injected signal adjusted
 - ✓ each pulse height measurement is average over 10 readouts

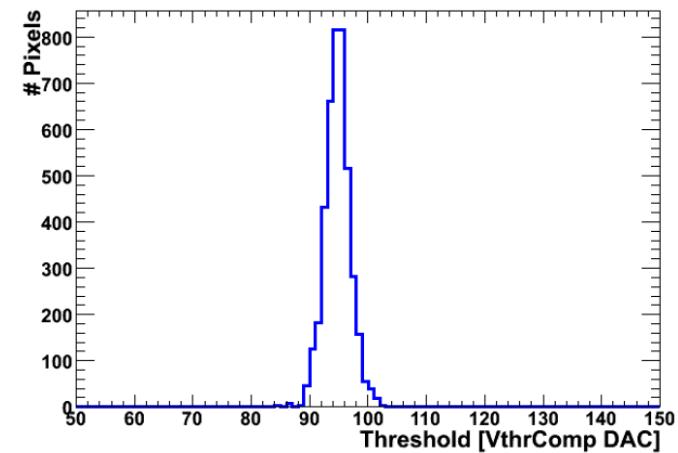
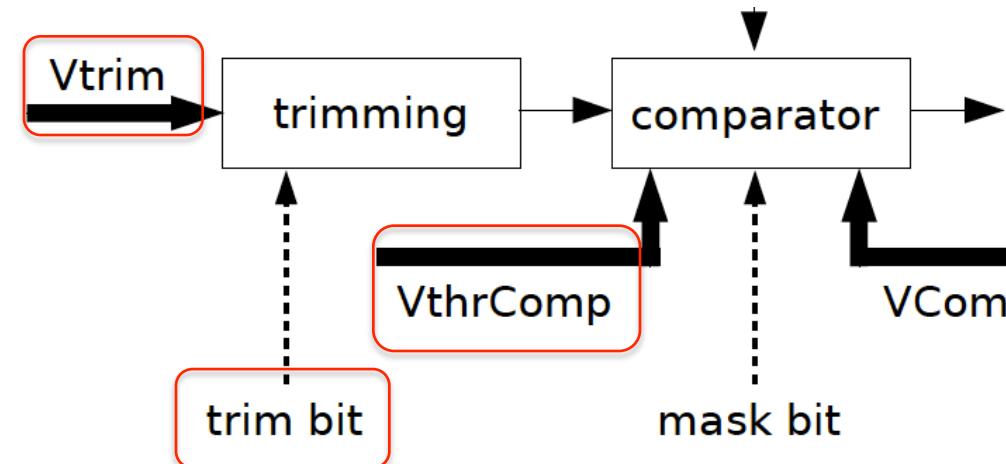


Pulse height (Gain) calibration



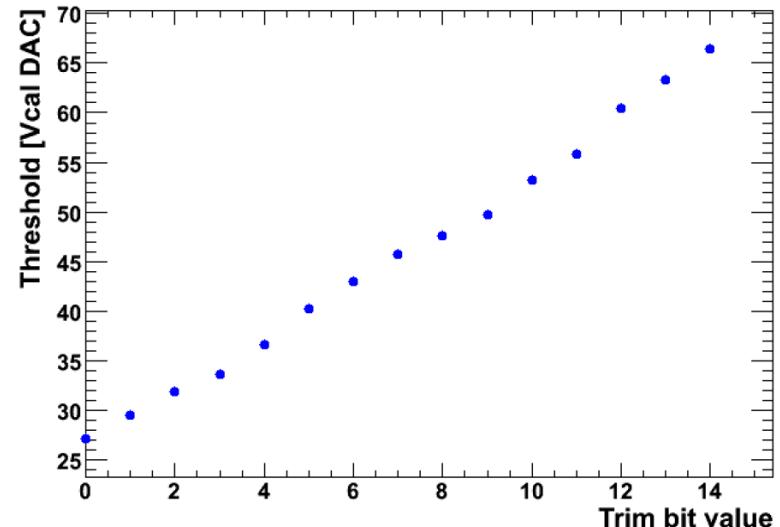
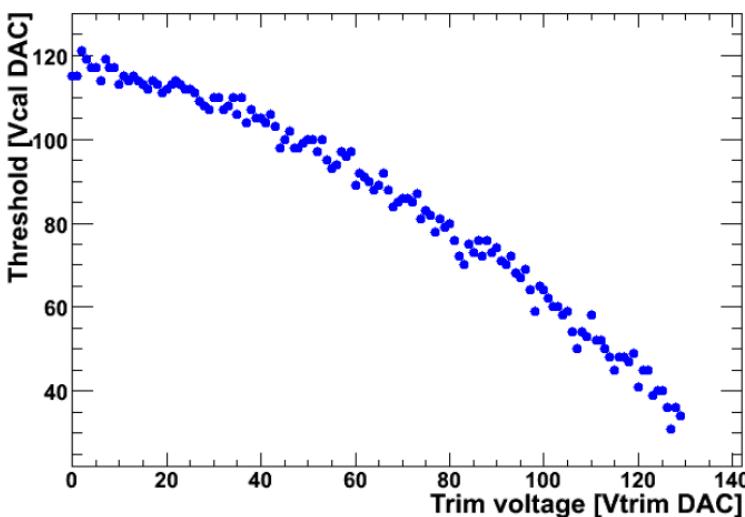
Trimming

- Goal: threshold unification for ALL pixels
- Input parameter: threshold charge (calibration voltage V_{cal})
- Free parameters:
 - ✓ threshold voltage ($V_{thrComp}$) per ROC
 - ✓ trim voltage (V_{trim}) per ROC
 - ✓ 4 trim bits per pixel
- Step 1: setting $V_{thrComp}$
 - ✓ Send internal calibrate signal with fixed $V_{cal}=60$
 - ✓ Measure $V_{thrComp}$ -threshold distribution
 - ✓ Choose minimal $V_{thrComp}$ value (ignore outliers more than 5xRMS away from mean)

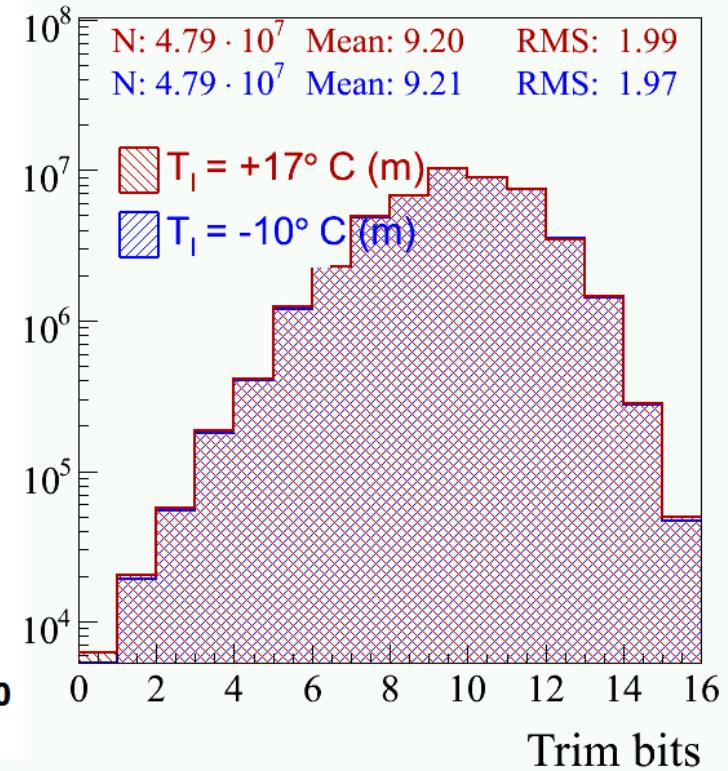
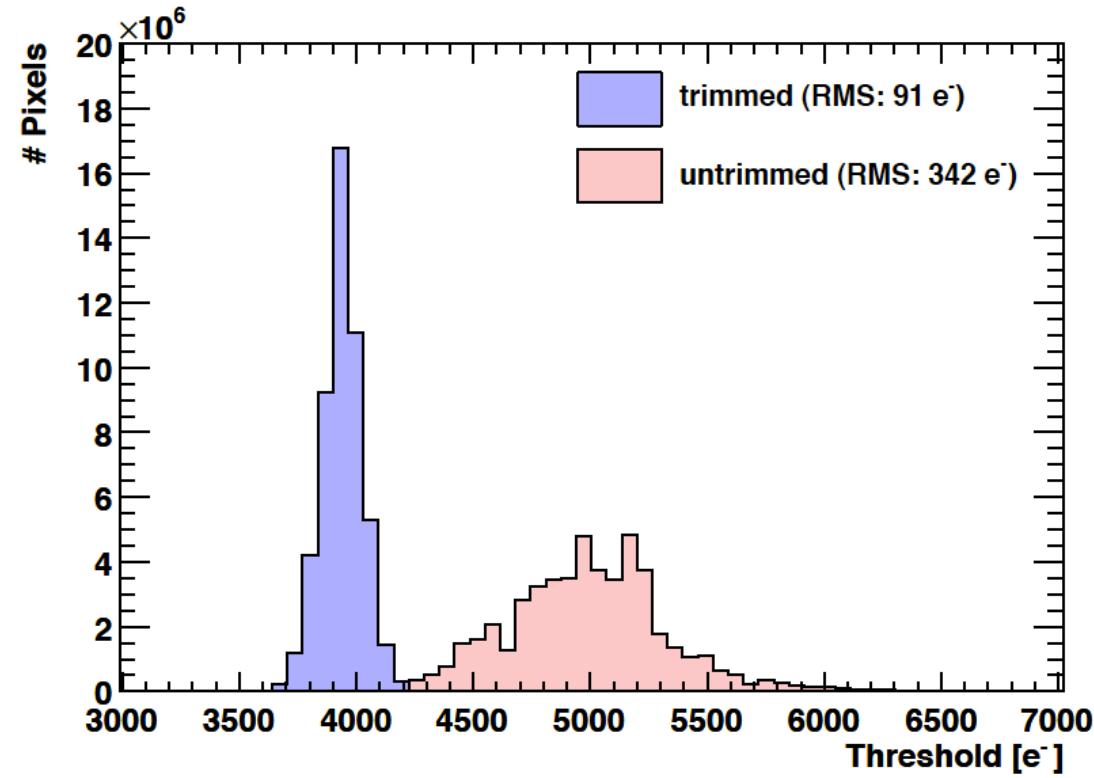


Trimming, cont.

- Step 2: setting $Vtrim$
 - ✓ Measure $Vcal$ threshold distribution for fixed $VthrComp$
 - ✓ Choose pixel with highest threshold (ignore outliers more than 5xRMS away from mean)
 - ✓ Enable all trim bits
 - ✓ Increase $Vtrim$ till target threshold
- Step 3: setting trim bits
 - ✓ Perform binary search for the optimal value
 - ✓ Optimal: Threshold as close as possible to the target threshold

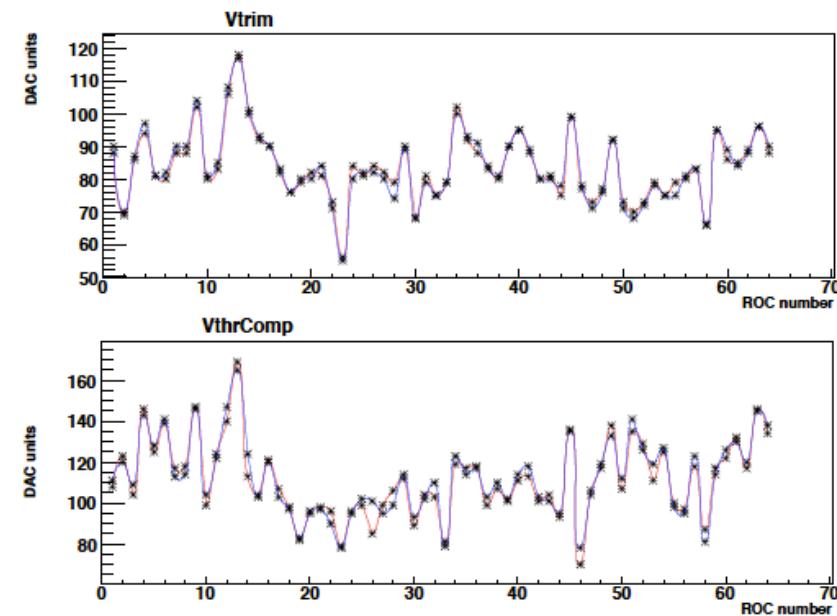
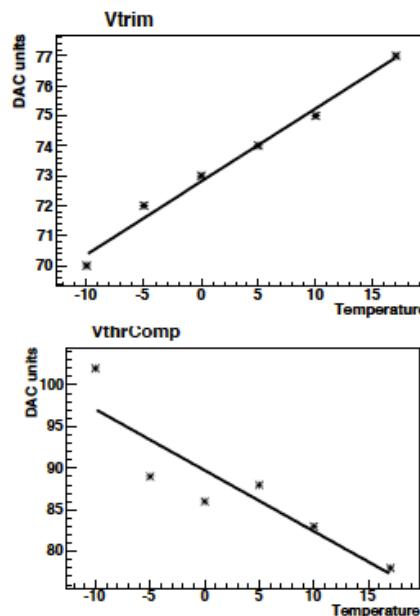


Trimming results



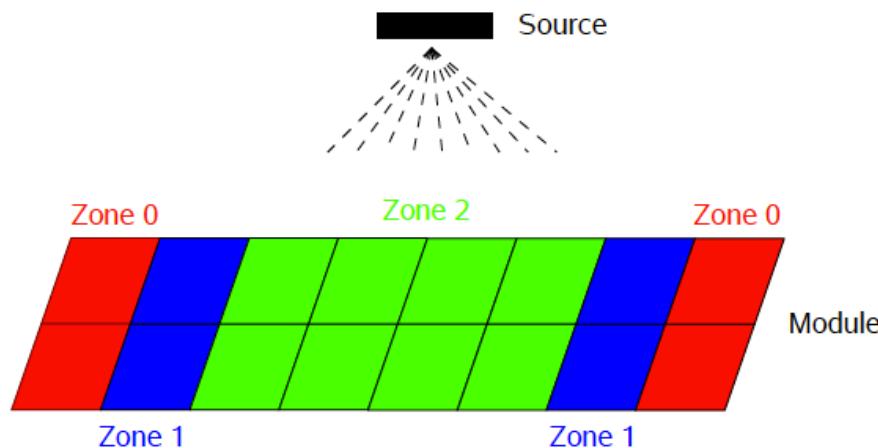
Trimming: parameterization

- ▶ Trimming is iterative procedure \Rightarrow can't be done in situ
- ▶ Trim bit values **do not depend** on target Threshold, T and irradiation dose
- ▶ $V_{ThrComp}$ and V_{trim} **depend** on target Threshold and T:
 - ▶ $V_{ThrComp}(V_{Cal}) = V_{ThrComp}(60) - 0.65 \times (V_{Cal} - 60)$
 - ▶ $V_{Trim}(V_{Cal}) = V_{Trim}(60) - 0.45 \times (V_{Cal} - 60)$



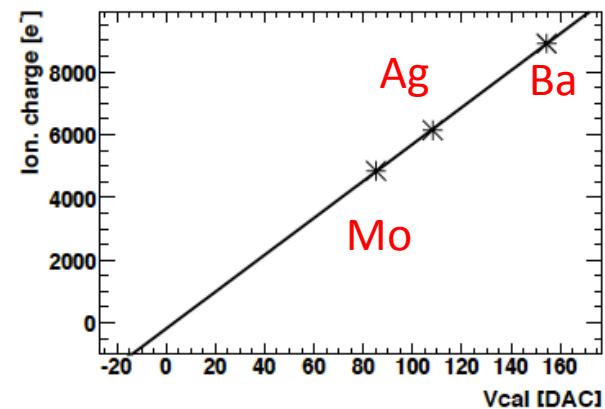
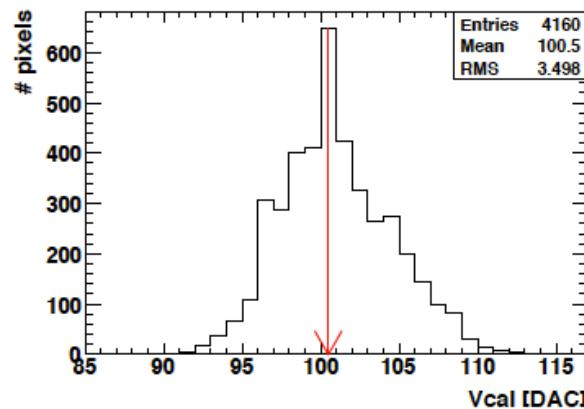
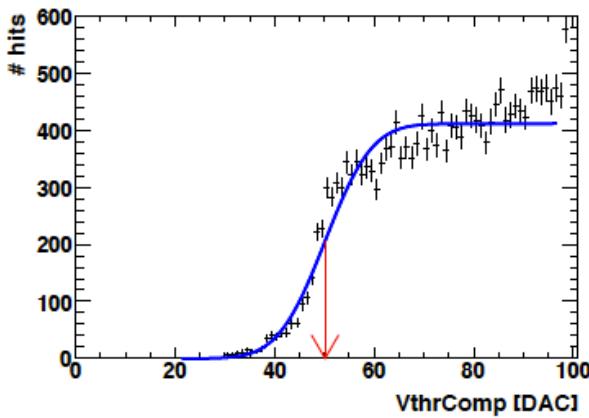
Vcal calibration with X-ray

- ▶ Twofold purpose:
 - ▶ test module response to the injected charge into Si sensor
 - ▶ calibrate internal signal used for the trimming (setting threshold)
- ▶ X-ray source:
 - ▶ Primary source: Americium-241
 - ▶ Targets: Mo(4844 e^-), Ag(6139^-), Ba (8906 e^-)
 - ▶ Random trigger, stretched bunch-crossing
- ▶ Test setup:



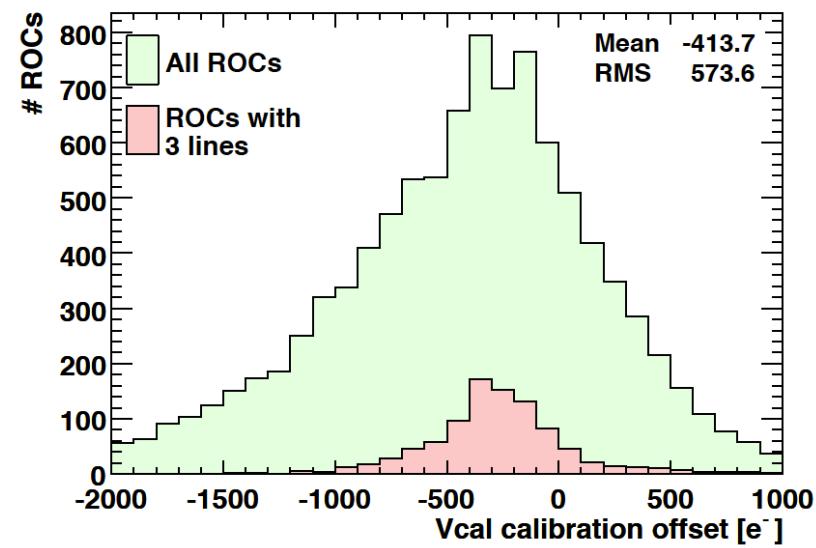
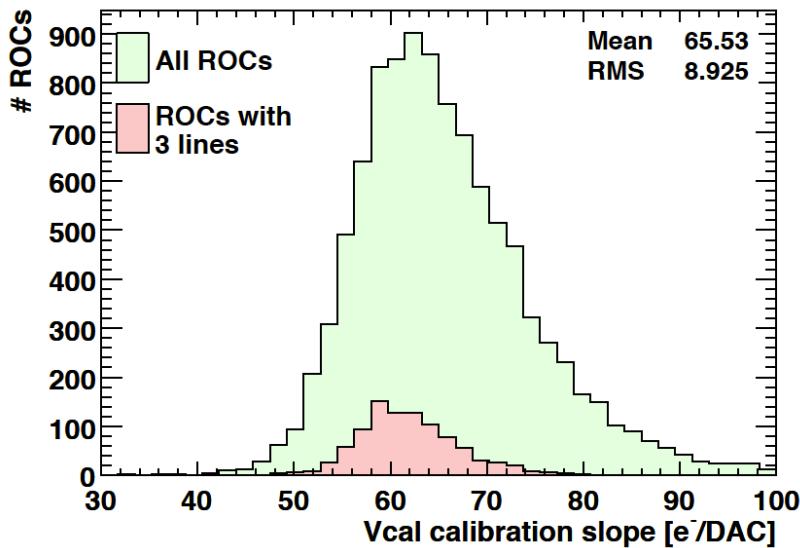
X-ray calibration procedure

- ▶ Trim ROC
- ▶ Measure # of hits vs threshold
- ▶ Fit with error function
- ▶ Find threshold (50%)
- ▶ Set VthrComp to found value
- ▶ Measure Vcal value for all pixels
- ▶ Take mean Vcal
- ▶ Combine Vcal from different sources
- ▶ Fit with a straight line
- ▶ Determine slope and offset



X-ray calibration: conclusion

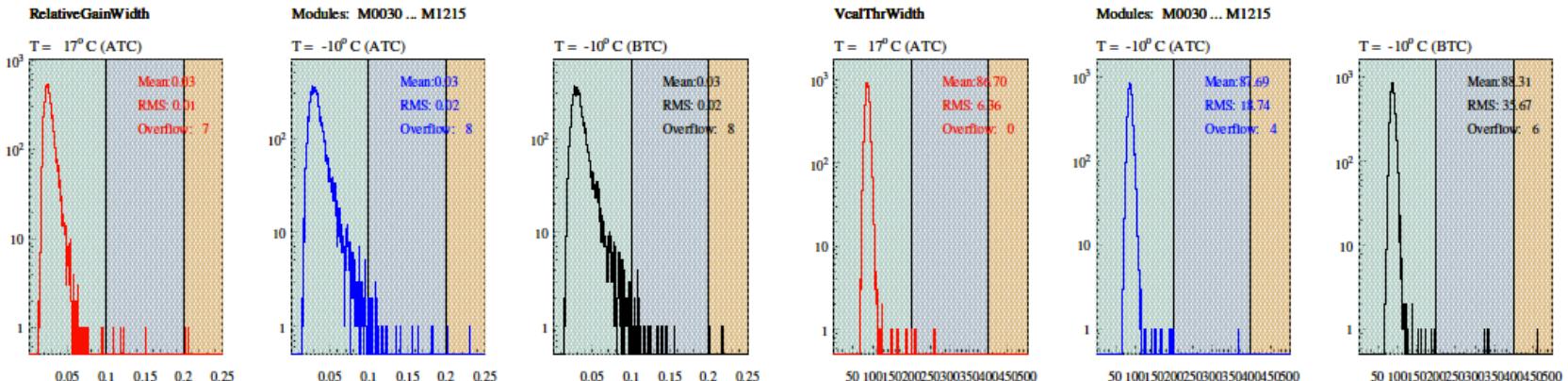
- ▶ On average 1 Vcal DAC corresponds to 66 e^-
- ▶ The mean offset at $\text{Vcal}=0$ is around -420 e^-
- ▶ Trimming with $\text{Vcal}=50$ corresponds to threshold of 2800 e^-
- ▶ For calibration use
 - ▶ if available, results for individual ROC from 3 sources
 - ▶ otherwise, mean from 2 sources average over module



Grading

	Pixel	Mask	Noise	Gain	Pedestal	Thr.	$I_{+17}^{meas}(150V)$	$I_{-10}^{calc}(150V)$
A	$\leq 1\%$	0	$\leq 500e^-$	$\leq 10\%$	$<2.5ke^-$	$<200e^-$	$<2\mu A$	$<3\mu A$
B	$\leq 4\%$	0	$\leq 1000e^-$	$\leq 20\%$	$<5.0ke^-$	$<400e^-$	$<10 \mu A$	$<15 \mu A$
C	$> 4\%$	$\geq 1\%$	$\geq 1000e^-$	$> 20\%$	$>5.0ke^-$	$>400e^-$	$>10\mu A$	$>15\mu A$

- ▶ Pixel defects/chip
- ▶ Mask: permanent readout
- ▶ Noise in e^-
- ▶ Relative Gain width
- ▶ Pedestal spread in e^-
- ▶ Vcal Threshold Width in e^-
- ▶ $I_{+17}^{meas}(150V)$: measured leakage current at $+17^\circ$
- ▶ $I_{-10}^{calc}(150V)$: recalculated leakage current at -10°

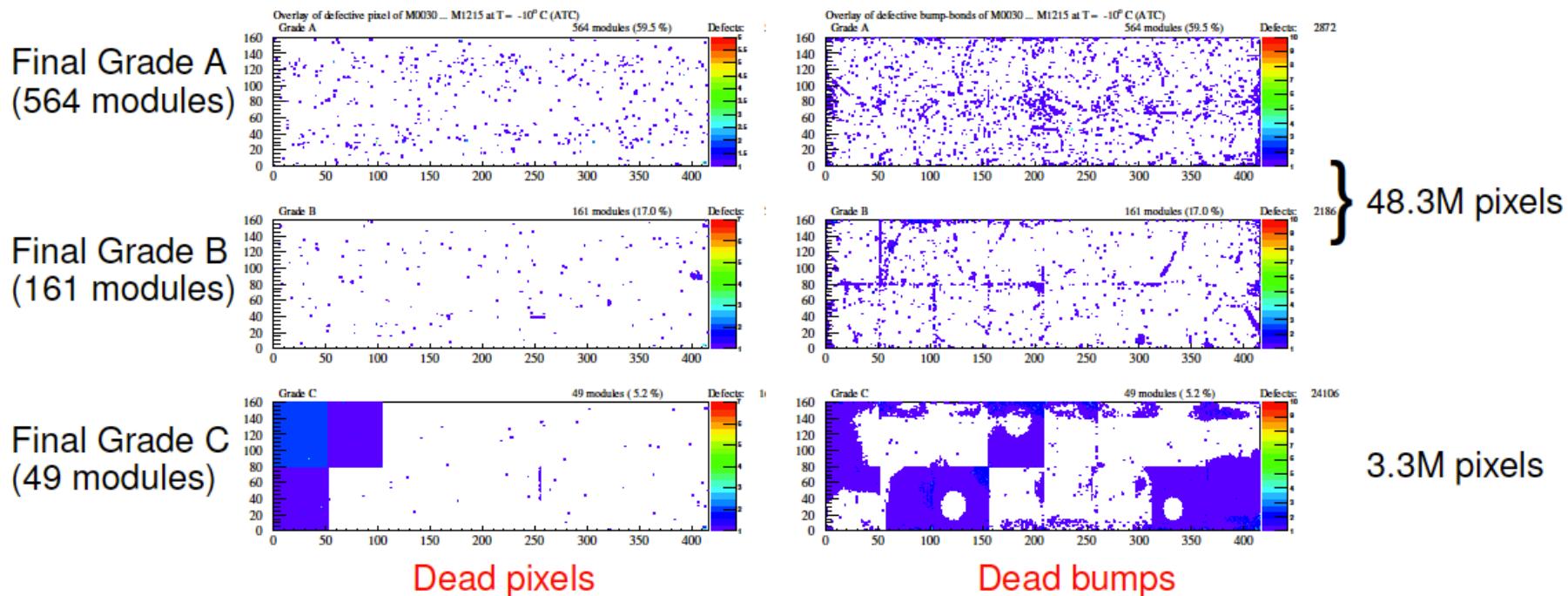


Production summary

948 modules tested (827 full/ 121 half)

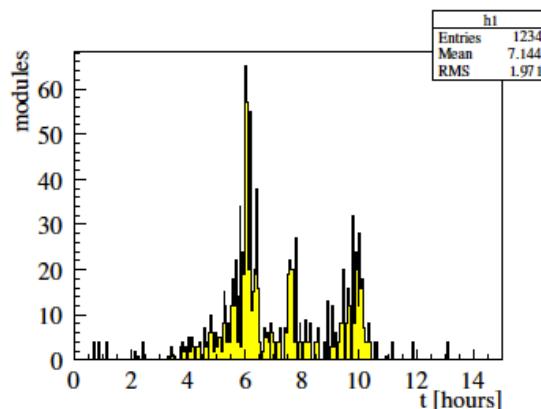
- ▶ 565/161 graded as A/B → 88% || 87/23 → 91%
- ▶ 101 graded as C → 12% || 11 → 9%

Overlay of modules tested at $T = -10^\circ \text{C}$ (ATC)

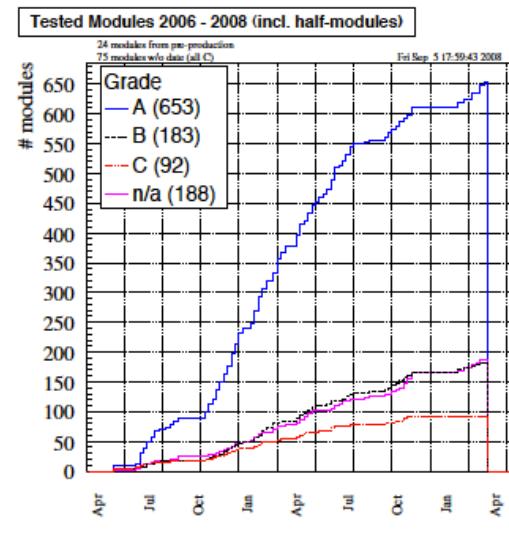
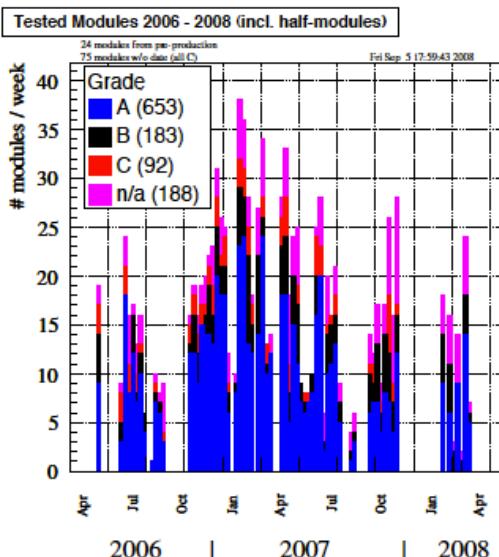
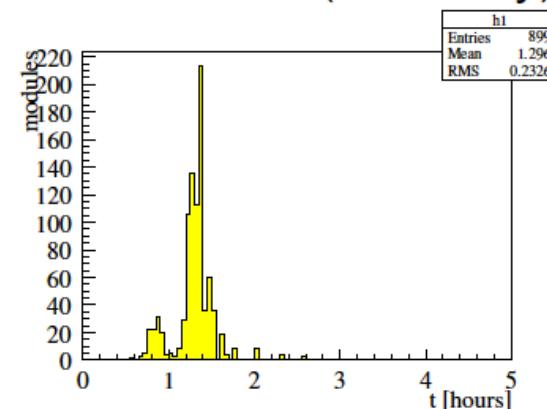


Production time

Full tests



Short tests (w/o x-ray)

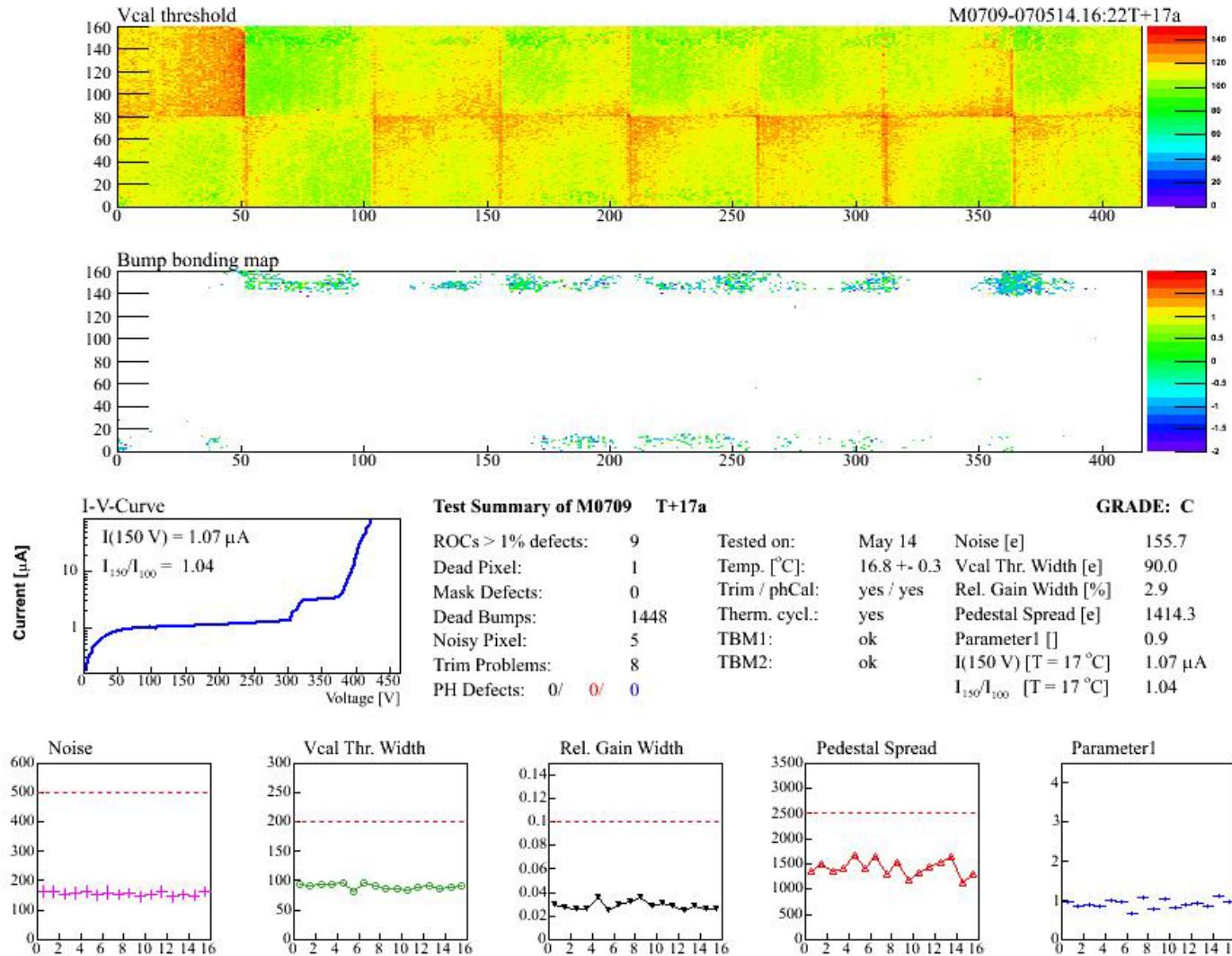


On-line test ‘DB’ at PSI

----> [Weekly Summaries](#)

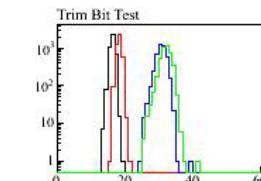
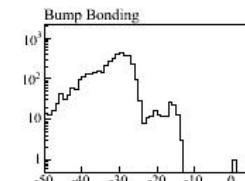
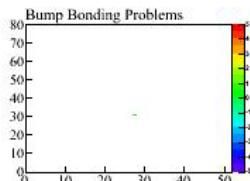
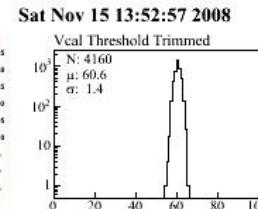
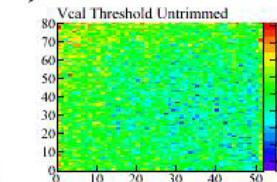
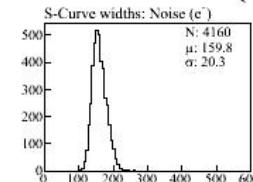
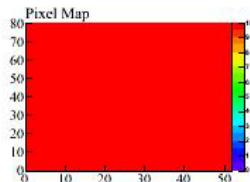
FINAL	Module	Test	Date	<u>Grade</u>	Full	Short	<u>Pixel Defects</u>	ROCs > 1%	Noise	Trimming	PH Cal.	Ad. Lvl	Current	I (150 V)	IV-Slope	Temp	T cycling	Mount Pos.	Comments
C	M1216	T-10b	Mar 17 2008	B	B	c	0/0/6/0/0 1/0/0/2/0	0	ok	ok	1B Ped	fits	1.54 uA (0.13 uA)	1.72 uA (0.14 uA)	1.53	-10.00+-0.02	yes (2.5+-9.2)	-	Ped Par C13 ?
C	M1216	T-10a	Mar 17 2008	B	B	c	0/0/6/0/0 1/1/0/0/0	0	ok	ok	1B Ped	fits	1.30 uA (0.11 uA)			-10.00+-0.02	yes (2.5+-9.2)	-	Ped Par C13 ?
C	M1216	T+17a	Mar 17 2008	A	B	c	0/0/6/0/0 2/0/0/0/0	0	ok	ok	ok	fits	1.17 uA	0.80 uA	1.26	16.87+-0.86	yes (2.5+-9.2)	-	
A	M1215	T-10b	Mar 20 2008	A	A	a	0/0/3/0/0 0/6/0/0/0	0	ok	ok	ok	fits	3.36 uA (0.28 uA)	2.70 uA (0.22 uA)	1.60	-10.00+-0.02	yes (2.8+-9.6)	21048	
A	M1215	T-10a	Mar 20 2008	A	A	a	0/0/3/0/0 2/9/0/0/0	0	ok	ok	ok	fits	2.65 uA (0.22 uA)			-10.00+-0.01	yes (2.8+-9.6)	21048	
A	M1215	T+17a	Mar 20 2008	A	A	a	0/0/3/0/0 0/5/0/0/0	0	ok	ok	ok	fits	1.39 uA	1.50 uA	1.15	16.84+-0.27	yes (2.8+-9.6)	21048	
A	M1213	T-10b	Mar 20 2008	A	A	a	0/0/3/0/0 0/2/0/0/0	0	ok	ok	ok	fits	0.36 uA (0.03 uA)	0.42 uA (0.03 uA)	1.20	-10.00+-0.02	yes (2.8+-9.6)	210412	
A	M1213	T-10a	Mar 20 2008	A	A	a	0/0/3/0/0 0/5/0/0/1	0	ok	ok	ok	fits	0.35 uA (0.03 uA)			-10.00+-0.01	yes (2.8+-9.6)	210412	
A	M1213	T+17a	Mar 20 2008	A	A	a	0/0/3/0/0 0/7/0/0/0	0	ok	ok	ok	fits	0.51 uA	0.56 uA	1.10	16.84+-0.27	yes (2.8+-9.6)	210412	
B	M1211	T-10b	Mar 18 2008	B	B	a	0/0/6/0/0 2/0/0/0/1	0	ok	ok	1B Gain	fits	3.01 uA (0.25 uA)	0.81 uA (0.07 uA)	1.10	-10.00+-0.02	yes (2.6+-9.4)	311313	Gain C11 ?
B	M1211	T-10a	Mar 18 2008	B	B	a	0/0/6/0/0 3/0/0/0/4	0	ok	ok	1B Gain	fits	0.77 uA (0.06 uA)			-10.00+-0.02	yes (2.6+-9.4)	311313	Gain C11 ?
B	M1211	T+17a	Mar 18 2008	A	B	a	0/0/6/0/0 2/0/0/0/0	0	ok	ok	ok	fits	1.05 uA	1.21 uA	1.06	16.81+-0.31	yes (2.6+-9.4)	311313	

On-line test 'DB' at PSI, cont.



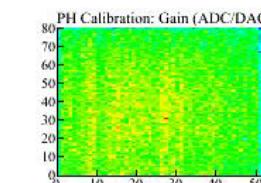
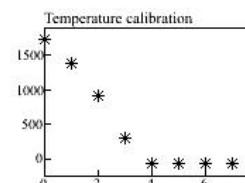
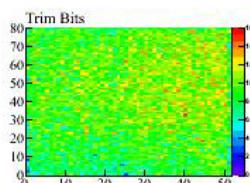
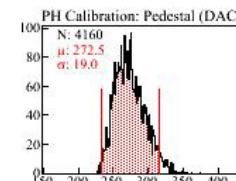
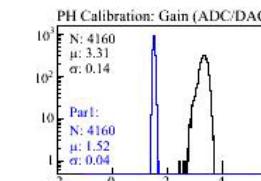
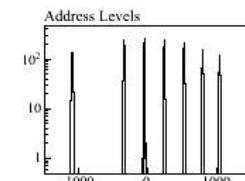
On-line test ‘DB’ at PSI, cont.

M1216-080317.08:49 T-10b (C0)



Summary

Dead Pixels:	0
Mask defects:	0
Dead Bumps:	1
Dead Trimbits:	0
Address Probl:	0
Noisy Pixels 2:	0
Trim Probl.:	0
PH defects:	0/ 0/ 0



Op. Parameters

VANA:	164 DAC
CALDEL:	84 DAC
VTHR:	96 DAC
VTRIM:	136 DAC
IBIAS_DAC:	99 DAC
VOFFSETOP:	82 DAC

Preparation for Upgrade 1 detector

New digital ROC

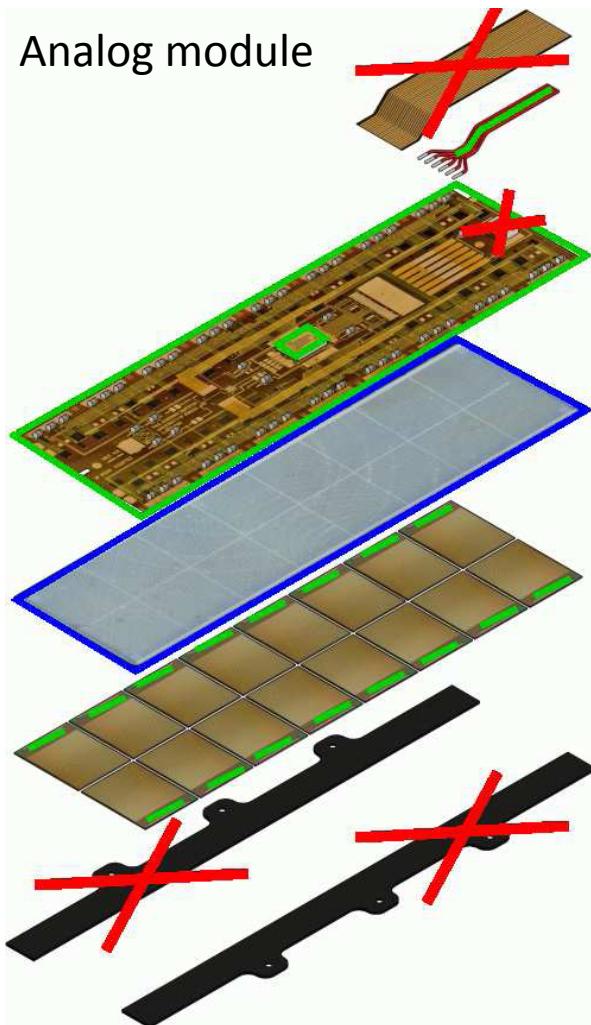
Table 5.1: Comparison of the PSI46V2 and PSI46dig Readout chips.

	PSI46V2	PSI46DIG
ROC size	7.9 x 9.8 mm	7.9 x 10.2 mm
Pixel size	100 x 150 μm	100 x 150 μm
Smallest radius	4.3cm	2.9cm
Settable DACs / registers	26 / 2	19 / 2
Power Up condition	not defined	default values
pixel charge readout	analog	digitized, 8bit
Readout speed	40 MHz	160 Mbit/s
Time stamp Buffer size	12	24
Data Buffer size	32	80
Output Buffer FIFO	no	yes
Double column Speed	20 MHz	40 MHz ^(*)
Metal layers	5	6
Leakage current compensation	yes	no
in-time threshold	3500 e	< 2000 e
PLL	no	yes
Data loss at max Operating flux	$\sim 3.8\%$ at 120 MHz/cm ²	$\sim 3\%$ at 580 MHz/cm ² ^(*)

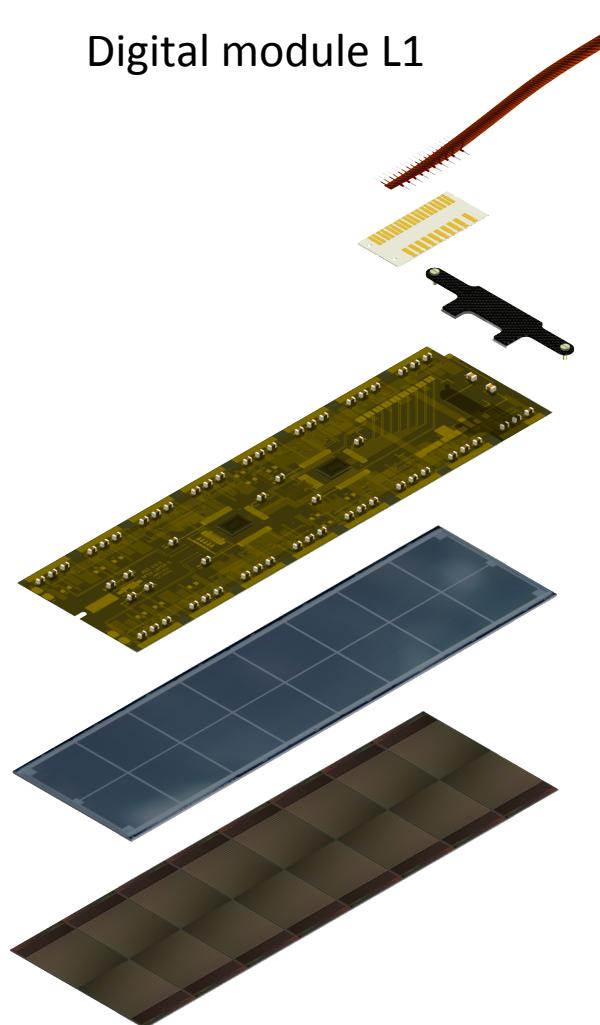
(*) valid for advanced L1 version

Digital modules

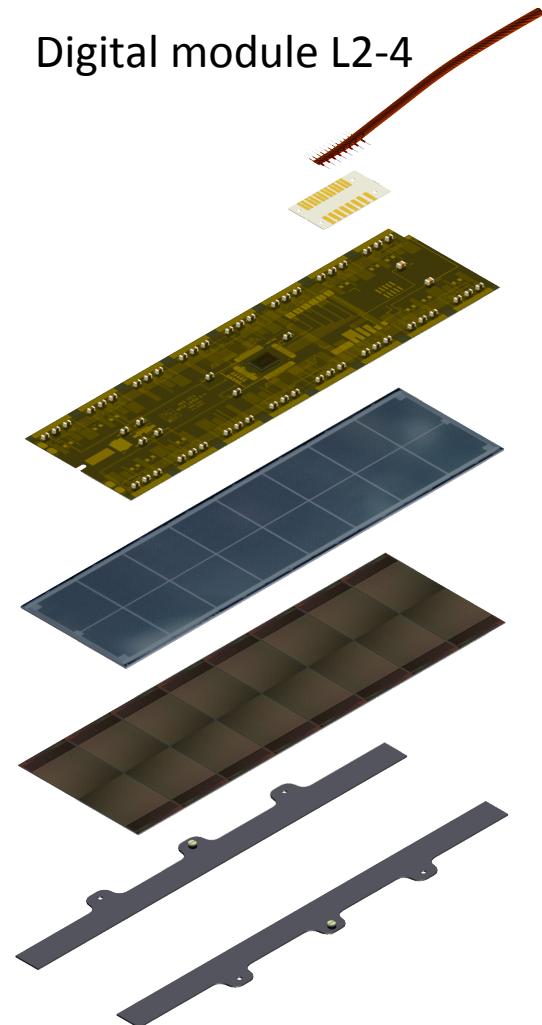
Analog module



Digital module L1

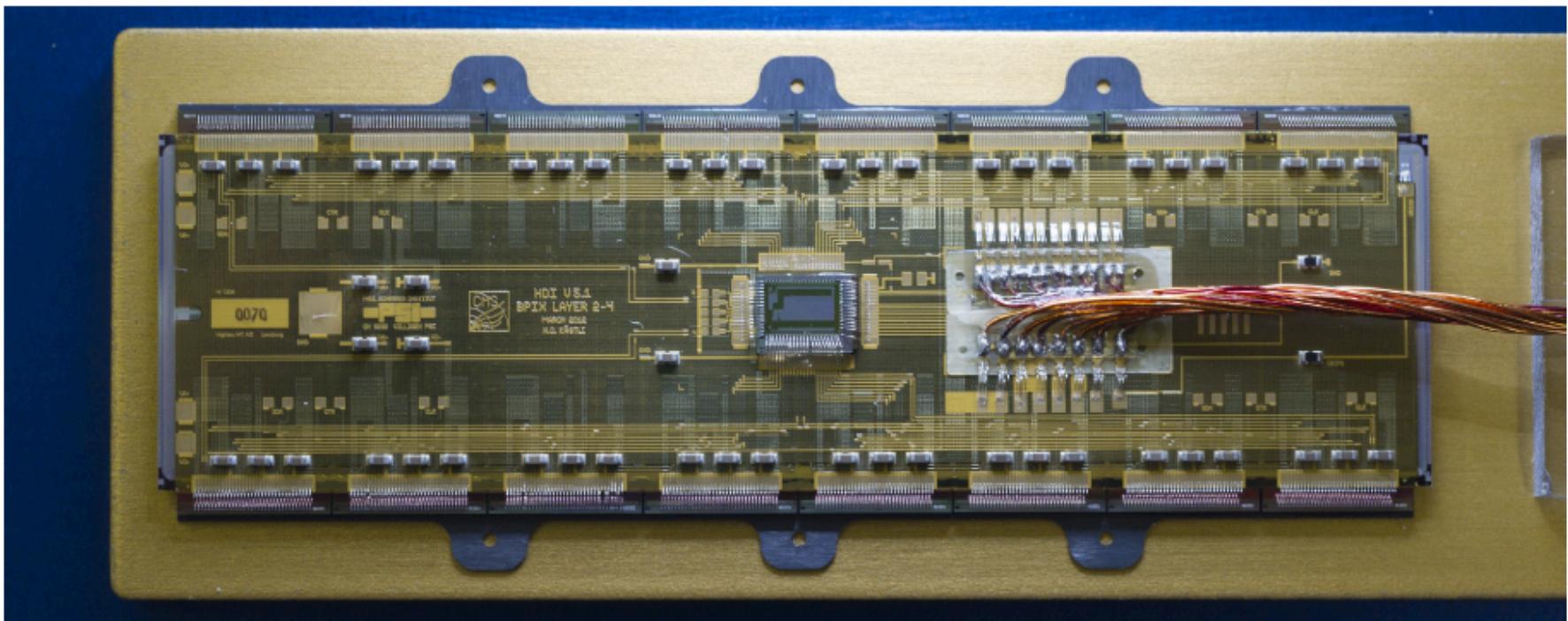


Digital module L2-4



First digital module

- Note: Digital TBM for BPIX currently not available (expected Spring 2013).
TBM-07a (FPIX) used instead. Module operation only with restrictions possible ($\frac{1}{2}$ speed readout – uncoded).
- The purpose of building this sensor module was to check the modified assembly tools, handling and the new cable connection to the HDI.

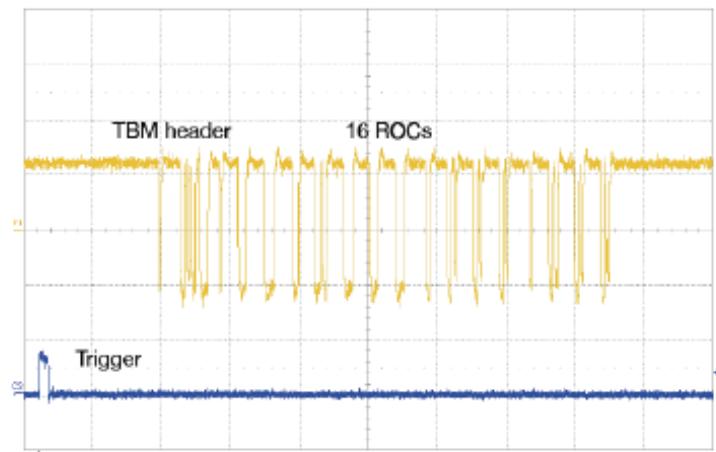
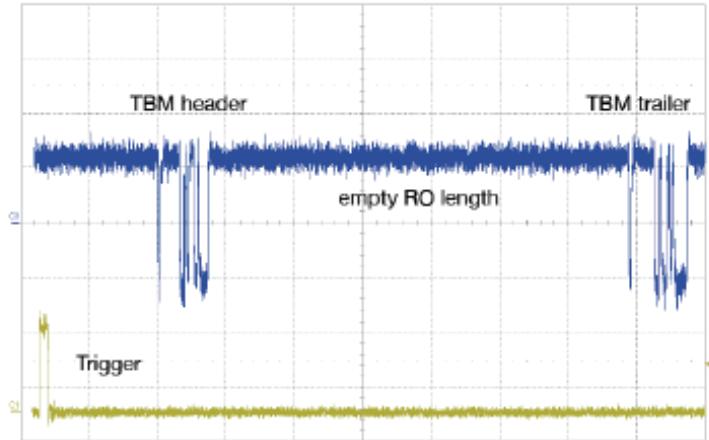


Digital module test

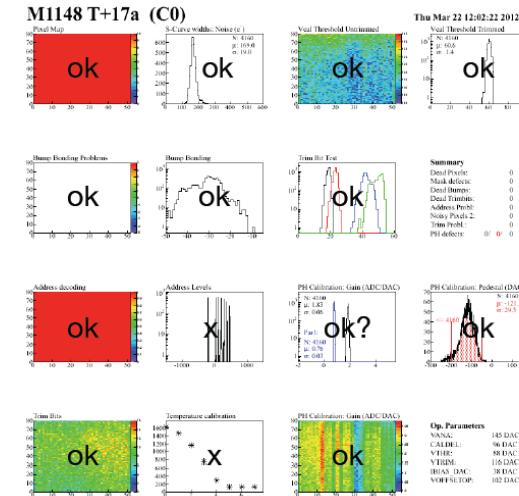
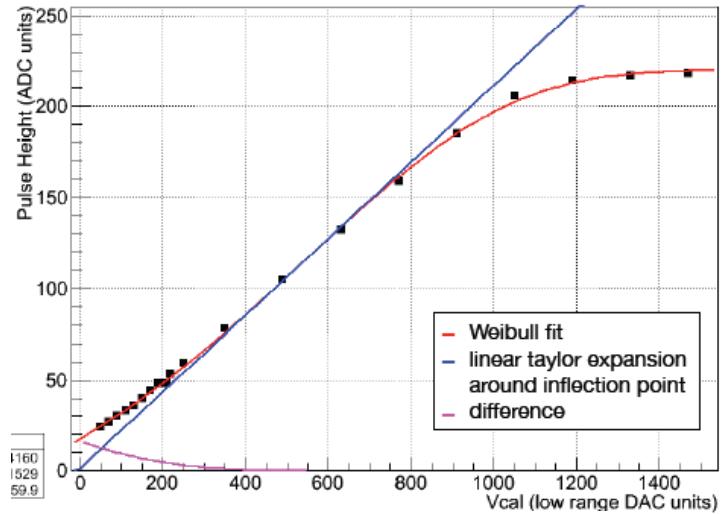
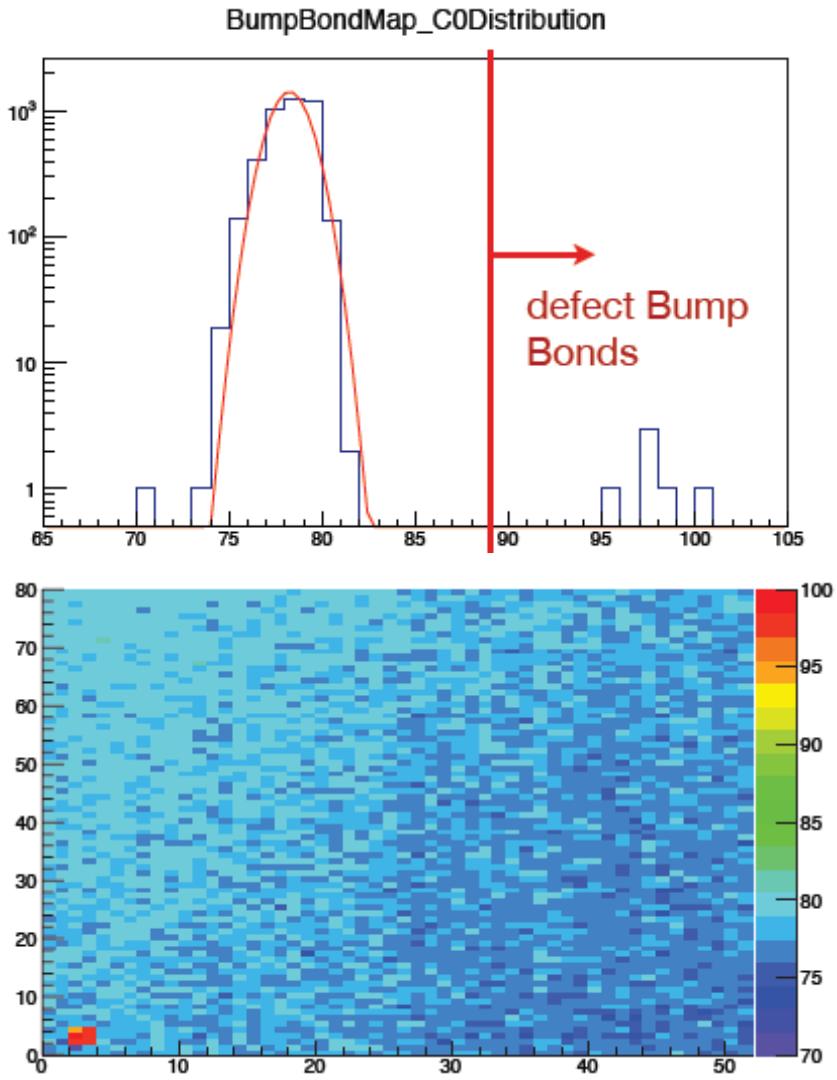
Testing Status

- TBM programmable (SDA/RDA)
- Token going through all ROCs
- empty readout with TBM header and trailer
- SDA on TBM branches
- Readout of ROCs on chip itself ok
- TBM Problem:
 - ROCs sometimes programmable (timing problem)
 - readout not passing TBM to Testboard

→ Ed Bartz identified a problem in the TBM



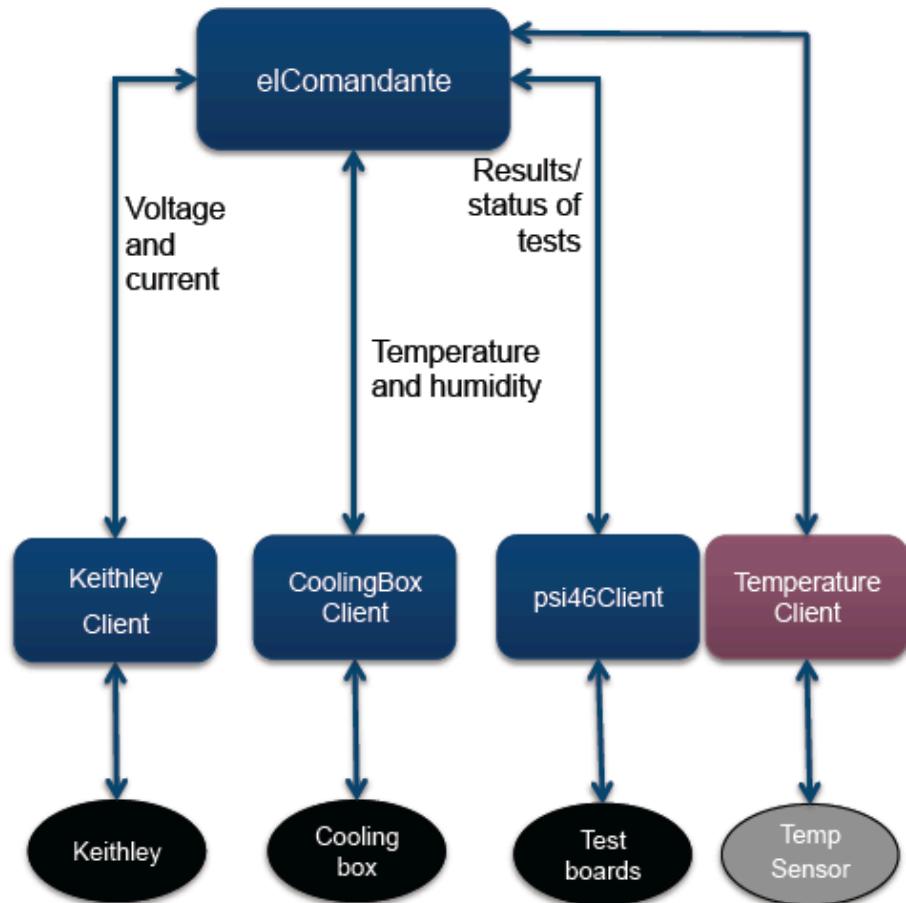
Digital module: full test



New full test supervisor

eComandante: main ideas

- every hardware tool is controlled by an individual software client
- The communication between this software clients is made by network messages
 - Server/Client structure based on a subscription model (libsubsystem)
- Advantage:
 - Easy to substitute one client(e.g. control of coolingbox)
 - A client crash will not crash the whole test
 - Easy to expand software with more clients(e.g. temp sensors, etc.)



New full test supervisor, cont.

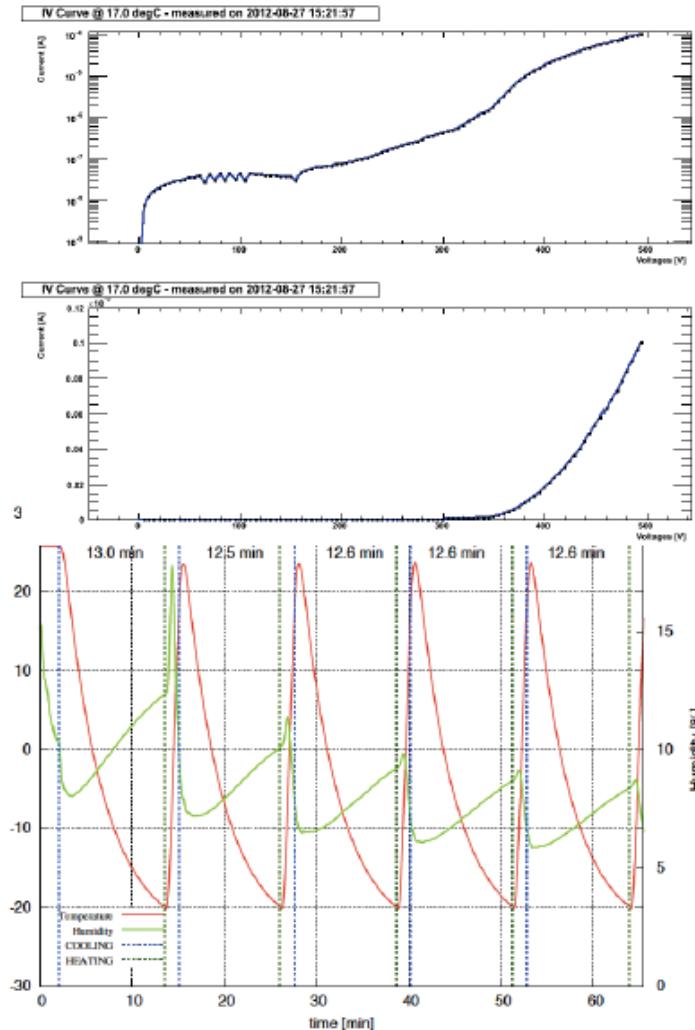
Status of development I

KeithleyClient:

- Based on python
- IV curves and automatic voltage/current monitoring during tests

Cooling Box Client:

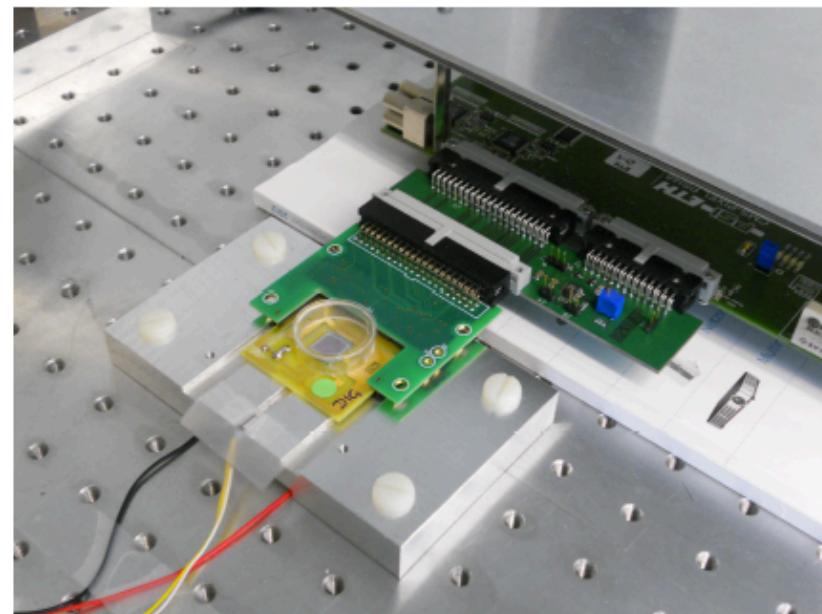
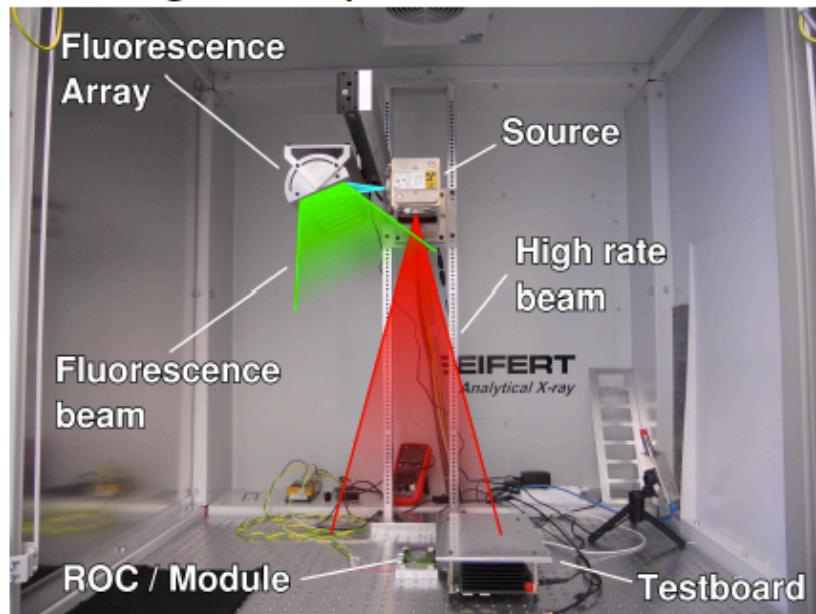
- Dry/cool/heat-routine can be adjusted for any temperature
- Automatic stop at high humidity(interlock)
- Automatic cycling
 - New: +20 / -20 degC
→ 12.5 min
 - Old: +17 / -10 degC
→ 10 min



New test setup: X-ray

At ETH we have an x-ray setup that allows both high rate and monochromatic illumination of ROCs/modules.

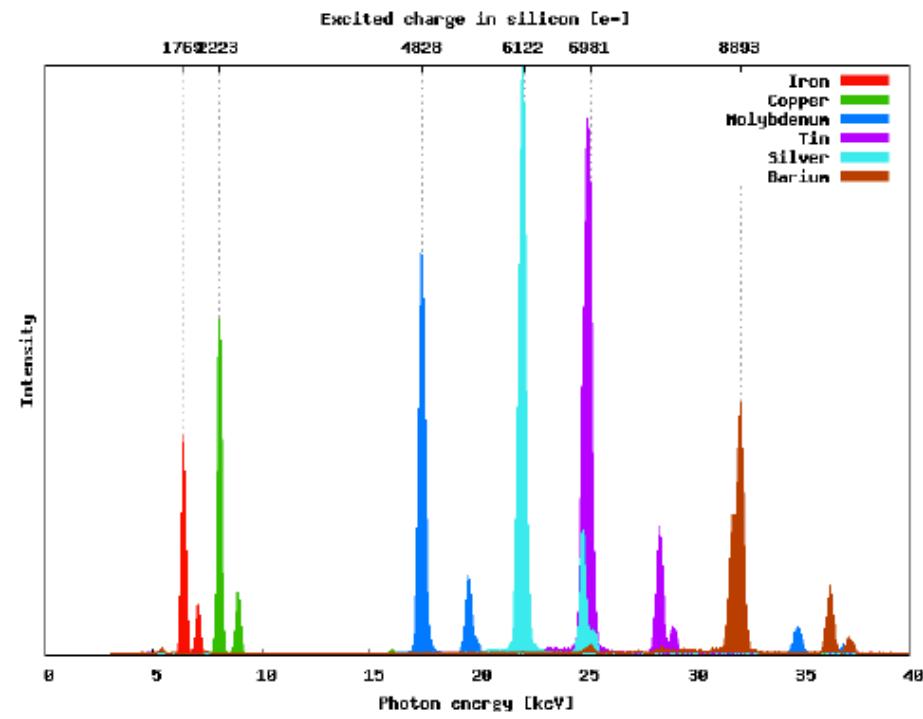
- ▶ Same setup for both illumination types
- ▶ ROC cooled to 17 ° C
- ▶ Use adapter board with analog testboard to work with the digital chip



New test setup: X-ray, cont.

Array of 6 materials as fluorescence targets

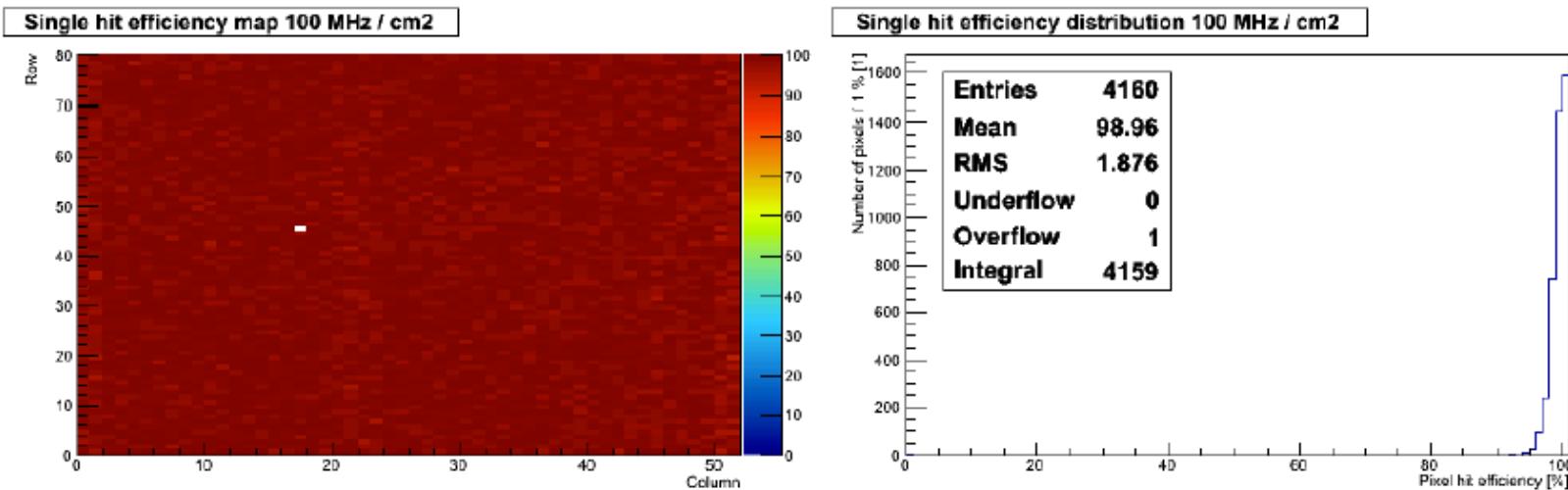
- ▶ Iron (1769 e⁻)
- ▶ Copper (2223 e⁻)
- ▶ Molybdenum (4828 e⁻)
- ▶ Silver (6122 e⁻)
- ▶ Tin (6981 e⁻)
- ▶ Barium (8893 e⁻)



High X-ray rate test: hit efficiency

Efficiency determined through repetitive injection of the calibrate signal and readout.

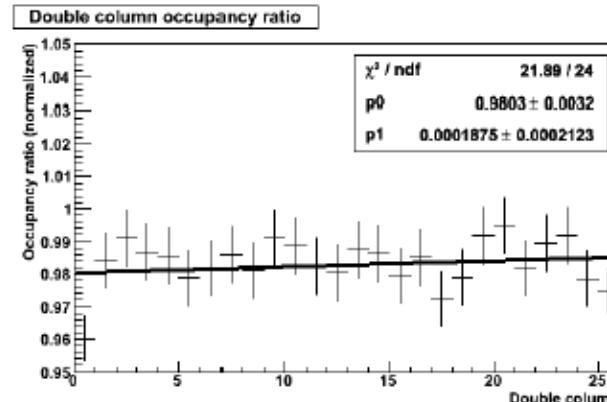
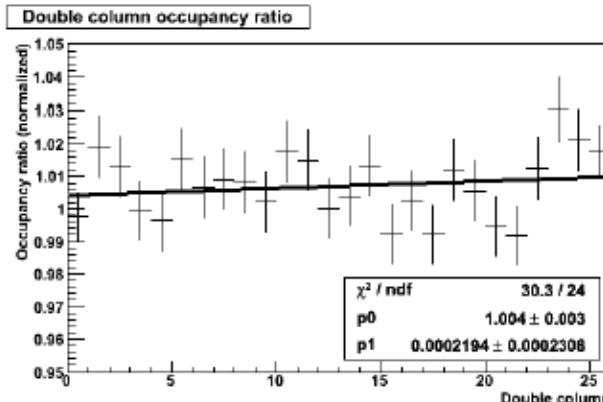
- ▶ Efficiency is defined as ratio between read-out and injected hits
- ▶ Measurement is done along with high rate x-ray hits
- ▶ At present limited by decoding error problems that have negative impact on the efficiency
 - ▶ Cause is not clear yet, currently under investigation



High X-ray rate test: dcol efficiency

Test the efficiency of individual double columns with x-rays only.

- ▶ Take data at low and high rate and determine occupancy of double columns
- ▶ Ratio of high vs low rate occupancy eliminates problems with
 - ▶ non-uniform illumination
 - ▶ shadow of HDI (not present here)
 - ▶ bad bump-bonds
- ▶ Double columns with less efficiency at high rate will show a smaller ratio

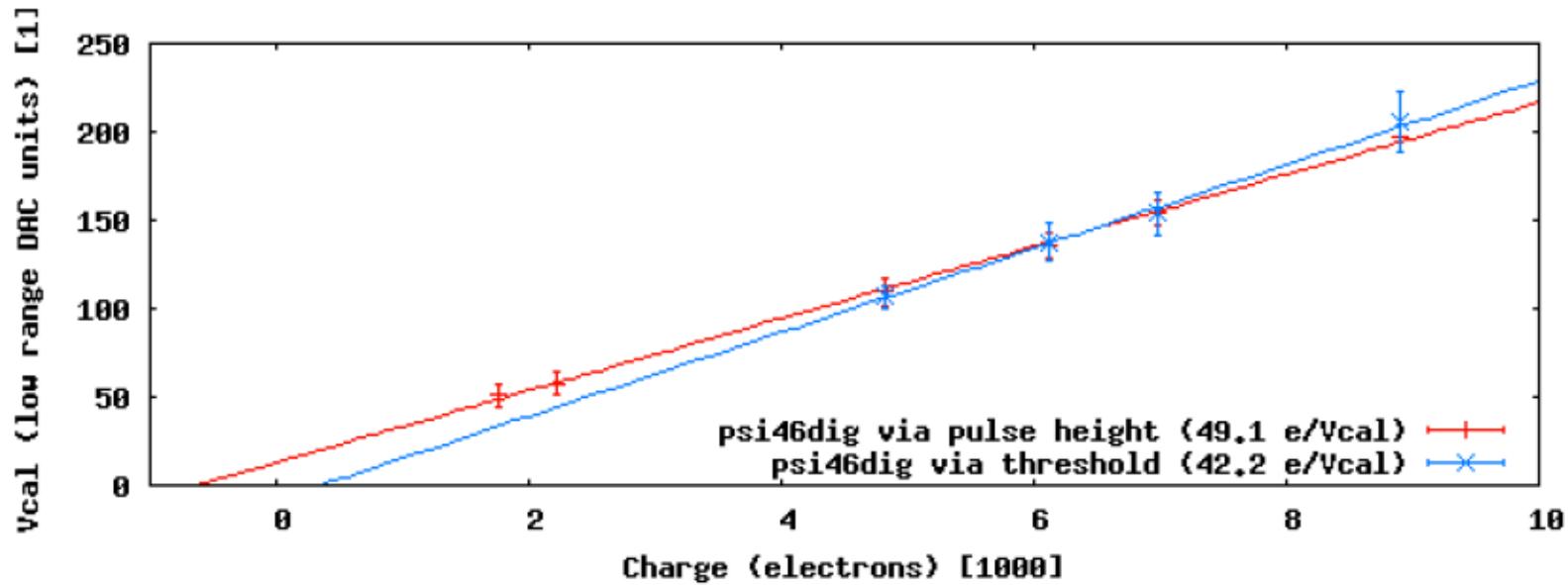


Vcal calibration with X-ray

Several groups have now found that VCal calibration is not the same when done

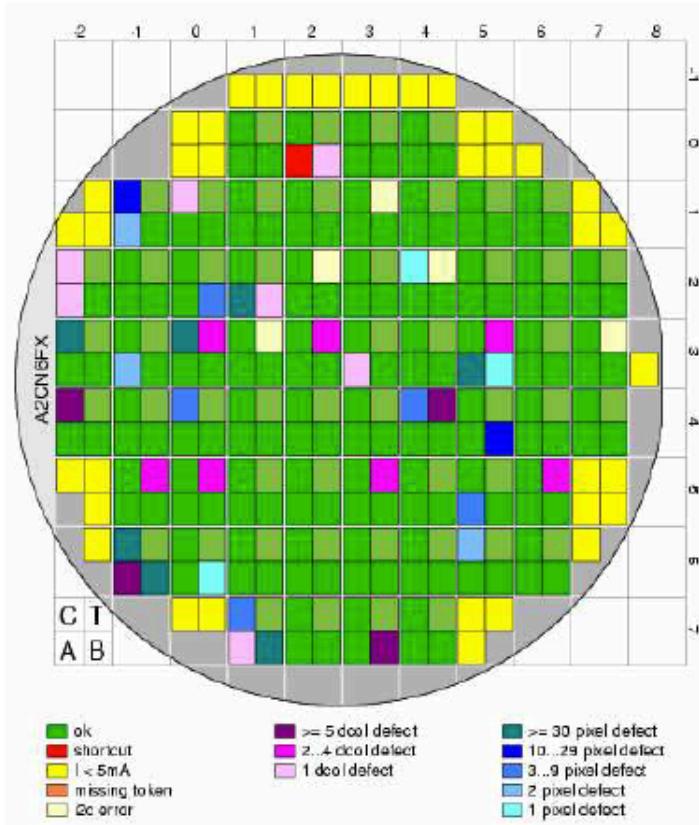
- ▶ through threshold (using threshold scan)
- ▶ through the pulse height (using pulse height calibration)

The cause is not yet known.



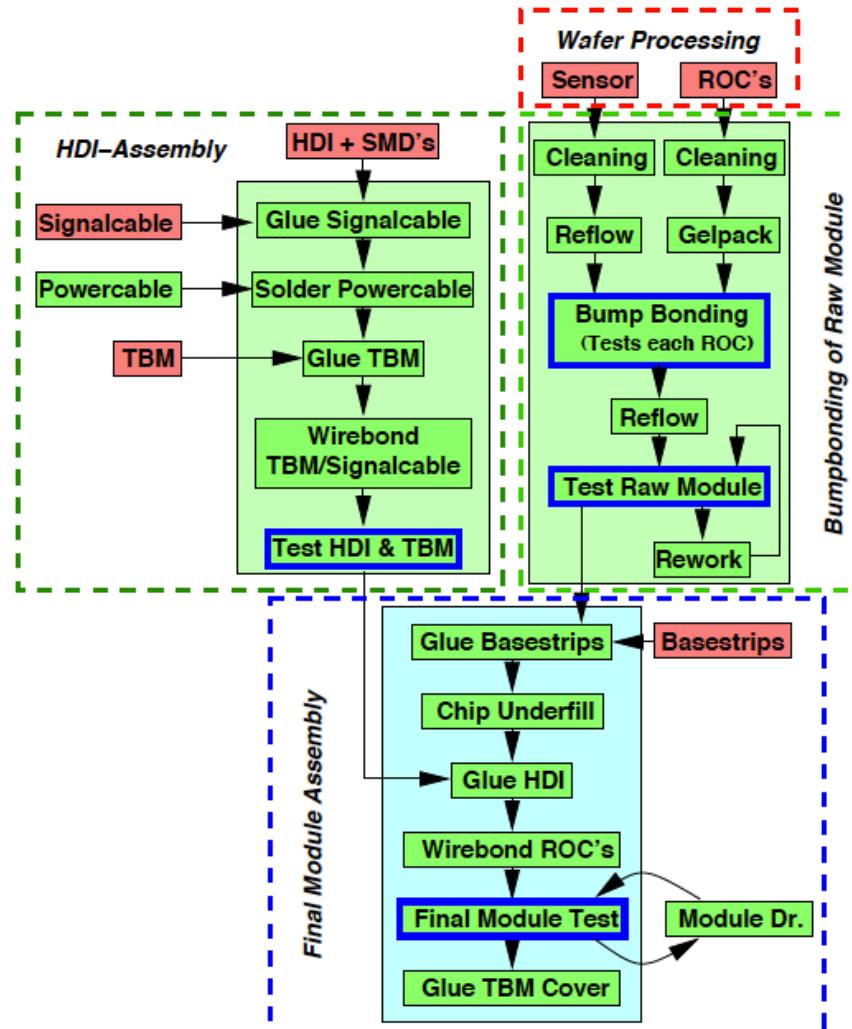
BPIX module production

ROC testing on wafer

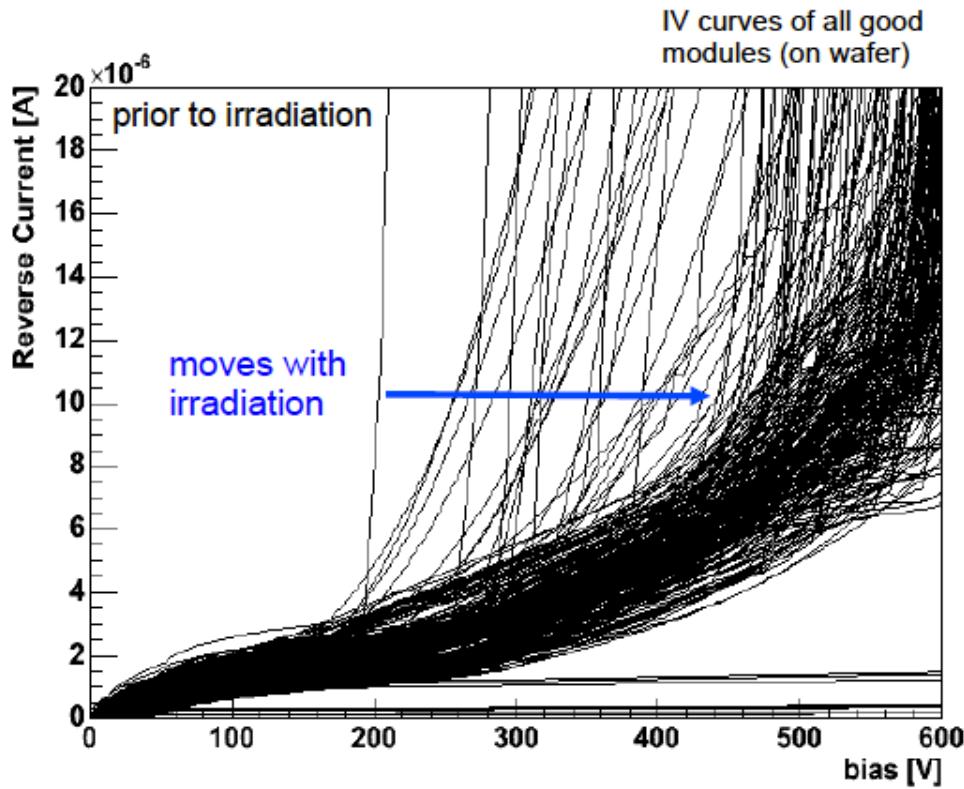


- ▶ Automated Suss Prober (8"):
- ▶ Test procedure
 - ▶ Threshold scan for all pixels
 - ▶ Test all DACs
 - ▶ Check all trim bits & mask
 - ▶ Check all data buffers
 - ▶ Check all time stamp buffers
 - ▶ Check power consumption
- ▶ 400K I2C commands to ROC
- ▶ Time 70 sec/chip, 1 wafer/day
- ▶ Average yield 74%

Flowchart of assembly procedure

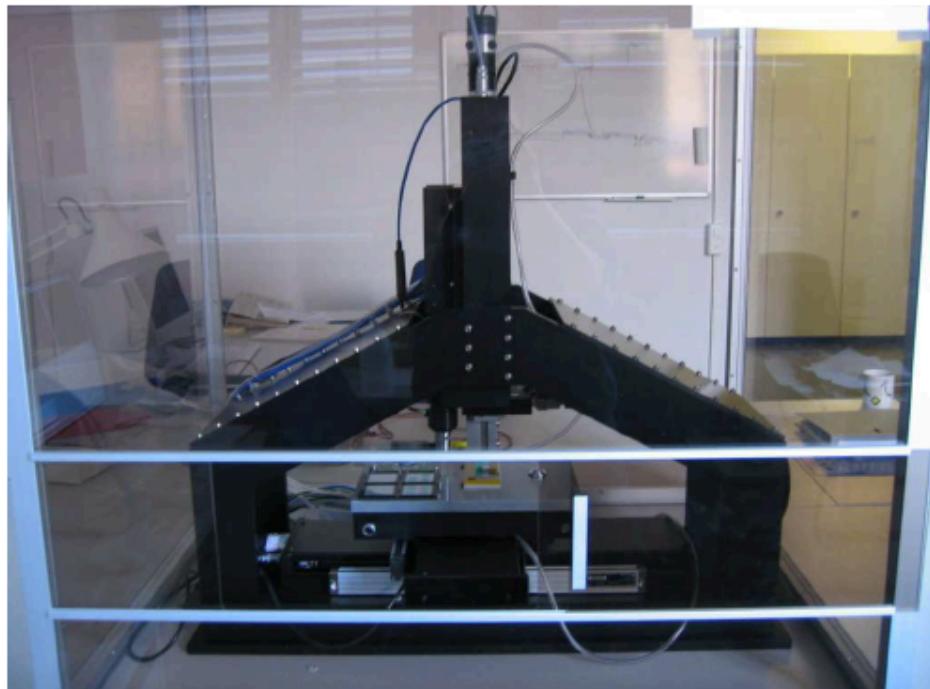


Si sensor testing

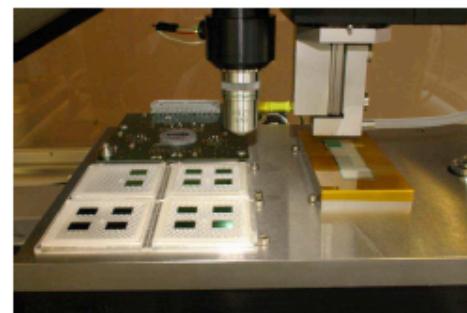


- ▶ 3 full modules / wafer
- ▶ Sensor specifications:
 - ▶ same ingot ($V_{depl} \sim 55 \div 65 V$)
 - ▶ $I(150V) < 2 \mu A$
 - ▶ $I(150V)/I(100V) < 2$
- ▶ Sensors lost:
 - ▶ 10% in bump deposition and cutting
 - ▶ 5% in module production

Si sensor to ROCs bump bonding



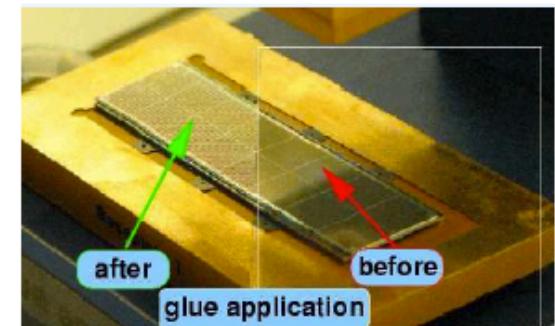
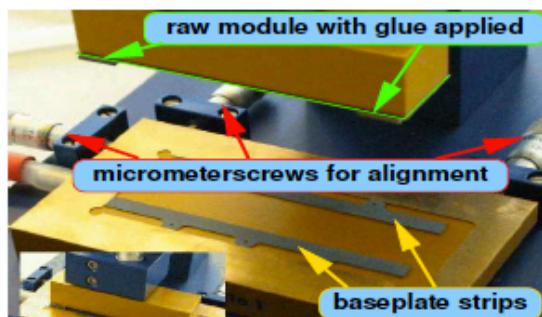
- ▶ Precision: $1 \div 2 \mu\text{m}$
- ▶ Production rate:
 - ▶ 6 modules / day + tests
 - ▶ automated: 1 hr/module
- ▶ Bare module test:
 - ▶ IV-curve
 - ▶ ROC functionality
 - ▶ bump yield
 - ▶ rework: 80% success



Pixel module assembly line in PSI

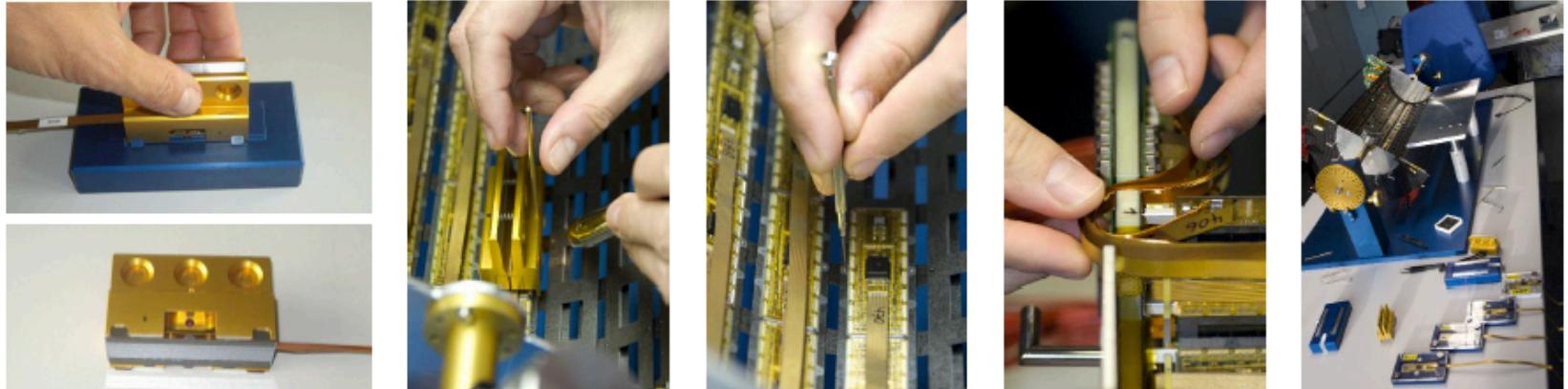


- ▶ Production rate:
 - ▶ 4 full + 2 half modules / day
 - ▶ or 6 full modules / day
- ▶ Three glueing steps:
 - ▶ glue basestrips to raw module
 - ▶ underfill sensor with glue
 - ▶ glue HDI to complete assembly
- ▶ Important: custom-made tools



At this step module testing happened

BPIX modules mounting in PSI

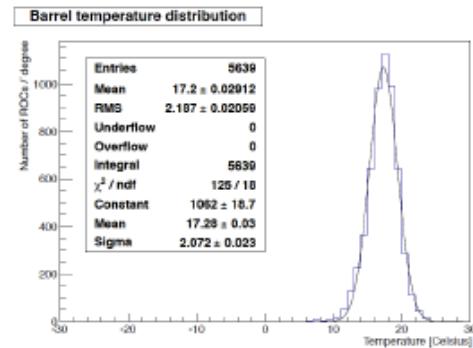
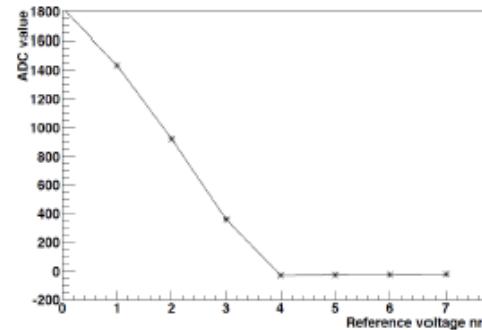
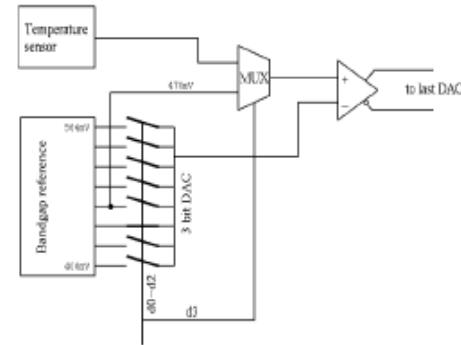


- ▶ 768 modules to mount
- ▶ Mounting tool is crucial
- ▶ Up to 60 modules / day
- ▶ Only 3 modules destroyed
- ▶ About 10 modules repaired:
 - ▶ broken wire bonds
 - ▶ bad connector
- ▶ Difficult object to survey
- ▶ Module position/ladder in 2D
- ▶ Pictures of 2 facing modules
- ▶ Optical pattern recognition SW
- ▶ Mean errors (z-dependent):
 - ▶ $r - \phi = 9.5 \mu\text{m}$, $z = 4.5 \mu\text{m}$
 - ▶ $\gamma = 240 \mu\text{rad}$

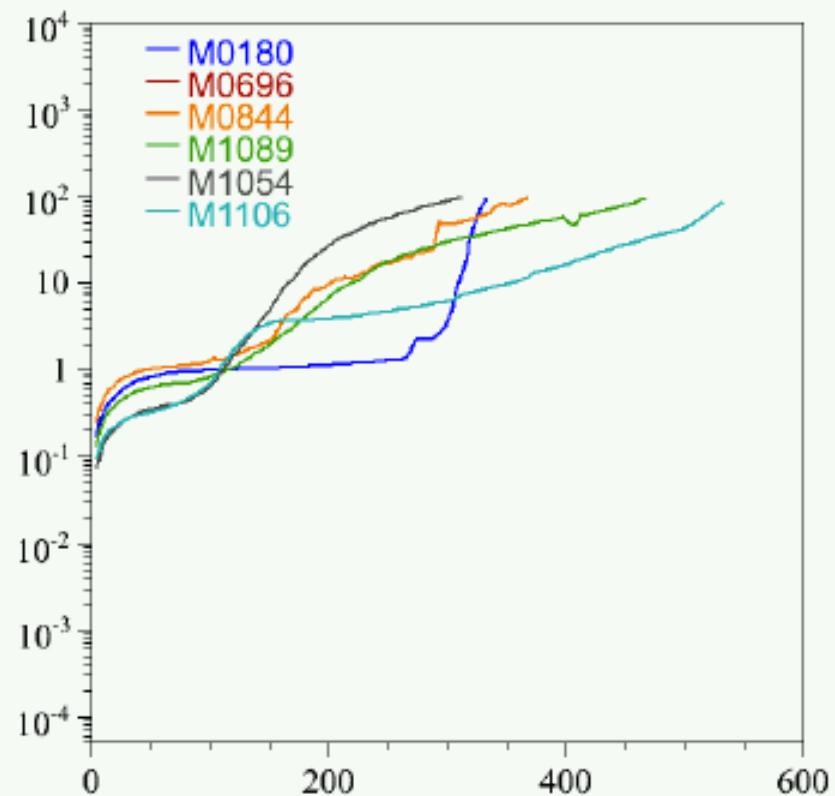
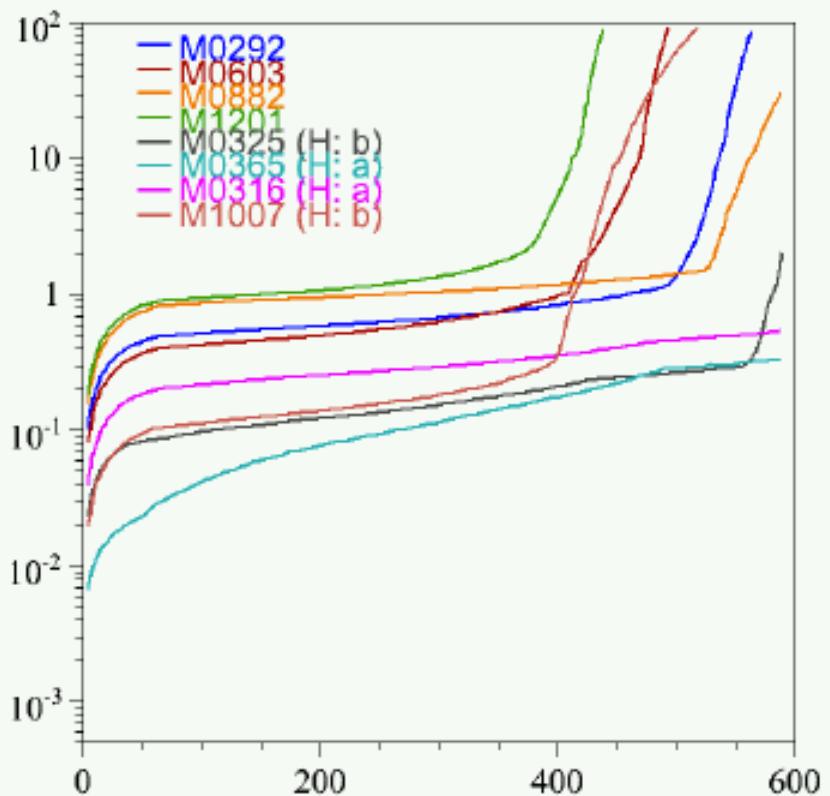
Backup slides

Temperature calibration

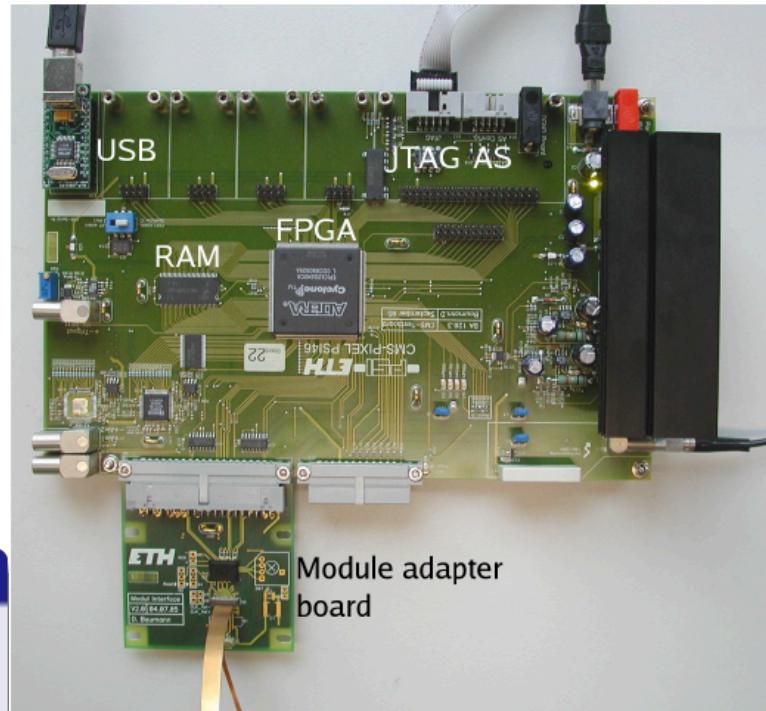
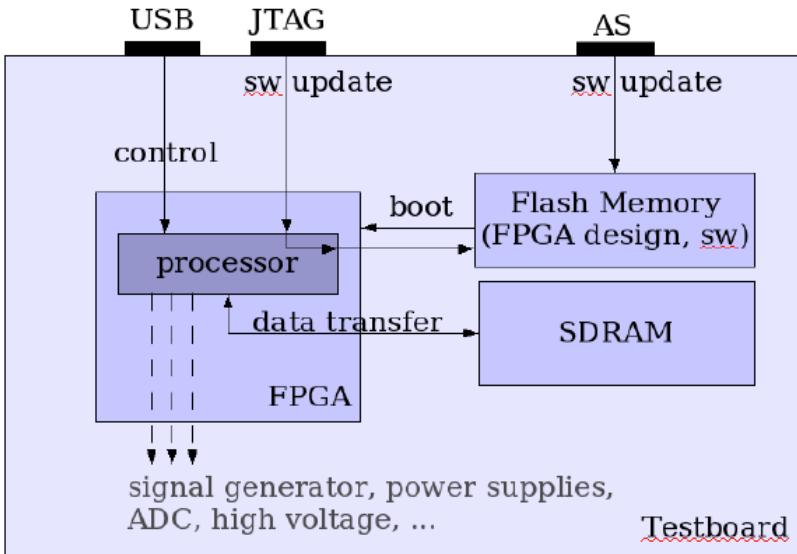
- ▶ Goal:
 - determine temperature dependent voltage (of T-sensor) at 2(3) temperatures and extract offset and slope of linear fit for every module
- ▶ What to do:
 - compare T dependent voltage to 8 reference T independent voltages
 - linearize measurements and make a fit
 - check that at different T interpolation works
- ▶ Where result will be used:
 - measurements of absolute temperature of modules in P5



Sensor leakage current, cont.



Test board



Components

- FPGA (field-programmable gate array): Cyclone (Altera)
- FPGA processor: Nios II, 32 Bit
- Memory: SDRAM, 64 MB
- Interfaces:
 - USB I (Universal serial bus)
 - JTAG (Joint Test Action Group)
 - AS (Active serial)
- Flash memory: 4 Mbit