



» **DATA SHEET**

(DOC No. HX8717-A-DS)

» **HX8717-A**

400x300CH EPD Source+Gate
Driver

Preliminary version 01 May, 2022

Revision History

May, 2022

Version	Date	Description of changes
01	2022/05/06	New setup.

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Preliminary Version 01

March, 2022

1. General Description

This driver is an Active Matrix EPD all-in-one driver with timing controller for ESL. The sources have 2-bit outputs per pixel to support white/black/color. The timing controller provides control signals for the source driver and gate drivers.

The DC-DC controller allows generate all necessary source and gate output voltage for VSPH(+15V and +3V to +15V)/VSPL(+3V to +15V),VSN(-15V and -3V to -15V),and VGH/VGL ($\pm 10V$, $\pm 15V$, $\pm 17V$, $\pm 20V$). The chip also includes an output buffer for the supply of the COM electrode (AC-VCOM or DC-VCOM). The system is configurable through a 3-wire/4-wire (SPI) serial interface.

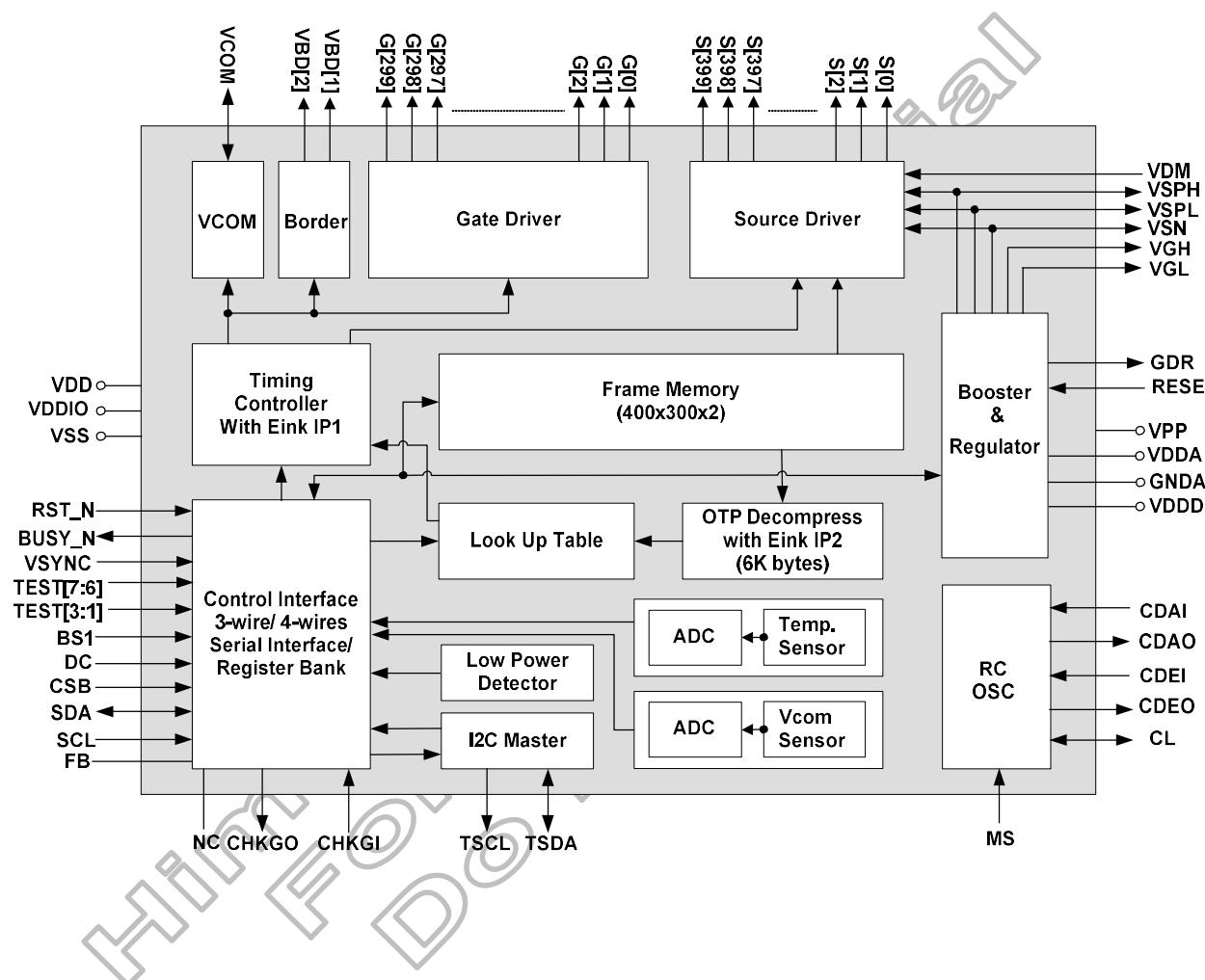
2. Features

- System-on-chip (**SOC**) for ESL
- Supply voltage VDD/VDDA/VDDIO: 2.3V to 3.6V
- Timing controller supports several resolutions
 - Up to 400 source x 300 gate resolution + 1 Border + 1 VCOM
 - 2-bit for white/black/color per pixel
- Cascade: 2 or more chips cascade mode
- Memory (**Max.**): 400x 300 x 2-bit SRAM
- 3-wire/4-wire (**SPI**) serial interface
 - Clock rate up to 10MHz
- Temperature sensor:
 - On-Chip: -25°C to 50°C ($\pm 2^\circ C$) / 8-bit status
- Support LPD, Low Power Detection (**VDD<2.5V**)
- OSC / PLL: On-chip RC oscillator
- VCOM
 - AC-VCOM / DC-VCOM (**by LUT**)
 - Support VCOM sensing (8-bit digital status)
- On-chip booster and regulator:
 - VGH/VGL: $\pm 10V$, $\pm 15V$, $\pm 17V$, $\pm 20V$ (**programmable**)
 - VSPH: +15V(mode1), +3V to+15V(mode2)
 - VSPL: +3V to+15V (mode1), +3V to+15V (mode2)
 - VSN: -15V (mode1), -3V to-15V (mode2)
- OTP: 6K-byte OTP for LUTs and settings
- Package: COG
- Source/Gate bump information
 - Bump pitch: $42\mu m \pm 3\mu m$
 - Bump space: $25\mu m \pm 3\mu m$
 - Bump surface: $1275\mu m^2$

3. Application

- E-tag application

4. Block Diagram



5. Pin Description

Pin name	I/O	Type	Description						
LDO									
VSPH	In/Out	Power	1 st positive source driver voltage.						
VSPL	In/Out	Power	2 nd positive source driver voltage.						
VSN	In/Out	Power	Negative source driver voltage.						
Control interface									
BS1	In	-	SPI interface bus selection. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>BS1</th><th>SPI interface</th></tr> <tr> <td>L</td><td>4-wire SPI</td></tr> <tr> <td>H</td><td>3-wire SPI</td></tr> </table>	BS1	SPI interface	L	4-wire SPI	H	3-wire SPI
BS1	SPI interface								
L	4-wire SPI								
H	3-wire SPI								
RST_N	In	(Pull-up)	Global reset pin. Low: Active, default RST_N=H. When RST_N becomes low, driver will reset. All register will reset to default value. Driver all function will disable. SD output and VCOM will base on previous condition. It may have two conditions: 0V or floating. The minimal width of RST_N=L is 100μs.						
BUSY_N	Out	-	IC busy flag. BUSY_N=H: Host side can send command/data to driver. BUSY_N=L: IC is busy, SD/VCOM is transforming.						
MS	In	-	Cascade setting pin. MS=H: Master chip. MS=L: Slave chip.						
CL	In/Out	-	Clock input/output pin. Master: Clock output. Slave: Clock input.						
CDAI	In	(Pull-down)	Cascade data pin. Leave it open if not used.						
CDAO	Out	-	Cascade data pin. Leave it open if not used.						
CDEI	In	(Pull-down)	Cascade data pin. Leave it open if not used.						
CDEO	Out	-	Cascade data pin. Leave it open if not used.						
TSCL	Out	-	Leave it open if not used.						
TSDA	In/Out	-	Leave it open if not used.						
MCU interface (SPI)									
CSB	In	(Pull-up)	Serial communication chip selection.						
SDA	In/Out	-	Serial communication data input/output. (3-wire/4-wire SPI)						
DC	In	-	Command/Data input. (4-wire SPI) DC=H: Data. DC=L: Command. Connect to VSS in 3-wire.						
SCL	In	-	Serial communication clock input.						
Output									
S[399:0]	Out	-	Source driver output signals.						
G[299:0]	Out	-	Gate driver output signals.						
VCOM	In/Out	-	a. (15V+(-VCOMDC)) V or (-15V+(-VCOMDC)) V b. (-VCOMDC) V c. Floating.						
VBD[2:1]	Out	-	Border output pins.						
Booster									
GDR	Out	-	N-MOS gate control for VGH Boost.						
RESE	In	-	Current sense input for control loop for VGH Boost.						
Check panel									
CHKGI	In	(Pull-down)	Check panel break input. Leave open if it is not used.						

Pin name	I/O	Type	Description
CHKGO	Out		Check panel break output. Leave open if it is not used.
Power			
VGH	In	Power	Positive gate voltage.
VGL	In	Power	Negative gate voltage.
VPP	In	Power	VPP for OTP programing. (8.25V)
VDM	In	Power	Analog ground.
VDDD	In	Power	Digital power. (1.5V)
VDDIO	In	Power	I/O power input.
VDDA	In	Power	Analog power input.
VDD	In	Power	Digital power input.
VSS	In	Power	Digital ground.
GNDA	In	Power	Analog ground.
Reserved			
VSYNC	Out	-	Reserved pins. Leave it floating.
TEST[3:1]	In	-	Reserved pins. Leave it floating or connected to VSS.
TEST[7:6]	Out	-	Reserved pins. Leave it floating.
FB	-	-	Keep it floating. Don't connect any power or signal to FB pin.
NC	-	-	Keep it floating.

6. Command Table

W/R: W: Write Cycle / R: Read Cycle

C/D: C: Command / D: Data

D[7:0]: -: Don't Care / #: Valid Data

Addr. ⁽¹⁾	Command ⁽²⁾	W/R ⁽³⁾	C/D	D[7:0] ⁽⁴⁾								Registers	Default	
00h	Panel setting register (PSR)	W	C	0	0	0	0	0	0	0	0	-	-	00h
		W	D	#	#	#	-	#	#	#	#	RES[1:0], PST_mode, UD, SHL, SHD_N, RST_N	0Fh	
		W	D	#	0	#	#	#	#	#	#	LUT_EN, FOPT, VCMZ, TS_AUTO, TIEG, NORG, VC_LUTZ	09h	
01h	Power setting register (PWR)	W	C	0	0	0	0	0	0	0	0	1	-	01h
		W	D	-	-	-	-	-	#	#	#	VSC_EN, VS_EN, VG_EN	0Fh	
		W	D	-	-	-	-	-	-	#	#	VGPN[1:0]	00h	
		W	D	-	#	#	#	#	#	#	#	(Power Mode0) VSPL[6:0]	00h	
		W	D	-	#	#	#	#	#	#	#	(Power Mode1) VSPH[6:0]	00h	
		W	D	-	#	#	#	#	#	#	#	(Power Mode1) VSN[6:0]	00h	
		W	D	-	#	#	#	#	#	#	#	(Power Mode01) VSPL[6:0]	00h	
02h	Power off (POF)	W	C	0	0	0	0	0	0	1	0	-	-	02h
		W	D	-	-	-	-	-	-	#	-	EDSE	00h	
03h	Power on/off sequence setting (POFS)	W	C	0	0	0	0	0	0	1	1	-	-	03h
		W	D	-	-	#	#	-	-	#	#	T_VDPG_OFF[1:0], T_VDS_OFF[1:0]	00h	
		W	D	#	#	#	#	#	#	#	#	VGH_LEN[3:0], VGH_EXT[3:0]	54h	
		W	D	#	#	#	#	#	#	#	#	XON_DLY[3:0], XON_LEN[3:0]	44h	
04h	Power on (PON)	W	C	0	0	0	0	0	1	0	0	-	-	04h
06h	booster soft start (BTST)	W	C	0	0	0	0	0	1	1	0	-	-	06h
		W	D	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17h	
		W	D	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17h	
		W	D	-	-	#	#	#	#	#	#	BT_PHC[5:0]	17h	
07h	Deep sleep (DSLP)	W	C	0	0	0	0	0	1	1	1	-	-	07h
		W	D	1	0	1	0	0	1	0	1	Check code	00h	
10h	Display start transmission (DTM)	W	C	0	0	0	1	0	0	0	0	Pixel data	10h	
		W	D	#	#	#	#	#	#	#	#	Pixel1, Pixel2, Pixel3, Pixel4	00h	
		W	D	-	:	:	:	-	:	:	:	:	00h	
		W	D	#	#	#	#	#	#	#	#	Pixel(n-3), Pixel(n-2), Pixel(n-1), Pixel(n)	00h	
		W	C	0	0	0	1	0	0	0	1	-	-	11h
11h	Data stop (DSP)	R	D	#	-	-	-	-	-	-	-	Data_flag	00h	
		W	C	0	0	0	1	0	0	1	0	-	-	12h
12h	Display refresh (DRF)	W	D	-	-	-	-	-	-	#	-	AC/DC VCOM	00h	
		W	C	0	0	0	1	0	0	1	0	-	-	17h
17h	Auto sequence (AUTO)	W	D	1	0	1	0	0	1	0	1	Check code	00h	
		W	C	0	0	0	1	0	1	1	1	-	-	30h
30h	PLL control (PLL)	W	C	0	0	1	1	0	0	0	0	-	-	02h
		W	D	-	-	-	-	#	#	#	#	Dyna, FR[2:0]	-	
40h	Temperature sensor command (TSC)	W	C	0	1	0	0	0	0	0	0	-	-	40h
		R	D	#	#	#	#	#	#	#	#	D[10:3] / TS[7:0]	00h	
		R	D	#	#	#	-	-	-	-	-	D[2:0]	00h	
41h	Temperature sensor enable (TSE)	W	C	0	1	0	0	0	0	0	1	-	-	41h
		W	D	#	-	-	-	#	#	#	#	TSE, TO[3:0]	00h	
50h	VCOM and data interval setting (CDI)	W	C	0	1	0	1	0	0	0	0	-	-	50h
		W	D	#	#	#	#	#	#	#	#	VBD[2:0], DDX, CDI[3:0]	97h	
51h	Lower power detection (LPD)	W	C	0	1	0	1	0	0	0	1	-	-	51h
		R	D	-	-	-	-	-	-	-	#	LPD	01h	

Reg ⁽¹⁾	Command ⁽²⁾	W/R ⁽³⁾	C/D	D[7:0] ⁽⁴⁾								Registers	Default
61h	Resolution setting (TRES)	W	C	0	1	1	0	0	0	0	1	-	61h
		W	D	-	-	-	-	-	#	#	#	VRES[9:8]	00h
		W	D	#	#	#	#	#	#	#	#	VRES[7:0]	00h
		W	D	-	-	-	-	-	#	#	#	VRES[9:8]	00h
		W	D	#	#	#	#	#	#	#	#	VRES[7:0]	00h
70h	Chip revision (REV)	W	C	0	1	1	1	0	0	0	0	-	70h
		R	D	0	0	0	0	0	1	1	0	REV	06h
		R	D	#	#	#	#	#	#	#	#	REV1[7:0]	05h
		R	D	#	#	#	#	#	#	#	#	REV2[7:0]	01h
80h	Auto measurement VCOM (AMV)	W	C	1	0	0	0	0	0	0	0	-	80h
		W	D	#	#	#	#	#	#	#	#	P[1:0], AMVT[1:0], AMVX, AMVS, AMV, AMVE	00h
		W	D	#	#	#	#	#	#	#	#	AMVP2	-
81h	VCOM value (VV)	W	C	1	0	0	0	0	0	0	1	-	81h
		R	D	-	#	#	#	#	#	#	#	VV[6:0]	00h
82h	VCOMDC setting (VDCS)	W	C	1	0	0	0	0	0	1	0	-	82h
		W	D	#	#	#	#	#	#	#	#	OTP_VCM ,VDCS[6:0]	00h
83h	Partial window (PTLW)	W	C	1	0	0	0	0	0	1	1	-	83h
		W	D	-	-	-	-	-	-	#	#	HRST[9:8]	00h
		W	D	#	#	#	#	#	#	0	0	HRST[7:0]	00h
		W	D	-	-	-	-	-	-	#	#	HRED[9:8]	00h
		W	D	#	#	#	#	#	#	1	1	HRED[7:0]	03h
		W	D	-	-	-	-	-	-	#	#	VRST[9:8]	00h
		W	D	#	#	#	#	#	#	#	#	VRST[7:0]	00h
		W	D	-	-	-	-	-	-	#	#	VRED[9:8]	00h
		W	D	#	#	#	#	#	#	#	#	VRED[7:0]	00h
		W	D	-	-	-	-	-	-	#	#	PMODE	00h
90h	Program mode (PGM)	W	C	1	0	0	1	0	0	0	0	-	90h
91h	Active program (APG)	W	C	1	0	0	1	0	0	0	1	-	91h
92h	Read OTP data (ROTP)	W	C	1	0	0	1	0	0	1	0	-	92h
		R	D	-	-	-	-	-	-	-	-	Dummy	00h
		R	D	#	#	#	#	#	#	#	#	OTP data of address 0	00h
		R	D	:	:	:	:	:	:	:	:	:	00h
		R	D	#	#	#	#	#	#	#	#	OTP data of address n	00h
E3h	Power saving (PWS)	W	C	1	1	1	0	0	0	1	1	-	E3h
		W	D	#	#	#	#	#	#	#	#	VCOM_W[3:0], SD_W[3:0]	00h
E4h	LVD voltage select (LVSEL)	W	C	1	1	1	0	0	1	0	0	-	E4h
		W	D	-	-	-	-	-	-	#	#	LVD_SEL[1:0]	03h

Note: (1) All other register addresses are invalid or reserved by Himax and should not be used.

(2) Commands are processed on the 'stop' condition of the interface.

(3) Registers marked 'W/R' can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.

(4) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.

6.1. Command description

W/R: W: Write Cycle / R: Read Cycle

C/D: C: Command / D: Data

D[7:0]: -: Don't Care

6.1.1. PSR (R00h): Panel setting register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
PSR	W	C	0	0	0	0	0	0	0	0	00h															
1 st parameter	W	D	RES [1:0]	PST_mode	-	UD	SHL	SHD_N	RST_N	0Fh																
2 nd parameter	W	D	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUT_Z	09h															
1st parameter:																										
<table border="1"> <thead> <tr> <th>RES[1:0]</th><th>Bit[7:6]: Resolution setting</th><th>Note</th></tr> </thead> <tbody> <tr> <td>00</td><td>Display resolution is 400x300</td><td>Default</td></tr> <tr> <td>01</td><td>Display resolution is 300x300</td><td>-</td></tr> <tr> <td>10</td><td>Display resolution is 256x256</td><td>-</td></tr> <tr> <td>11</td><td>Display resolution is 128x128</td><td>-</td></tr> </tbody> </table>												RES[1:0]	Bit[7:6]: Resolution setting	Note	00	Display resolution is 400x300	Default	01	Display resolution is 300x300	-	10	Display resolution is 256x256	-	11	Display resolution is 128x128	-
RES[1:0]	Bit[7:6]: Resolution setting	Note																								
00	Display resolution is 400x300	Default																								
01	Display resolution is 300x300	-																								
10	Display resolution is 256x256	-																								
11	Display resolution is 128x128	-																								
<table border="1"> <thead> <tr> <th>PST_mode</th><th>Bit[5]: Power switching operation mode</th><th>Note</th></tr> </thead> <tbody> <tr> <td>0</td><td>Power switching time in the period of frame scanning</td><td>Default</td></tr> <tr> <td>1</td><td>Power switching time in the external period before frame scanning</td><td>-</td></tr> </tbody> </table>												PST_mode	Bit[5]: Power switching operation mode	Note	0	Power switching time in the period of frame scanning	Default	1	Power switching time in the external period before frame scanning	-						
PST_mode	Bit[5]: Power switching operation mode	Note																								
0	Power switching time in the period of frame scanning	Default																								
1	Power switching time in the external period before frame scanning	-																								
<table border="1"> <thead> <tr> <th>UD</th><th>Bit[3]: UD select</th><th>Note</th></tr> </thead> <tbody> <tr> <td>0</td><td>Scan down, first line=G[n-1] → ... → G1 → Last line=G0</td><td>-</td></tr> <tr> <td>1</td><td>Scan up, first line=G[0] → G1 → ... → Last line=G[n-1]</td><td>Default</td></tr> </tbody> </table>												UD	Bit[3]: UD select	Note	0	Scan down, first line=G[n-1] → ... → G1 → Last line=G0	-	1	Scan up, first line=G[0] → G1 → ... → Last line=G[n-1]	Default						
UD	Bit[3]: UD select	Note																								
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<table border="1"> <thead> <tr> <th>SHL</th><th>Bit[2]: SHL select</th><th>Note</th></tr> </thead> <tbody> <tr> <td>0</td><td>Shift left, first data= S[n-1] → ... → S1 → Last data=S0</td><td>-</td></tr> <tr> <td>1</td><td>Shift right, first data=S0 → S1 → ... → Last data=S[n-1]</td><td>Default</td></tr> </tbody> </table>												SHL	Bit[2]: SHL select	Note	0	Shift left, first data= S[n-1] → ... → S1 → Last data=S0	-	1	Shift right, first data=S0 → S1 → ... → Last data=S[n-1]	Default						
SHL	Bit[2]: SHL select	Note																								
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LUT_EN	Bit[7]: LUT enable	Note																								
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TS_AUTO	Bit[3]: Temperature Auto	Note																								
0	NO effect	-																								

1	After system reset, Temperature Sensor will be activated automatically one time	Default
TIEG	Bit[2]: Tie to GND select	Note
0	NO effect	Default
1	After power off booster, VGL will be tied to GND	-
NORG	Bit[1]:NORG function	Note
0	NO effect	Default
1	After refreshing display, VCOM is tied to GND before power off	-
VC_LUTZ	Bit[0]: VCOM Hi-Z after DRF	Note
0	NO effect	-
1	After refreshing display, the output of VCOM is set to floating automatically	Default

Priority of VCOM setting: VCMZ > NORG > FOPT > VC_LUTZ.
FOPT setting is part of refreshing display.

- A. Non-select gate line keeps at VGL for DSP/DRF and AMV.
- B. Inactive source line follows LUTC for DSP/DRF.
- C. When SHD_N become low, Booster will turn off. Register and SRAM data will keep until VDD off. SD output and VCOM will base on previous condition. It may have two conditions: 0V or floating.
- D. When RST_N become low, driver will reset. All register will reset to default value. Driver all function will disable. Source/Gate/Border/VCOM will be released to floating.

6.1.2. PWR (R01h): Power setting register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWR	W	C	0	0	0	0	0	0	0	1	01h
1 st parameter	W	D	-	-	-	-	VSC_EN	VS_EN	VG_EN	0Fh	
2 nd parameter	W	D	-	-	-	-	-	-	VGPN [1:0]	00h	
3 rd parameter	W	D	-	(Power Mode0) VSPL [6:0]						00h	
4 th parameter	W	D	-	(Power Mode1) VSPH [6:0]						00h	
5 th parameter	W	D	-	(Power Mode1) VSN [6:0]						00h	
6 th parameter	W	D	-	(Power Mode1) VSPL [6:0]						00h	

The command define as follows:

1st parameter:

VSC_EN	Bit[2]:Source LV power selection	Note
0	External source LV power from VSPL pins	-
1	Internal DC/DC function for generate VSPL	Default

VS_EN	Bit[1]:Source power selection	Note
0	External source power from VSPH/ VSN pins	-
1	Internal DC/DC function for generate VSPH/ VSN	Default

VG_EN	Bit[1]:Gate power selection	Note
0	External gate power from VGH/VGL pins	-
1	Internal DCDC function for generate VGH/VGL	Default

2nd parameter:

VGPN [1:0]	Bit[1:0]:VGPN voltage ⁽¹⁾ level	Note
00	VGH=20V, VGL=-20V	Default
01	VGH=17V, VGL=-17V	-
10	VGH=15V, VGL=-15V	-
11	VGH=10V, VGL=-10V	-

Notes: (1) If VGPN voltage is set to ±17V, ±15V, ±10V, IC will auto correct source voltage as follows.

- A. VGH-VSPH/VSPL ≥ 2V.
- B. VGL-VSN ≥ -2V.

Description

For example:

	Symbol	Voltage setting	Real voltage
Voltage	VGH	+10V	+10V
	VGL	-10V	-10V
	VSPH	+15V	+8V
	VSN	-15V	-8V
	VSPL	+5V	+5V
	VCOMH	+15V+(-2V)	+8V+(-2V)
	VCOML	-15V+(-2V)	-8V+(-2V)
	VCOMDC	-2V	-2V

Power mode 0:

VSPH = 15V (0x78)

VSN = -15V (0x78)

3rd Parameter: Internal VSPL power selection (Default value: 0000000) (3V~15V)

Power mode 1:

4th & 6th Parameter: Internal VSPH/VSPL power selection (Default value: 0000000) (3V~15V)

5th Parameter: Internal VSN power selection (Default value: 0000000) (-3V~15V)

Bit[6:0]	Internal VSPH/VSPL Power	Internal VSN Power	Bit[6:0]	Internal VSPH/VSPL Power	Internal VSN Power
0000000	3 V	-3 V	0110010	8.0 V	-8.0 V
0000001	3.1 V	-3.1 V	:	:	:
0000010	3.2 V	-3.2 V	0111100	9.0 V	-9.0 V
0000011	3.3 V	-3.3 V	:	:	:

	0000100	3.4 V	-3.4 V	1000110	10.0 V	-10.0 V
	0000101	3.5 V	-3.5 V	:	:	:
	0000110	3.6 V	-3.6 V	1010000	11.0 V	-11.0 V
	0000111	3.7 V	-3.7 V	:	:	:
	0001000	3.8 V	-3.8 V	1011010	12.0 V	-12.0 V
	0001001	3.9 V	-3.9 V	:	:	:
	0001010	4.0 V	-4.0 V	1100100	13.0 V	-13.0 V
	0001011	4.1 V	-4.1 V	:	:	:
	0001100	4.2 V	-4.2 V	1101110	14.0 V	-14.0 V
	0001101	4.3 V	-4.3 V	:	:	:
	0001110	4.4 V	-4.4 V	1111000	15.0 V	-15.0 V
	0001111	4.5 V	-4.5 V	-	-	-
	0010000	4.6 V	-4.6 V	-	-	-
	:	:	:	-	-	-
	0010100	5.0 V	-5.0 V	-	-	-
	:	:	:	-	-	-
	0011110	6.0 V	-6.0 V	-	-	-
	:	:	:	-	-	-
	0101000	7.0 V	-7.0 V	-	-	-
	:	:	:	-	-	-

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6.1.3. POF (R02h): Power off command register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
POF	W	C	0	0	0	0	0	0	1	0	02h									
1 st parameter	W	D	-	-	-	-	-	-	-	EDSE	00h									
Description	<p>The command define as follows: After the power off command, the driver will power off based on power off sequence. After the power off command, BUSY_N signal will become '0'. This command will turn off charge pump, T-con, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned off. SD output and VCOM will base on previous condition. It may have two conditions:0V or floating</p> <table border="1"> <thead> <tr> <th>EDSE</th><th>Bit[0]:EPD Discharge Trigger</th><th>Note</th></tr> </thead> <tbody> <tr> <td>0</td><td>Disable EPD discharge</td><td>Default</td></tr> <tr> <td>1</td><td>Enable EPD discharge</td><td>-</td></tr> </tbody> </table>											EDSE	Bit[0]:EPD Discharge Trigger	Note	0	Disable EPD discharge	Default	1	Enable EPD discharge	-
EDSE	Bit[0]:EPD Discharge Trigger	Note																		
0	Disable EPD discharge	Default																		
1	Enable EPD discharge	-																		

6.1.4. POFS (R03h): Power on/off sequence setting register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																												
POFS	W	C	0	0	0	0	0	0	1	1	03h																																																												
1 st parameter	W	D	-	-	T_VDPG_OFF[1:0]	-	-	-	T_VDS_OFF[1:0]	-	00h																																																												
2 nd parameter	W	D	-	VGH_LEN[3:0]	-	-	VGH_EXT[3:0]	-	-	-	54h																																																												
3 rd parameter	W	D	-	XON_DLY[3:0]	-	-	XON_LEN[3:0]	-	-	-	44h																																																												
The 2 nd ~3 rd parameters are only for EPD discharge function. (EDSE) 1 st parameter and 2 nd ~3 rd parameter would not happen at the same time.																																																																							
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6.1.5. PON (R04h): Power on command register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PON	W	C	0	0	0	0	0	1	0	0	04h
Description	The command define as follows: After power on command, the driver will power ON base on Power ON sequence. After power on command and all power sequence are ready (Based on PWR command), then BUSY_N signal will become 1. This command only active when BUSY_N=1.										

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6.1.6. BTST (R06h): VGH booster soft start command register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BTST	W	C	0	0	0	0	0	1	1	0	06h
1 st parameter	W	D	BT_PHA[7:6]		BT_PHA[5:3]		BT_PHA[2:0]				17h
2 nd parameter	W	D	BT_PHB[7:6]		BT_PHB[5:3]		BT_PHB[2:0]				17h
3 rd parameter	W	D	-	-	BT_PHC[5:0]		BT_PHC[2:0]				17h

The command define as follows:

1st parameter:

BT_PHA[7:6]	Bit[7:6]:Soft start period of phase A	Note
00	10ms	Default
01	20ms	-
10	30ms	-
11	40ms	-

BT_PHA[5:3]	Bit[5:3]:Driving strength of phase A	Note
000	Strength 1	-
001	Strength 2	-
010	Strength 3	Default
011	Strength 4	-
100	Strength 5	-
101	Strength 6	-
110	Strength 7	-
111	Strength 8	Strongest

BT_PHA[2:0]	Bit[2:0]:Min. off time setting of GDR in phase A	Note
000	0.27μs	-
001	0.34μs	-
010	0.40μs	-
011	0.54μs	-
100	0.80μs	-
101	1.54μs	-
110	3.34μs	-
111	6.58μs	Default

Description

2nd parameter:

BT_PHB[7:6]	Bit[7:6]:Soft start period of phase B	Note
00	10ms	Default
01	20ms	-
10	30ms	-
11	40ms	-

BT_PHB[5:3]	Bit[5:3]:Driving strength of phase B	Note
000	Strength 1	-
001	Strength 2	-
010	Strength 3	Default
011	Strength 4	-
100	Strength 5	-
101	Strength 6	-
110	Strength 7	-
111	Strength 8	Strongest

BT_PHB[2:0]	Bit[2:0]:Min. off time setting of GDR in phase B	Note
000	0.27μs	-
001	0.34μs	-
010	0.40μs	-
011	0.54μs	-
100	0.80μs	-
101	1.54μs	-
110	3.34μs	-
111	6.58μs	Default

3rd parameter:

BT_PHC[5:3]	Bit[5:3]:Driving strength of phase C	Note
000	Strength 1	-
001	Strength 2	-
010	Strength 3	Default
011	Strength 4	-
100	Strength 5	-
101	Strength 6	-
110	Strength 7	-
111	Strength 8	Strongest

BT_PHC[2:0]	Bit[2:0]:Min. off time setting of GDR in phase C	Note
000	0.27μs	-
001	0.34μs	-
010	0.40μs	-
011	0.54μs	-
100	0.80μs	-
101	1.54μs	-
110	3.34μs	-
111	6.58μs	Default

6.1.7. DS LP (R07h): Deep sleep register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DSLP	W	C	0	0	0	0	0	1	1	1	07h
1 st parameter	W	D	0	0	0	0	0	0	0	0	00h
Description	The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset. The only one parameter is a check code, the command would be executed if check code=0xA5.										

6.1.8. DTM (R10h): Data start transmission register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																			
DTM	W	C	0	0	0	1	0	0	0	0	10h																																			
1 st parameter	W	D	Pixel1		Pixel2		Pixel3		Pixel4		00h																																			
:	W	D	:		:		:		:		00h																																			
M th parameter	W	D	Pixel(n-3)		Pixel(n-2)		Pixel(n-1)		Pixel(n)		00h																																			
Description	<p>The command define as follows: This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Data Refresh command. Then the chip will start to send data/VCOM for panel.</p> <p>Pixel[1~n][1:0] (2-bit mode):</p> <table border="1"> <thead> <tr> <th colspan="5">Source output look up table</th> </tr> <tr> <th>Image Data</th> <th colspan="2">DDX=1 (Default)</th> <th colspan="2">DDX=0</th> </tr> <tr> <th>Pixel[1:0]</th> <th>Gray level select</th> <th>IP output LUT select</th> <th>Gray level select</th> <th>IP output LUT select</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Gray 0</td> <td>ogray00</td> <td>Gray 3</td> <td>ogray03</td> </tr> <tr> <td>01</td> <td>Gray 1</td> <td>ogray01</td> <td>Gray 2</td> <td>ogray02</td> </tr> <tr> <td>10</td> <td>Gray 2</td> <td>ogray02</td> <td>Gray 1</td> <td>ogray01</td> </tr> <tr> <td>11</td> <td>Gray 3</td> <td>ogray03</td> <td>Gray 0</td> <td>ogray00</td> </tr> </tbody> </table> <p>Data mapping example: When DDX=1, Pixel[1:0]=01->Gray level select= Gray 1, follow LUT data output from IP output port "ogray01" When DDX=0, Pixel[1:0]=11->Gray level select= Gray 0, follow LUT data output from IP output port "ogray00"</p>											Source output look up table					Image Data	DDX=1 (Default)		DDX=0		Pixel[1:0]	Gray level select	IP output LUT select	Gray level select	IP output LUT select	00	Gray 0	ogray00	Gray 3	ogray03	01	Gray 1	ogray01	Gray 2	ogray02	10	Gray 2	ogray02	Gray 1	ogray01	11	Gray 3	ogray03	Gray 0	ogray00
Source output look up table																																														
Image Data	DDX=1 (Default)		DDX=0																																											
Pixel[1:0]	Gray level select	IP output LUT select	Gray level select	IP output LUT select																																										
00	Gray 0	ogray00	Gray 3	ogray03																																										
01	Gray 1	ogray01	Gray 2	ogray02																																										
10	Gray 2	ogray02	Gray 1	ogray01																																										
11	Gray 3	ogray03	Gray 0	ogray00																																										

6.1.9. DSP (R11h): Data stop command register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX						
DSP	W	C	0	0	0	1	0	0	0	1	11h						
1 st parameter	R	D	Data_flag	-	-	-	-	-	-	-	00h						
The command define as follows: To stop data transmission, this command must be issued to check the Data_flag.																	
1st parameter: <table border="1"> <thead> <tr> <th>Data_flag</th> <th>Bit[7]:Data flag of receiving user data</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Driver didn't receive all the data.</td> </tr> <tr> <td>1</td> <td>Driver has already received all the one frame data.</td> </tr> </tbody> </table>											Data_flag	Bit[7]:Data flag of receiving user data	0	Driver didn't receive all the data.	1	Driver has already received all the one frame data.	
Data_flag	Bit[7]:Data flag of receiving user data																
0	Driver didn't receive all the data.																
1	Driver has already received all the one frame data.																
After "Data stop" (R11h) commands and when Data_flag=1, BUSY_N signal will become 0 and the refreshing of panel starts.																	
This command only active when BUSY_N=1.																	

6.1.10. DRF (R12h): Display refresh command register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DRF	W	C	0	0	0	1	0	0	1	0	12h
1 st parameter	W	D	-	-	-	-	-	-	-	AC/DC VCOM	00h
Description	<p>The command define as follows: While user sent this command, driver will refresh display (Data/VCOM) base on SRAM data and LUT.</p> <p>AC/DC VCOM: AC, DC VCOM select. 0: AC VCOM, VCOM will follow LUTC when updating image. (Default) 1: DC VCOM, VCOM will always be VCOMDC when updating image.</p> <p>After display refresh command, BUSY_N signal will become 0.</p> <p>This command only active when BUSY_N=1.</p>										

6.1.11. AUTO (R17h): Auto sequence register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
AUTO	W	C	0	0	0	1	0	1	1	1	17h
1 st parameter	W	D	0	0	0	0	0	0	0	0	00h
Description	The command define as follows: The command is only for LUT from register mode (R00h LUT_EN=1) only. The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP. AUTO (0x17) + Code (0xA5) = (PON → DRF → POF) AUTO (0x17) + Code (0xA7) = (PON → DRF → POF → DSLP)										

6.1.12. PLL (R30h): PLL control register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PLL	W	C	0	0	1	1	0	0	0	0	30h
1 st parameter	W	D	-	-	-	-	Dyna	FR[2:0]	FR[2:0]	FR[2:0]	02h
The command define as follows:											
The command controls the PLL clock frequency. The PLL structure must support the following frame rates:											
Description	Dyna	Dynamic frame rate								Note	
	0	Disable								Default	
	1	Enable								-	
	FR[2:0]	Bit[2:0]:Frame rate								Note	
	000	12.5Hz								-	
	001	25Hz								-	
	010	50Hz								Default	
	011	65Hz								-	
	100	75Hz								-	
	101	85Hz								-	
	110	100Hz								-	
	111	120Hz								-	

6.1.13. TSC (R40h): Temperature sensor command register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TSC	W	C	0	1	0	0	0	0	0	0	40h
1 st parameter	R	D	TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0	00h
2 nd parameter	R	D	-	-	-	-	-	-	-	-	00h

The command define as follows:
This command indicates the temperature value.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

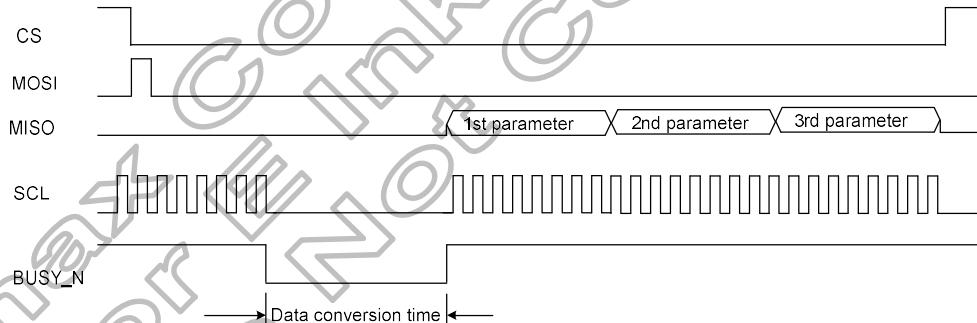
1st parameter:

TS[7:0]/D[10:3]	Temperature (°C)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
...	...
1111_1110	-2
1111_1111	-1

TS[7:0]/D[10:3]	Temperature (°C)
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
...	...
0011_1011	59
0011_1100	60

Description

The BUSY_N behavior of other type SPI communication is the same.

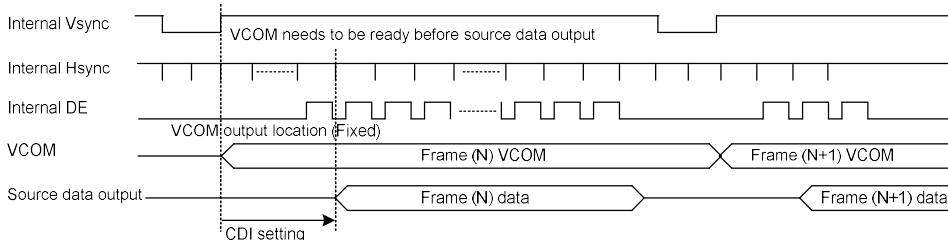


This command only active when BUSY_N=1.

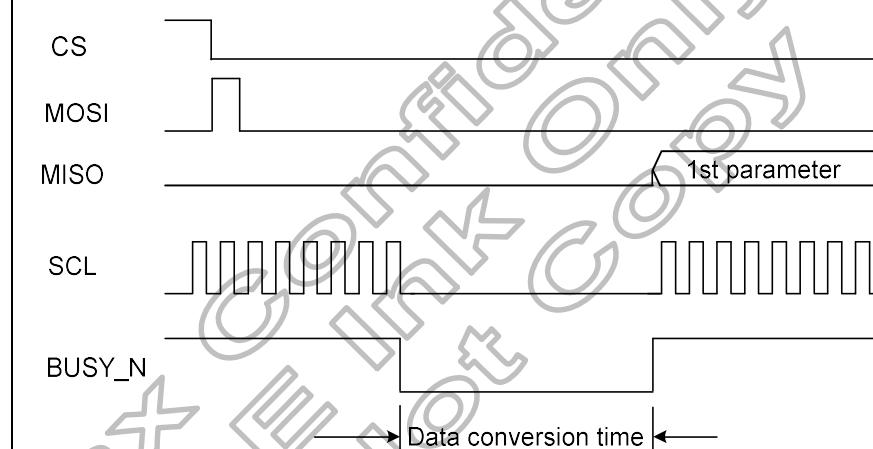
6.1.14. TSE (R41h): Temperature sensor enable register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX																												
TSE	W	C	0	1	0	0	0	0	0	1	41h																												
1 st parameter	W	D	TSE	-	-	-			TO[3:0]		00h																												
<p>The command define as follows: This command indicates the driver IC temperature sensor enable and calibration function.</p> <p>1st parameter:</p> <table border="1"> <thead> <tr> <th>TSE</th><th>Bit[7]:TSE</th><th>Note</th></tr> </thead> <tbody> <tr> <td>0</td><td>Enable internal temperature sensor</td><td>Default</td></tr> <tr> <td>1</td><td>Disable internal temperature sensor.</td><td>-</td></tr> </tbody> </table> <p>TO[3:0]: Reserve one temperature offset TO[3:0] for calibration (Internal temperature sensor)</p> <ol style="list-style-type: none"> 1. TO[3]: Mean '+' or '-', while 0 is '+'; 1 is '-'. 2. TO[2:0]: Mean temperature offset value. <p>Temperature offset:</p> <table border="1"> <thead> <tr> <th>TO[3:0]</th><th>Bit[3:0]:Temperature level</th><th>TO[3:0]</th><th>Bit[3:0]:Temperature level</th></tr> </thead> <tbody> <tr> <td>0000</td><td>+ 0°C (Default)</td><td>1000</td><td>- 8°C</td></tr> <tr> <td>0001</td><td>+ 1°C</td><td>1001</td><td>- 7°C</td></tr> <tr> <td>:</td><td>:</td><td>:</td><td>:</td></tr> <tr> <td>0111</td><td>+ 7°C</td><td>1111</td><td>- 1°C</td></tr> </tbody> </table>											TSE	Bit[7]:TSE	Note	0	Enable internal temperature sensor	Default	1	Disable internal temperature sensor.	-	TO[3:0]	Bit[3:0]:Temperature level	TO[3:0]	Bit[3:0]:Temperature level	0000	+ 0°C (Default)	1000	- 8°C	0001	+ 1°C	1001	- 7°C	:	:	:	:	0111	+ 7°C	1111	- 1°C
TSE	Bit[7]:TSE	Note																																					
0	Enable internal temperature sensor	Default																																					
1	Disable internal temperature sensor.	-																																					
TO[3:0]	Bit[3:0]:Temperature level	TO[3:0]	Bit[3:0]:Temperature level																																				
0000	+ 0°C (Default)	1000	- 8°C																																				
0001	+ 1°C	1001	- 7°C																																				
:	:	:	:																																				
0111	+ 7°C	1111	- 1°C																																				

6.1.15. CDI (R50h): VCOM and Data interval setting register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																						
CDI	W	C	0	1	0	1	0	0	0	0	50h																																																																																																						
1 st parameter	W	D	VBD[2:0]			DDX	CDI[3:0]				97h																																																																																																						
The command define as follows: This command can set 2 kinds of parameters: 1. VCOM to data output interval (CDI) 2. Border pin output. VBD[2:0]/DDX: Border data selection. (From LUT) This register will make border pin output being mapped to a certain gray scale.																																																																																																																	
<table border="1"> <thead> <tr> <th>DDX</th><th>VBD[2:0]</th><th>Gray level</th><th>Note</th></tr> </thead> <tbody> <tr> <td rowspan="5">0</td><td>000</td><td>Floating</td><td>-</td></tr> <tr><td>001</td><td>Gray 3</td><td>-</td></tr> <tr><td>010</td><td>Gray 2</td><td>-</td></tr> <tr><td>011</td><td>Gray 1</td><td>-</td></tr> <tr><td>100</td><td>Gray 0</td><td>-</td></tr> <tr> <td rowspan="5">1</td><td>000</td><td>Gray 0</td><td>-</td></tr> <tr><td>001</td><td>Gray 1</td><td>-</td></tr> <tr><td>010</td><td>Gray 2</td><td>-</td></tr> <tr><td>011</td><td>Gray 3</td><td>-</td></tr> <tr><td>100</td><td>Floating</td><td>Default</td></tr> </tbody> </table> Border output voltage level: The level selection is based on mapping LUT data with VCOM shift added. E.g.: Gray 1 waveform is mapping to 15V, VCOM value being set as -2V, the real output on border pin shall be $15V + (-2V) = 13V$. Border output will follow FOPT definition being defined in R00h.												DDX	VBD[2:0]	Gray level	Note	0	000	Floating	-	001	Gray 3	-	010	Gray 2	-	011	Gray 1	-	100	Gray 0	-	1	000	Gray 0	-	001	Gray 1	-	010	Gray 2	-	011	Gray 3	-	100	Floating	Default																																																																		
DDX	VBD[2:0]	Gray level	Note																																																																																																														
0	000	Floating	-																																																																																																														
	001	Gray 3	-																																																																																																														
	010	Gray 2	-																																																																																																														
	011	Gray 1	-																																																																																																														
	100	Gray 0	-																																																																																																														
1	000	Gray 0	-																																																																																																														
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	010	Gray 2	-																																																																																																														
	011	Gray 3	-																																																																																																														
	100	Floating	Default																																																																																																														
CDI[3:0] : This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept as a default value (Count by Hsync).																																																																																																																	
<table border="1"> <thead> <tr> <th>Bit[3]</th><th>Bit[2]</th><th>Bit[1]</th><th>Bit[0]</th><th>VCOM and data interval</th><th>Note</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>17Hsync</td><td>-</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>16Hsync</td><td>-</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>15Hsync</td><td>-</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>14Hsync</td><td>-</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>13Hsync</td><td>-</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>12Hsync</td><td>-</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>11Hsync</td><td>-</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>10Hsync</td><td>Default</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>9Hsync</td><td>-</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>8Hsync</td><td>-</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>7Hsync</td><td>-</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>6Hsync</td><td>-</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>5Hsync</td><td>-</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>4Hsync</td><td>-</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>3Hsync</td><td>-</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>2Hsync</td><td>-</td></tr> </tbody> </table>												Bit[3]	Bit[2]	Bit[1]	Bit[0]	VCOM and data interval	Note	0	0	0	0	17Hsync	-	0	0	0	1	16Hsync	-	0	0	1	0	15Hsync	-	0	0	1	1	14Hsync	-	0	1	0	0	13Hsync	-	0	1	0	1	12Hsync	-	0	1	1	0	11Hsync	-	0	1	1	1	10Hsync	Default	1	0	0	0	9Hsync	-	1	0	0	1	8Hsync	-	1	0	1	0	7Hsync	-	1	0	1	1	6Hsync	-	1	1	0	0	5Hsync	-	1	1	0	1	4Hsync	-	1	1	1	0	3Hsync	-	1	1	1	1	2Hsync	-
Bit[3]	Bit[2]	Bit[1]	Bit[0]	VCOM and data interval	Note																																																																																																												
0	0	0	0	17Hsync	-																																																																																																												
0	0	0	1	16Hsync	-																																																																																																												
0	0	1	0	15Hsync	-																																																																																																												
0	0	1	1	14Hsync	-																																																																																																												
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0	1	1	1	10Hsync	Default																																																																																																												
1	0	0	0	9Hsync	-																																																																																																												
1	0	0	1	8Hsync	-																																																																																																												
1	0	1	0	7Hsync	-																																																																																																												
1	0	1	1	6Hsync	-																																																																																																												
1	1	0	0	5Hsync	-																																																																																																												
1	1	0	1	4Hsync	-																																																																																																												
1	1	1	0	3Hsync	-																																																																																																												
1	1	1	1	2Hsync	-																																																																																																												
																																																																																																																	

6.1.16. LPD (R51h): Lower power detection register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
LPD	W	C	0	1	0	1	0	0	0	1	51h									
1 st parameter	R	D	-	-	-	-	-	-	-	LPD	01h									
The command define as follows:																				
This command indicates the input power condition. Host can read this data to understand the battery condition.																				
LPD:																				
LPD=1: System input power is normal.																				
LPD=0: Low power input. (VDD < 2.5V, selected by LVD_SEL[1:0] in command LVSEL)																				
1st parameter:																				
<table border="1"> <thead> <tr> <th>LPD</th><th>Bit[0]:LPD</th><th>Note</th></tr> </thead> <tbody> <tr> <td>0</td><td>Low power input</td><td>-</td></tr> <tr> <td>1</td><td>Normal status</td><td>Default</td></tr> </tbody> </table>												LPD	Bit[0]:LPD	Note	0	Low power input	-	1	Normal status	Default
LPD	Bit[0]:LPD	Note																		
0	Low power input	-																		
1	Normal status	Default																		
Description	CS																			
	MOSI																			
	MISO										1 st parameter									
	SCL																			
	BUSY_N																			
																				
This command only active when BUSY_N = "1".																				

6.1.17. TRES (R61h): Resolution setting register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TRES	W	C	0	1	1	0	0	0	0	1	61h
1 st parameter	W	D	-	-	-	-	-	-	HRES[9:8]	00h	
2 nd parameter	W	D			HRES[7:2]				HRES[1] HRES[0]	00h	
3 rd parameter	W	D	-	-	-	-	-	-	VRES[9:8]	00h	
4 th parameter	W	D				VRES[7:0]				00h	
Description	<p>(HRES ≤ 400, VRES ≤ 300)</p> <p>No matter what value being set in D1 and D0 of 1st parameter (HRES[1] and HRES[0]), the register shall be kept as 0.HRES[1:0]=00b.</p> <p>The command define as follows: When using register: Horizontal display resolution=HRES. Vertical display resolution=VRES. HRES[9]=0 and VRES[9]=0</p> <p>Channel disable calculation: GD: First G active=G0; LAST active GD=First active + VRES[7:0] – 1 SD: First active channel=S0; LAST active SD=First active + HRES[7:2]*4 – 1</p> <p>E.g.: SD176xGD296 GD: First G active=G0 LAST active GD=0 + 296 – 1=295 SD: First active channel=S0 LAST active SD=0 + 176 – 1=175.</p>										

6.1.18. REV (R70h): Chip revision register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
REV	W	C	0	1	1	1	0	0	0	0	70h	
1 st parameter	R	D	0	0	0	0	0	1	1	0	06h	
2 nd parameter	R	D					REV1[7:0]				05h	
3 rd parameter	R	D					REV2[7:0]				01h	
Description	The command define as follows:											
	2nd parameter:											
	REV1[7:0]		Bit[7:0]: E Ink internal number									
	3rd parameter:		REV2[7:0] Bit[7:0]: Increased each revision:									
(Default value is defined by customer.)												

6.1.19. AMV (R80h): Auto measurement VCOM register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																		
AMV	W	C	1	0	0	0	0	0	0	0	80h																																																																		
1 st parameter	W	D	P[1:0]		AMVT[1:0]	AMVX	AMVS	AMV	AMVE	00h																																																																			
2 nd parameter	W	D			AMVP2					-																																																																			
The command define as follows: This command indicates the IC status. Host can read this data to understand the IC status.																																																																													
1st parameter: <table border="1"> <thead> <tr> <th>P[1:0]</th><th>Bit[7:6]:The sensing points of sampling time</th><th>Note</th></tr> </thead> <tbody> <tr> <td>00</td><td>2</td><td>Default</td></tr> <tr> <td>01</td><td>4</td><td>-</td></tr> <tr> <td>10</td><td>8</td><td>-</td></tr> <tr> <td>11</td><td>16</td><td>-</td></tr> </tbody> </table> <p>Sampling time=The last quarter of sensing time(T). VCOM=Average of N points. N=2,4,8,16.</p> <table border="1"> <thead> <tr> <th>AMVT[1:0]</th><th>Bit[5:4]:The sensing time of VCOM detection</th><th>Note</th></tr> </thead> <tbody> <tr> <td>00</td><td>5s</td><td>Default</td></tr> <tr> <td>01</td><td>10s</td><td>-</td></tr> <tr> <td>10</td><td>15s</td><td>-</td></tr> <tr> <td>11</td><td>20s</td><td>-</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th>AMVX</th><th>Bit[3]:XON setting for all Gate ON of AMV</th><th>Note</th></tr> </thead> <tbody> <tr> <td>0</td><td>Gate normally scan during Auto Measure VCOM period</td><td>Default</td></tr> <tr> <td>1</td><td>All Gate ON during Auto Measure VCOM period</td><td>-</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th>AMVS</th><th>Bit[2]:AMVS setting for Source output of AMV</th><th>Note</th></tr> </thead> <tbody> <tr> <td>0</td><td>Source output 0V during auto measure VCOM period</td><td>Default</td></tr> <tr> <td>1</td><td>Source output VSPL during auto measure VCOM period</td><td>-</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th>AMV</th><th>Bit[1]:Analogy signal</th><th>Note</th></tr> </thead> <tbody> <tr> <td>0</td><td>Get VCOM value by R81H</td><td>Default</td></tr> <tr> <td>1</td><td>Gate scan only. Measure VCOM externally by probing the VCOM pad.</td><td>-</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th>AMVE</th><th>Bit[0]:Auto measure VCOM setting</th><th>Note</th></tr> </thead> <tbody> <tr> <td>0</td><td>Auto measure VCOM disable</td><td>Default</td></tr> <tr> <td>1</td><td>Auto measure VCOM enable</td><td>-</td></tr> </tbody> </table> 2nd parameter: Auto Measurement VCOM would be executed only if AMVP2 =0x00. This command only active when BUSY_N=1.												P[1:0]	Bit[7:6]:The sensing points of sampling time	Note	00	2	Default	01	4	-	10	8	-	11	16	-	AMVT[1:0]	Bit[5:4]:The sensing time of VCOM detection	Note	00	5s	Default	01	10s	-	10	15s	-	11	20s	-	AMVX	Bit[3]:XON setting for all Gate ON of AMV	Note	0	Gate normally scan during Auto Measure VCOM period	Default	1	All Gate ON during Auto Measure VCOM period	-	AMVS	Bit[2]:AMVS setting for Source output of AMV	Note	0	Source output 0V during auto measure VCOM period	Default	1	Source output VSPL during auto measure VCOM period	-	AMV	Bit[1]:Analogy signal	Note	0	Get VCOM value by R81H	Default	1	Gate scan only. Measure VCOM externally by probing the VCOM pad.	-	AMVE	Bit[0]:Auto measure VCOM setting	Note	0	Auto measure VCOM disable	Default	1	Auto measure VCOM enable	-
P[1:0]	Bit[7:6]:The sensing points of sampling time	Note																																																																											
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01	4	-																																																																											
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0	Auto measure VCOM disable	Default																																																																											
1	Auto measure VCOM enable	-																																																																											

6.1.20. VV (R81h): VCOM value register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX																	
VV	W	C	1	0	0	0	0	0	0	1	81h																	
1 st parameter	R	D	-	VV[6:0]																								
Description	The command define as follows: This command gets VCOM value.																											
	1st parameter: <table border="1"> <thead> <tr> <th>VV[6:0]</th> <th>Bit[6:0]:VCOM value</th> <th>Note</th> </tr> </thead> <tbody> <tr> <td>0000000</td> <td>0V</td> <td>Default</td> </tr> <tr> <td>0000001</td> <td>-0.05V</td> <td>-</td> </tr> <tr> <td>0000010</td> <td>-0.10V</td> <td>-</td> </tr> <tr> <td>:</td> <td>:</td> <td>-</td> </tr> <tr> <td>1010000</td> <td>-4.00V</td> <td>-</td> </tr> </tbody> </table>											VV[6:0]	Bit[6:0]:VCOM value	Note	0000000	0V	Default	0000001	-0.05V	-	0000010	-0.10V	-	:	:	-	1010000	-4.00V
VV[6:0]	Bit[6:0]:VCOM value	Note																										
0000000	0V	Default																										
0000001	-0.05V	-																										
0000010	-0.10V	-																										
:	:	-																										
1010000	-4.00V	-																										

6.1.21. VDCS (R82h): VCM_DC setting register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX																					
VDCS	W	C	1	0	0	0	0	0	1	0	82h																					
1 st parameter	W	D	OTP_VCM				VDCS[6:0]				00h																					
The command define as follows: This command set the VCOMDC value. Driver will base on this value for VCOM. 1st parameter:																																
<table border="1"> <thead> <tr> <th>OTP_VCM</th><th>Bit[7]:Follow OTP VCOM value in OTP mode</th><th>Note</th></tr> </thead> <tbody> <tr> <td>0</td><td>IP output value</td><td>Default</td></tr> <tr> <td>1</td><td>From the setting register</td><td>-</td></tr> </tbody> </table>												OTP_VCM	Bit[7]:Follow OTP VCOM value in OTP mode	Note	0	IP output value	Default	1	From the setting register	-												
OTP_VCM	Bit[7]:Follow OTP VCOM value in OTP mode	Note																														
0	IP output value	Default																														
1	From the setting register	-																														
<table border="1"> <thead> <tr> <th>VDCS[6:0]</th><th>Bit[6:0]:VCOM value</th><th>Note</th></tr> </thead> <tbody> <tr> <td>0000000</td><td>0V</td><td>Default</td></tr> <tr> <td>0000001</td><td>-0.05V</td><td>-</td></tr> <tr> <td>0000010</td><td>-0.10V</td><td>-</td></tr> <tr> <td>:</td><td>:</td><td>-</td></tr> <tr> <td>1010000</td><td>-4.00V</td><td>-</td></tr> <tr> <td>Others</td><td>-4.00V</td><td>-</td></tr> </tbody> </table>												VDCS[6:0]	Bit[6:0]:VCOM value	Note	0000000	0V	Default	0000001	-0.05V	-	0000010	-0.10V	-	:	:	-	1010000	-4.00V	-	Others	-4.00V	-
VDCS[6:0]	Bit[6:0]:VCOM value	Note																														
0000000	0V	Default																														
0000001	-0.05V	-																														
0000010	-0.10V	-																														
:	:	-																														
1010000	-4.00V	-																														
Others	-4.00V	-																														

6.1.22. PTLW (R83h): Partial window

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLW	W	C	1	0	0	0	0	0	1	1	83h
1 st parameter	W	D	-	-	-	-	-	-	HRST[9:8]	00h	
2 nd parameter	W	D			HRST[7:2]				HRST[1:0]	00h	
3 rd parameter	W	D	-	-	-	-	-	-	HRED[9:8]	00h	
4 th parameter	W	D			HRED[7:2]				HRED[1:0]	03h	
5 th parameter	W	D	-	-	-	-	-	-	VRST[9:8]	00h	
6 th parameter	W	D			VRST[7:0]					00h	
7 th parameter	W	D	-	-	-	-	-	-	VRED[9:8]	00h	
8 th parameter	W	D			VRED[7:0]					00h	
9 th parameter	W	D	-	-	-	-	-	-	-	PMODE	00h
Description	<p>The command define as follows: The register is indicating the window before user start to transmit data.</p> <p>PMODE: 0: Disable partial mode (Default) 1: Enable partial mode</p> <p>HRST[9:0]: Horizontal start address. HRED[9:0]: Horizontal end address. VRST[9:0]: Vertical start address. VRED[9:0]: Vertical end address.</p> <p>No matter HRST[1:0] value being filled, it's always 00b. No matter HRED[1:0] value being filled, it's always 11b HRST[9]=0 and HRED[9]=0 VRST[9]=0 and VRED[9]=0</p> <p>Gates scan both inside and outside of the partial window.</p>										

6.1.23. PGM (R90h): Program mode

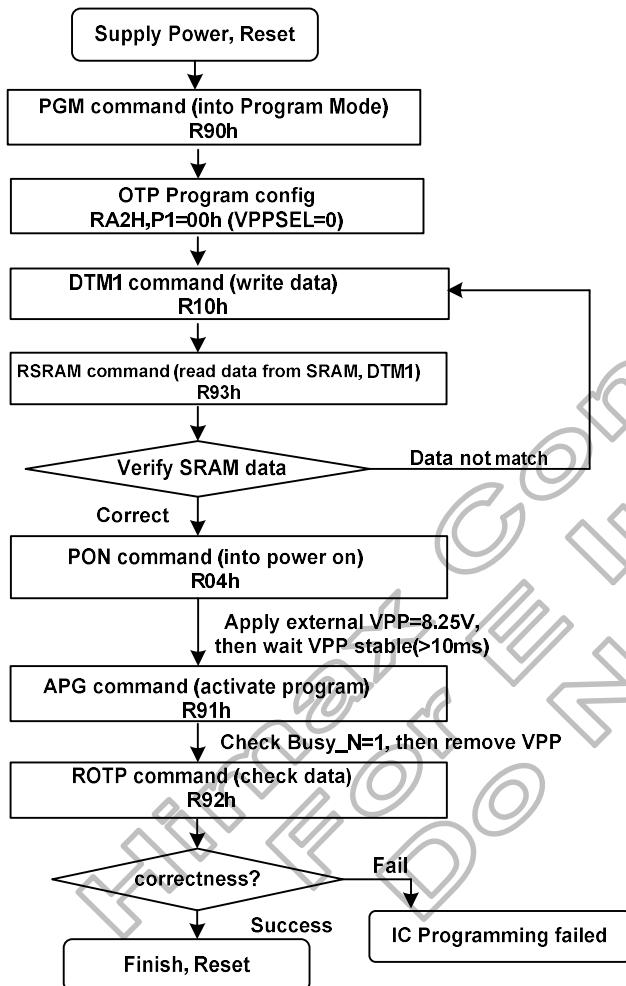
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PGM	W	C	1	0	0	1	0	0	0	0	90h
Description	After this command is issued, the chip would enter the program mode. After the programming procedure completed, a hardware reset is necessary for leaving program mode.										

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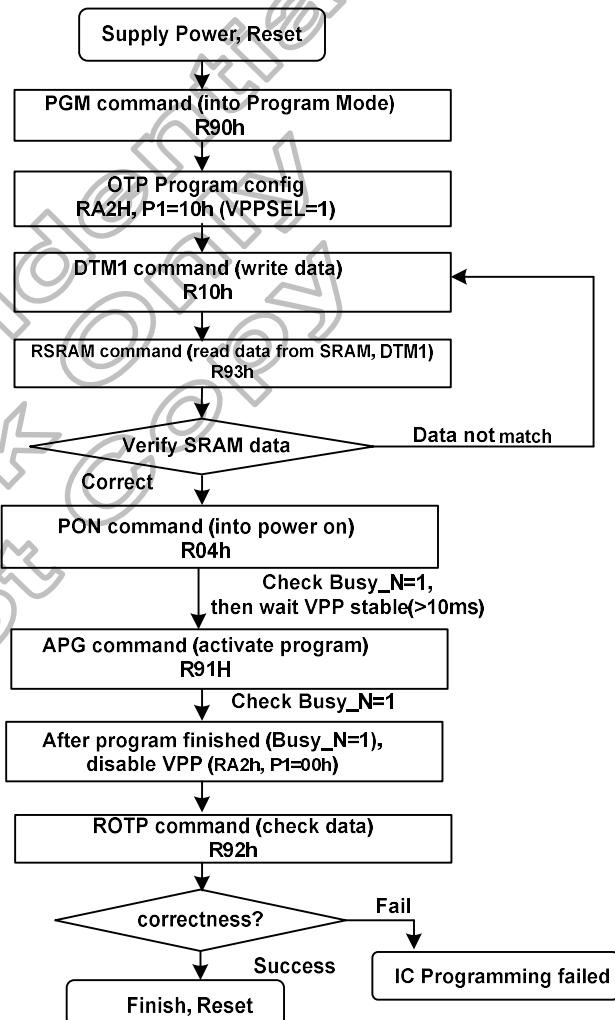
6.1.24. APG (R91h): Active program

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
APG	W	C	1	0	0	1	0	0	0	1	91h
Description	After this command is transmitted, the programming stage machine would be activated. The BUSY_N flag would fall to 0 until the programming is completed. This command only active when BUSY_N=1.										

OTP programming flow (External power)



OTP programming flow (Internal power)

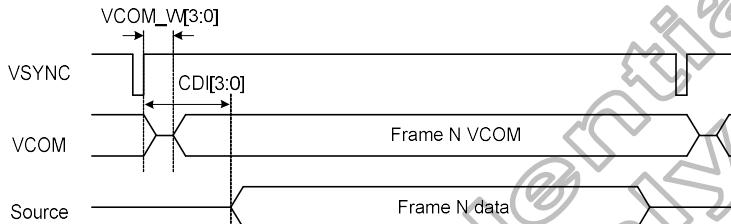
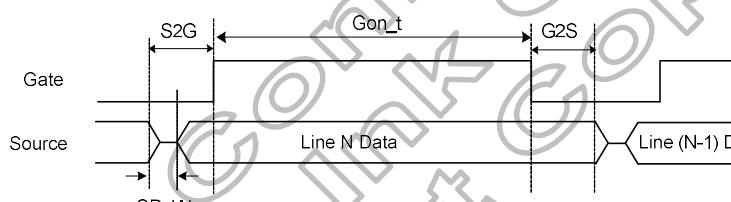


6.1.25. ROTP (R92h): Read OTP data

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
ROTP	W	C	1	0	0	1	0	0	1	0	92h
1 st parameter	R	D					Dummy				00h
2 nd parameter	R	D					The data of address 0 in the OTP				00h
3 rd parameter	R	D					The data of address 1 in the OTP				00h
:	R	D					:				00h
(n+1) th parameter	R	D					The data of address (n-1) in the OTP				00h
(n+2) th parameter	R	D					The data of address (n) in the OTP				00h
Description	The command is used for reading the content of OTP for checking the data of programming.										

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6.1.26. PWS (RE3h): Power saving register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
PWS	W	C	1	1	1	0	0	0	1	1	E3h								
1 st parameter	W	D	VCOM_W[3:0]				SD_W[3:0]				00h								
This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.																			
VCOM_W[3:0]: VCOM power saving width (Unit=Line period).  <p>The diagram shows the timing of VCOM and Source signals relative to VSYNC. The VCOM signal transitions from negative to positive at the start of Frame N. The Source signal also transitions at the same time. The width of the pulse is labeled VCOM_W[3:0]. The time interval between the start of the transition and the end of the pulse is labeled CDI[3:0].</p>																			
SD_W[3:0]: Source power saving width (Unit=500ns), SD_W<= S2G  <p>The diagram shows the timing of Gate and Source signals relative to Line N Data. The Gate signal transitions from low to high at the start of Line N Data. The Source signal transitions at the same time. The width of the pulse is labeled SD_W. The time interval between the start of the transition and the end of the pulse is labeled Gon_t. The time interval between the end of the pulse and the start of the next pulse is labeled G2S.</p>																			

6.1.27. LVSEL(RE4h): LVD voltage select register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
LVSEL	W	C	1	1	1	0	0	1	0	0	E4h
1 st parameter	W	D	-	-	-	-	-	-	LVD_SEL[1:0]	03h	
LVD_SEL: Low power voltage selection.											
Description	LVD_SEL[1:0]	LVD value		Note							
	00	< 2.2V									-
	01	< 2.3V									-
	10	< 2.4V									-
	11	< 2.5V									Default

6.2. HOST interface

HX8717-A provides 3-wire/4-wire serial interface for command and display data transferred from the MCU. The serial interface supports 8-bit mode. Data can be input/output by clocks while the chip is active (**CSB=L**). While input, data are written in order from MSB at the clock rising edge. When too many parameters are input, the chip accepts only defined parameters, and ignores undefined ones.

BS1	Interface	CSB	DC	SCL	SDA
H	3-wire SPI	Available	Fix to VSS	Available	Available
L	4-wire SPI	Available	Available	Available	Available

6.2.1. 3-wire SPI format

Data / Command is recognized with the first bit transferred. Data are transferred in the unit of 9-bit. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 9-bit. (The serial counter is reset at the rising edge of the CSB signal.)

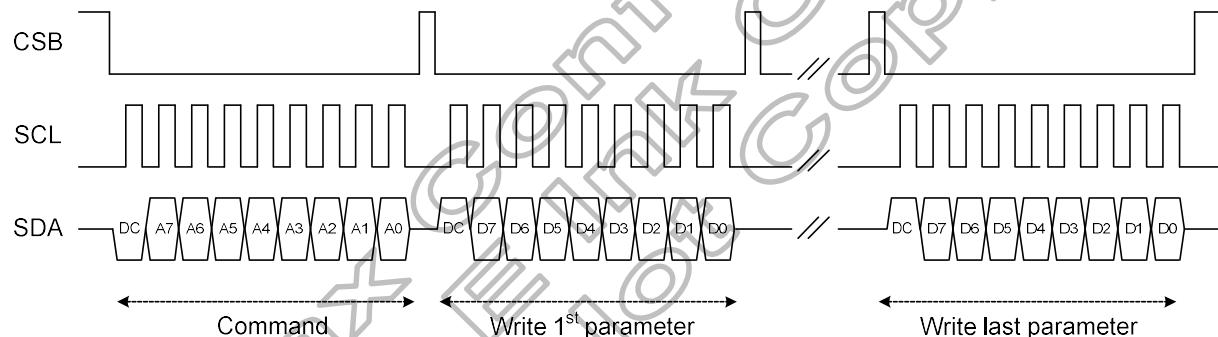


Figure 6.1: 3-wire SPI write parameter (timing type 1)

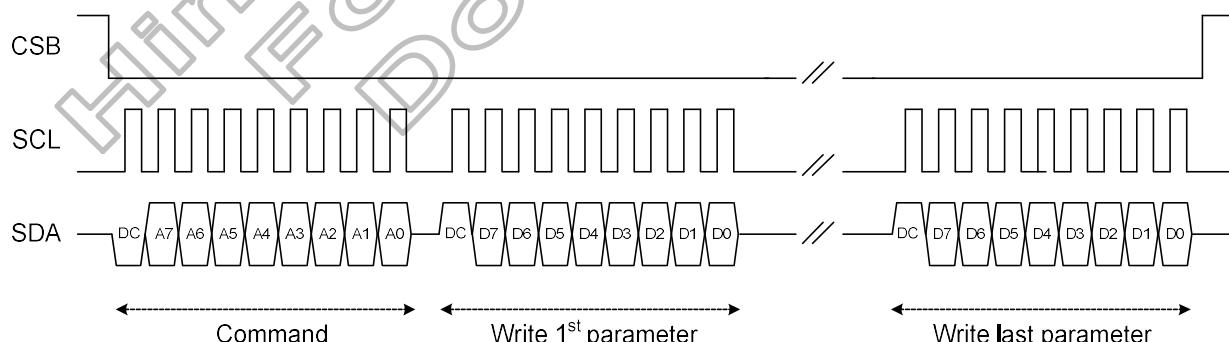


Figure 6.2: 3-wire SPI write parameter (timing type 2)

The MSB bit of data will be output at SDA pin after the 1st SCL falling edge, if the 1st input data at SDA is high. Only in the case of OTP data read, the 1st packet of output data are dummy data.

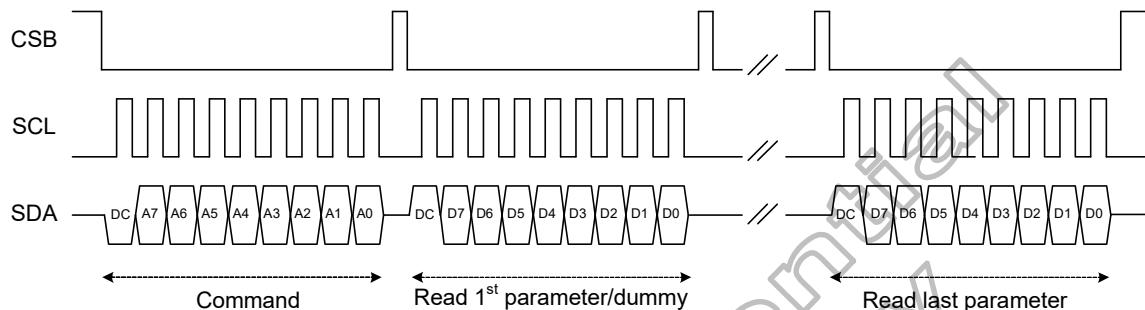


Figure 6.3: 3-wire SPI read parameter (timing type 1)

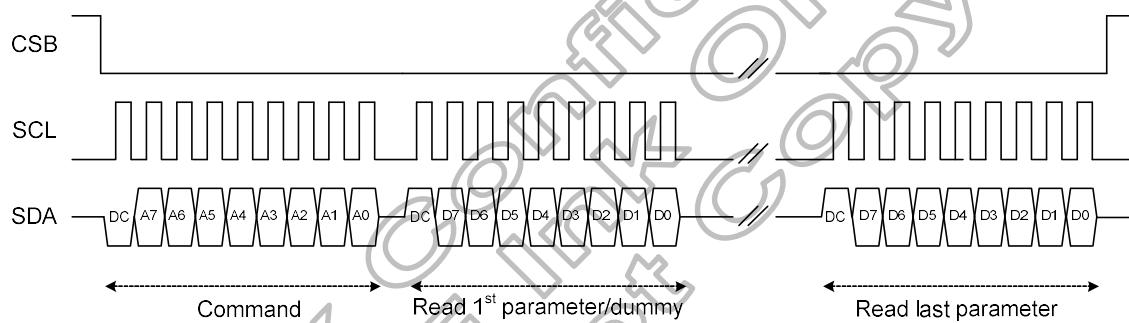


Figure 6.4: 3-wire SPI read parameter (timing type 2)

6.2.2. 4-wire SPI format

Data / Command is recognized with DC pin. Data are transferred in the unit of 8-bit. To prevent malfunction due to noise, it is recommended to set the CSB signal to high every 8-bit. (The serial counter is reset at the rising edge of the CSB signal.)

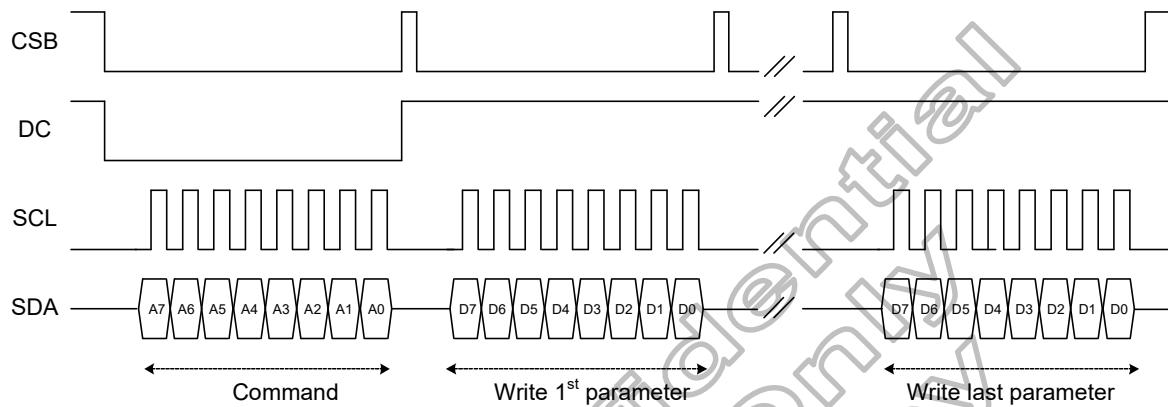


Figure 6.5: 4-wire SPI write parameter (timing type 1)

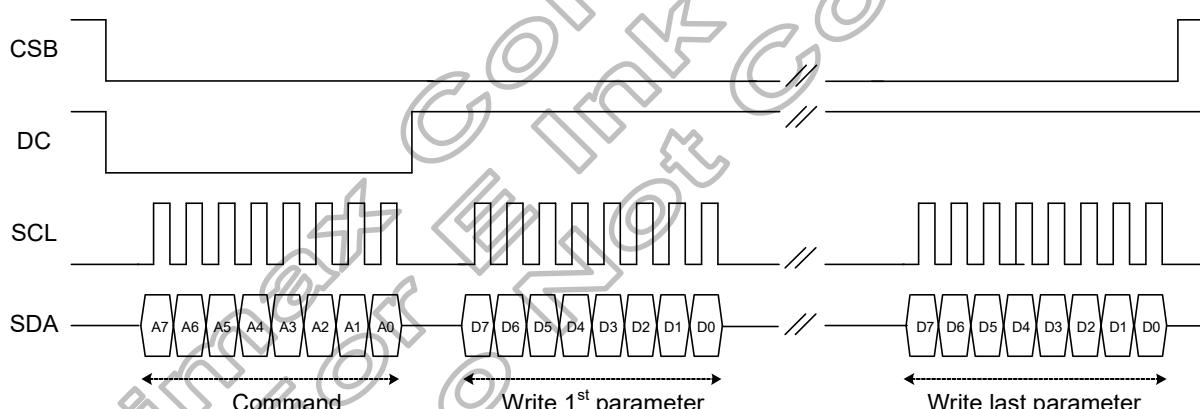


Figure 6.6: 4-wire SPI write parameter (timing type 2)

The MSB bit of data will be output at SDA pin after the CSB falling edge, if DC pin is high. Only in the case of OTP data read, the 1st packet of output data are dummy data.

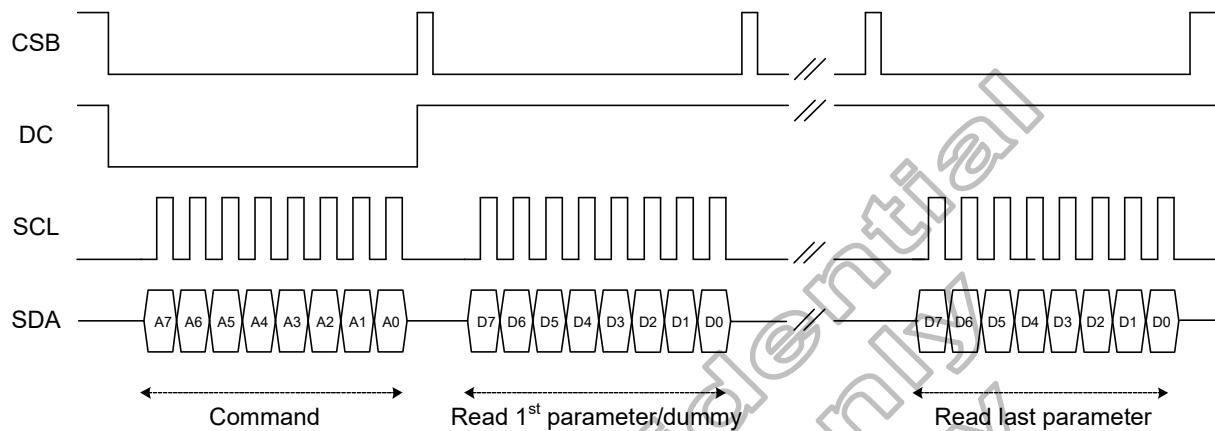


Figure 6.7: 4-wire SPI read parameter (timing type 1)

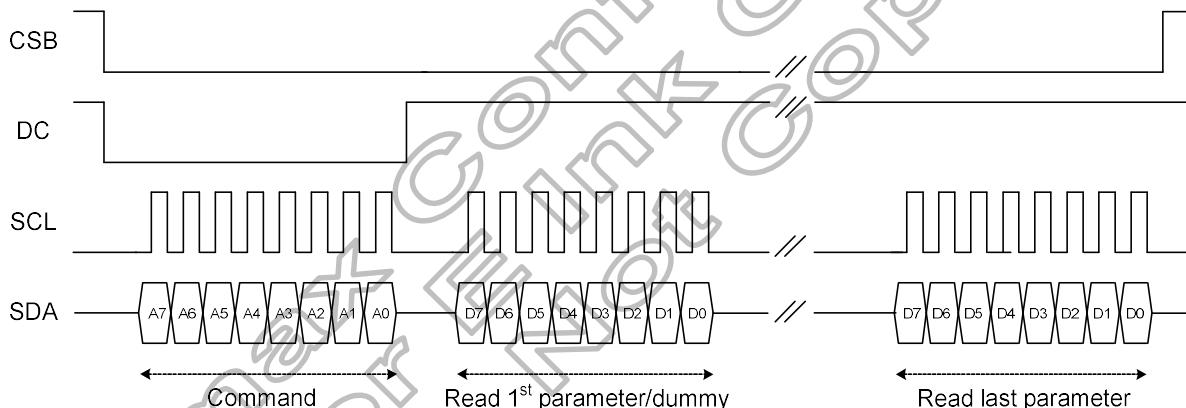


Figure 6.8: 4-wire SPI read parameter (timing type 2)

6.3. Power management

6.3.1. Power on sequence

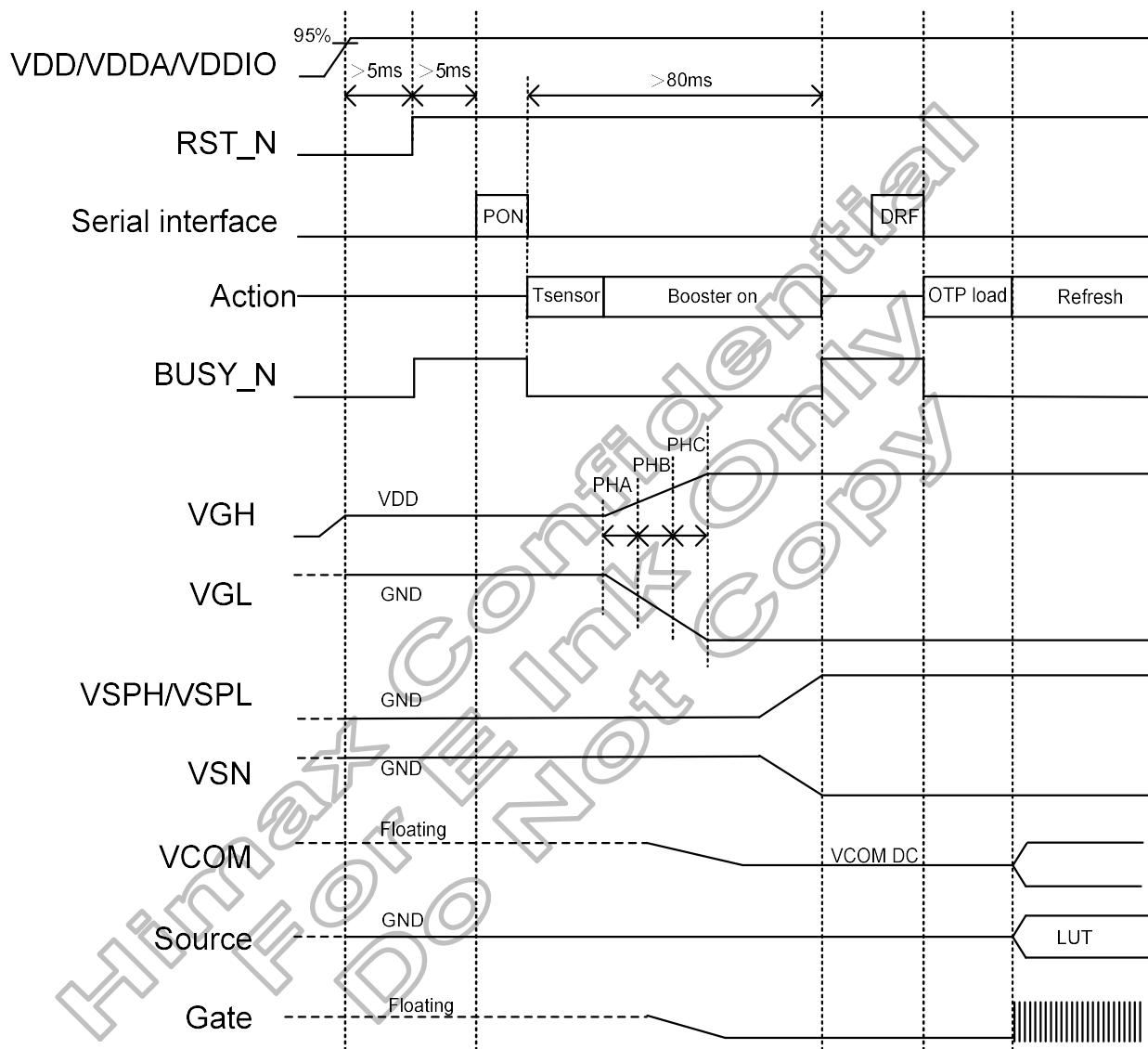


Figure 6.9: Power on sequence

6.3.2. Power off sequence

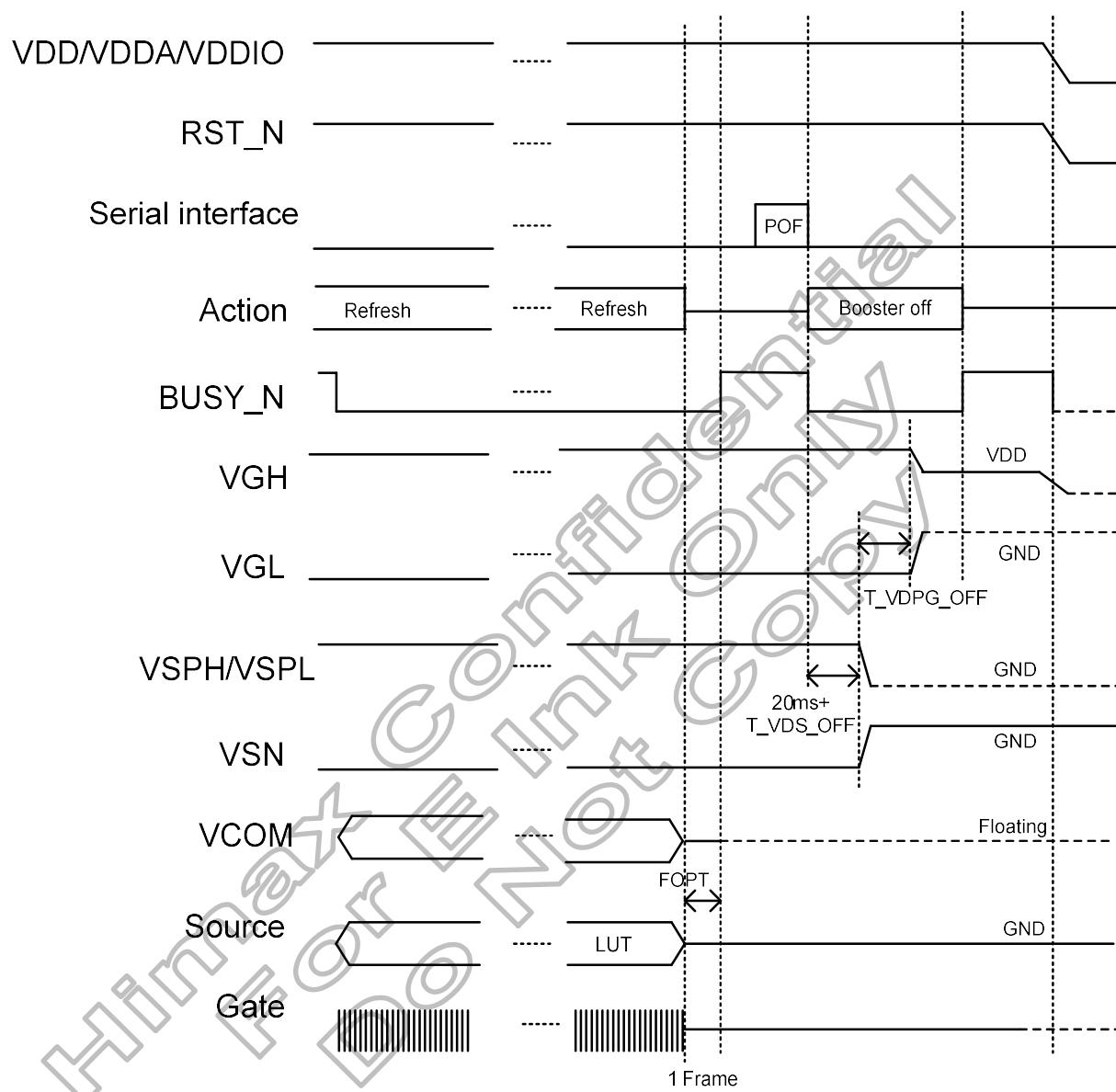


Figure 6.10: Power off sequence (no power off floating or EPD discharge)

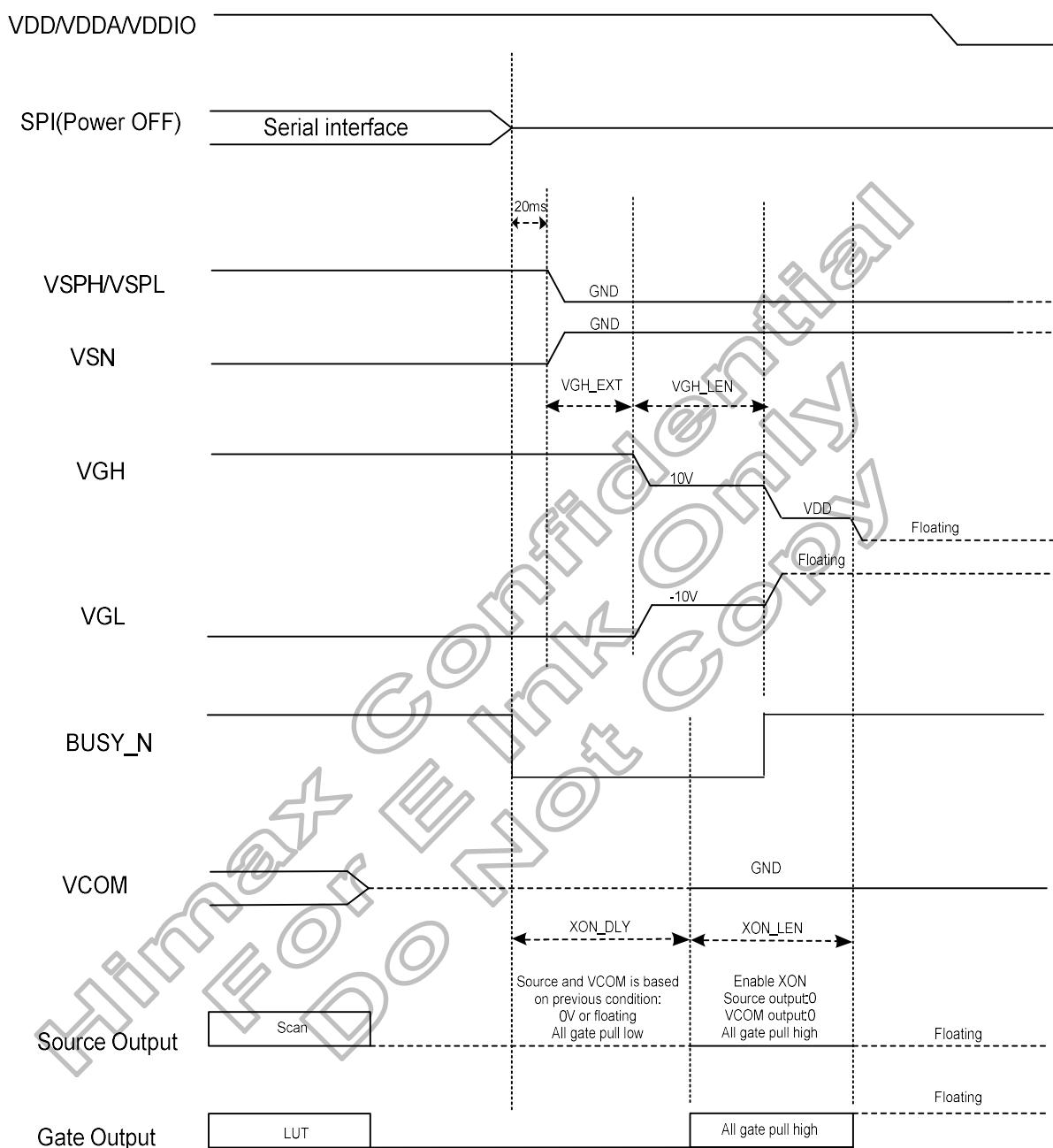


Figure 6.11: Power off sequence with EPD discharge (EDSE=1)

6.4. Power mode switch sequence

6.4.1. PST_MODE=0

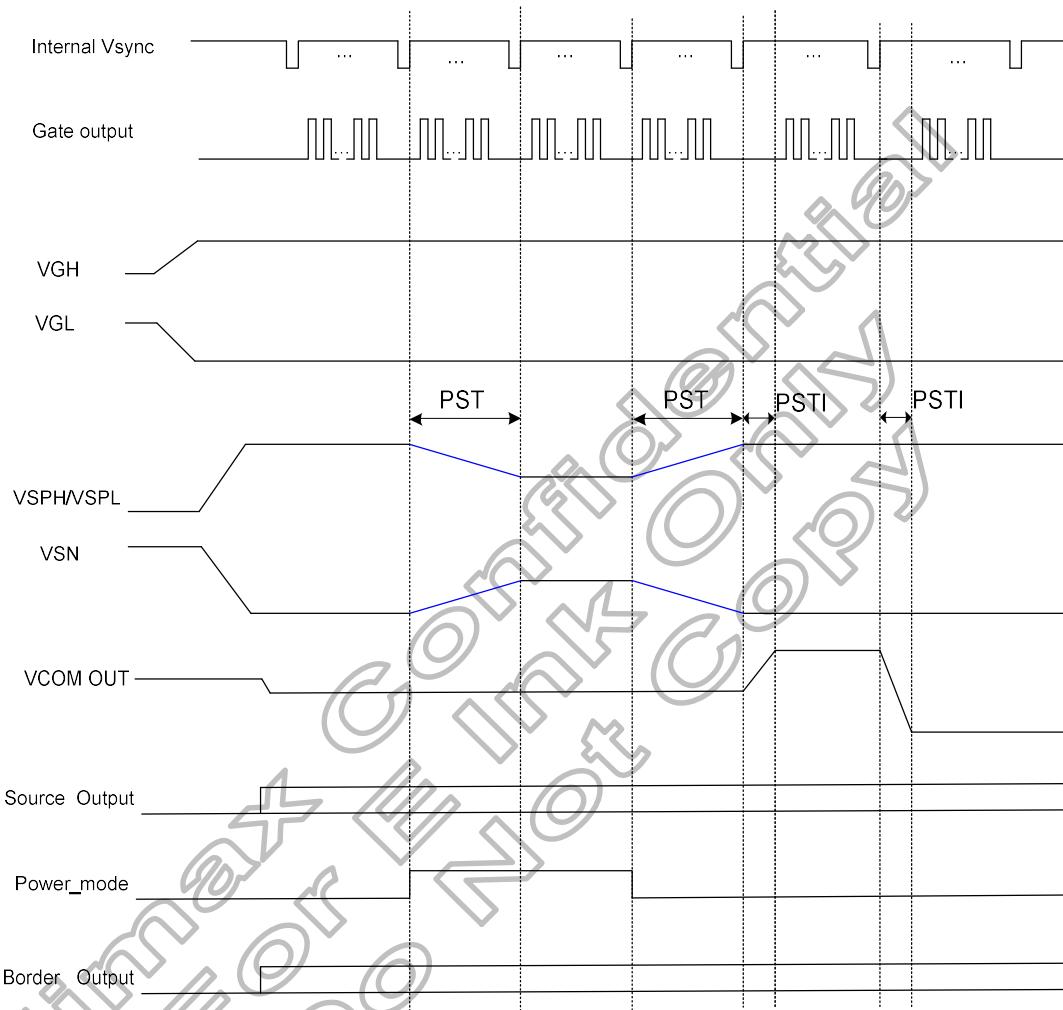


Figure 6.12: Power mode switch sequence (PST_MODE=0)

6.4.2. PST_MODE=1

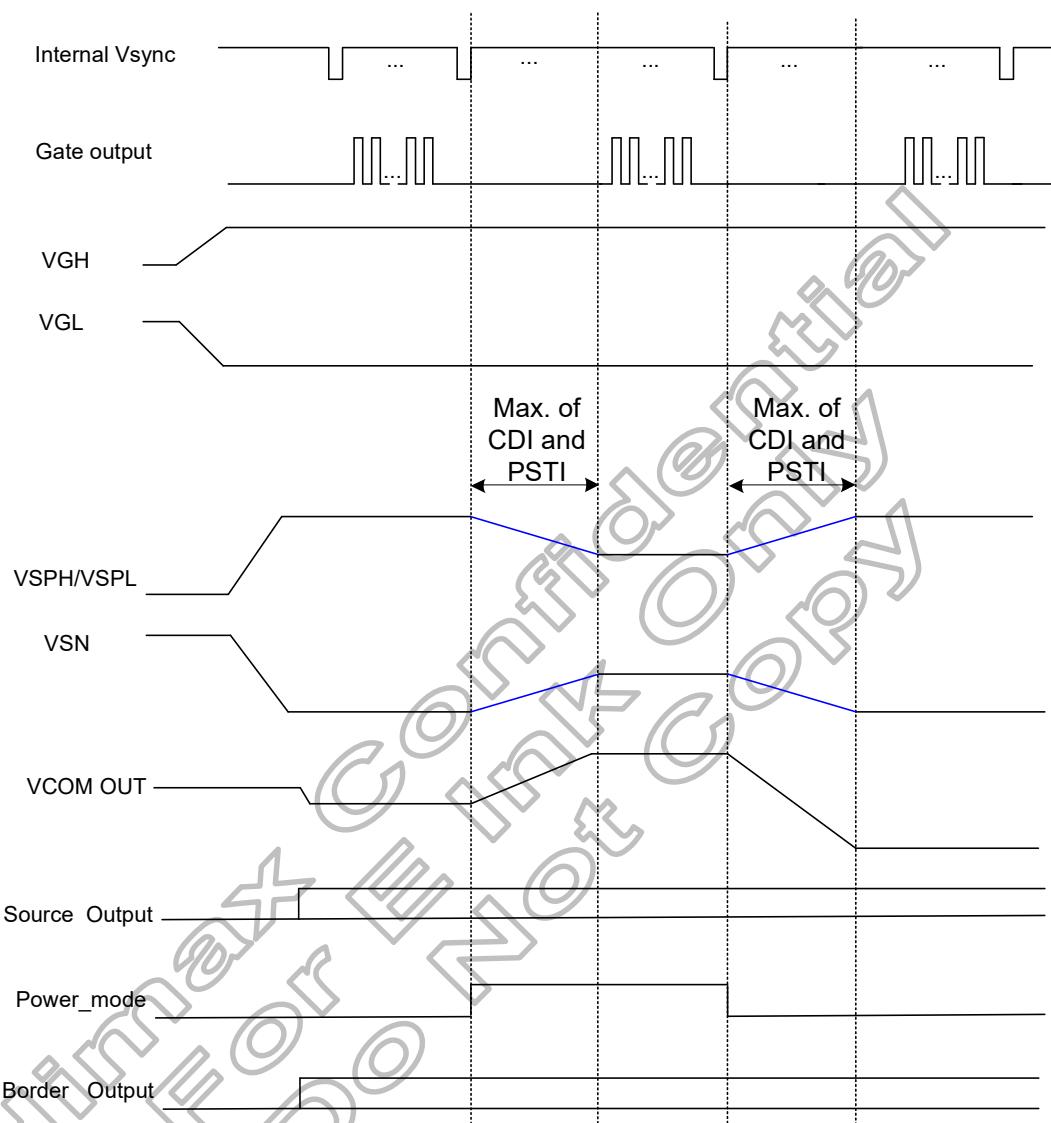


Figure 6.13: Power mode switch sequence (PST_MODE=1)

6.5. VCOM sensing

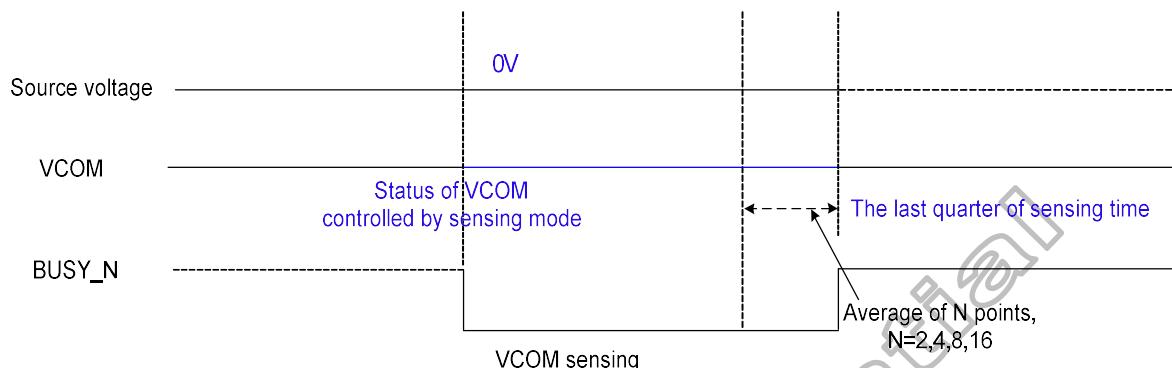


Figure 6.14: VCOM sensing timing

6.6. Boost application circuit

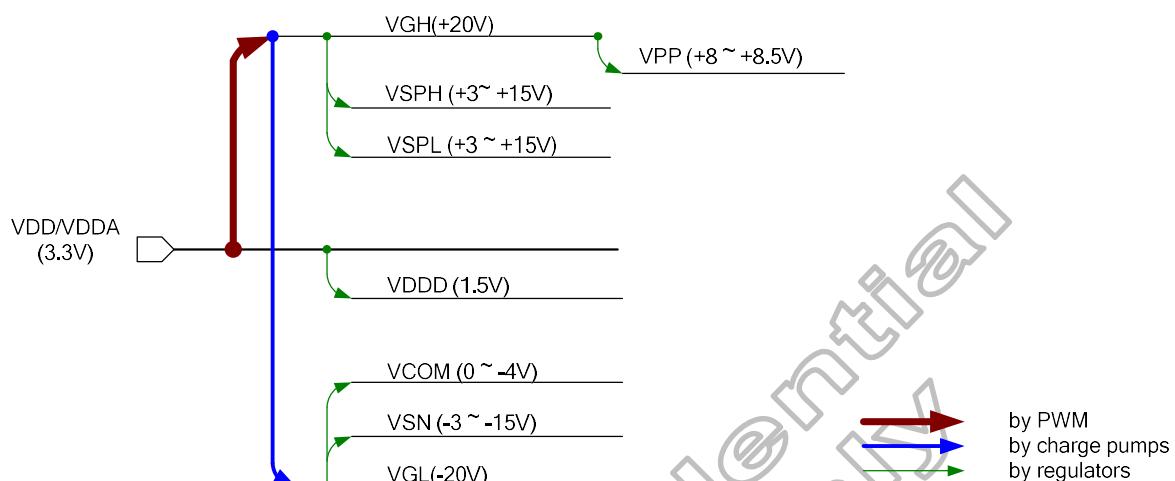


Figure 6.15: The output voltage of boost circuit

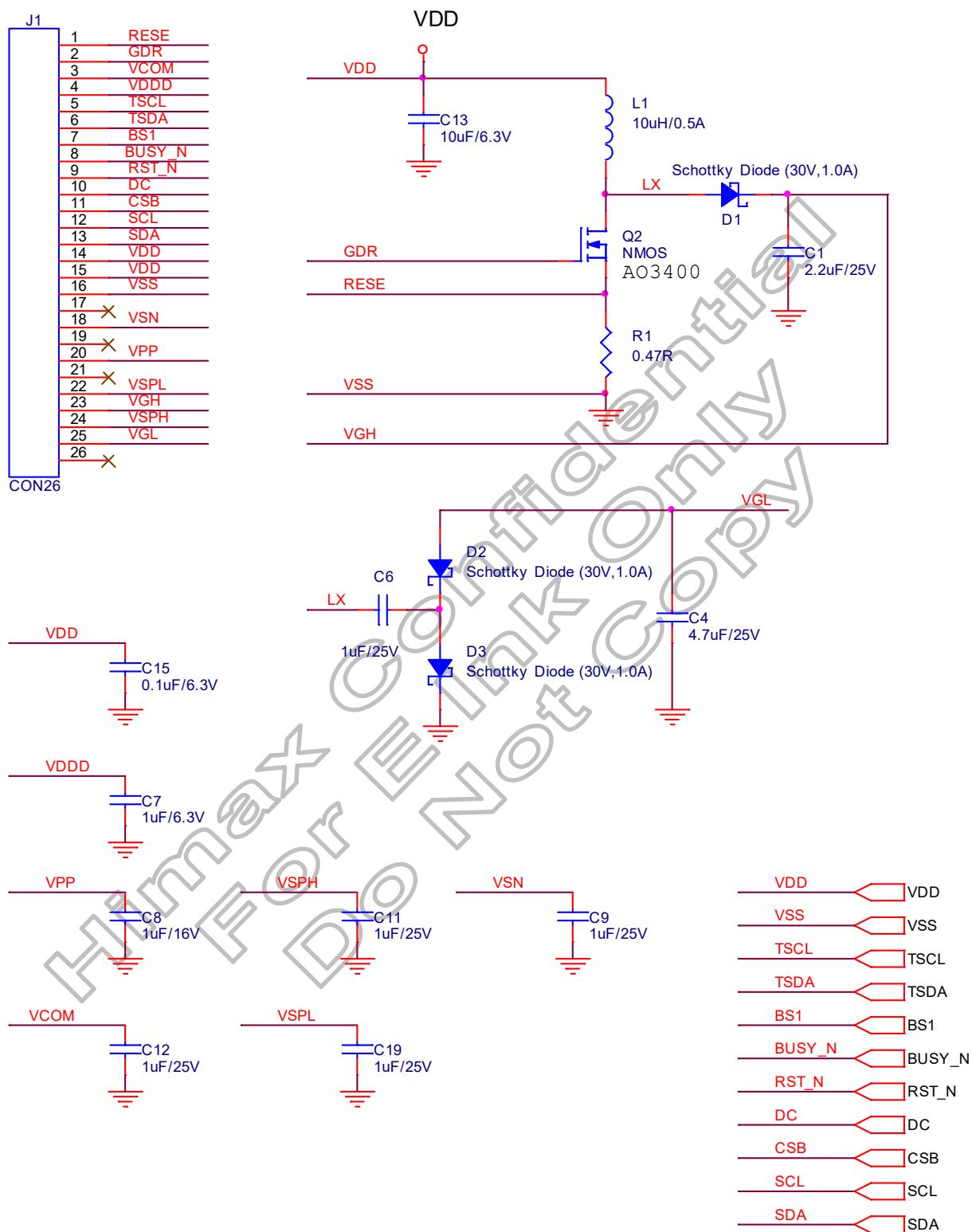


Figure 6.16: Boost application circuit

6.7. Display refresh waveform

Example 1: The driver will scan 1 frame to GND after waveform finished.

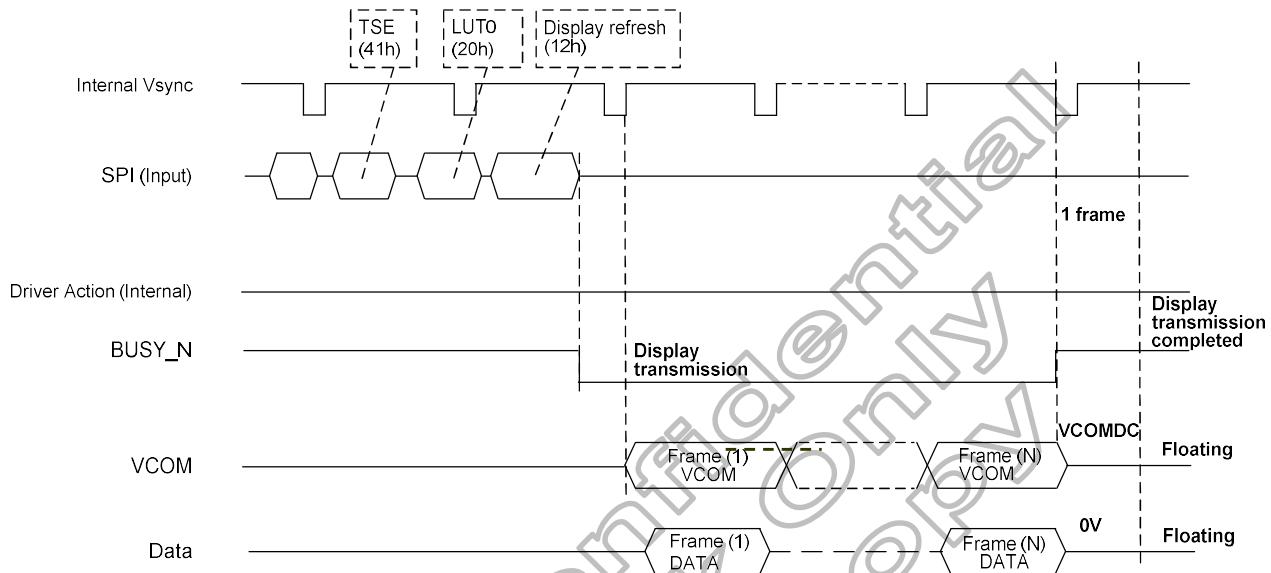


Figure 6.17: Display refresh example 1 waveform

Example 2: The driver will not scan after waveform finished. (Power off floating)

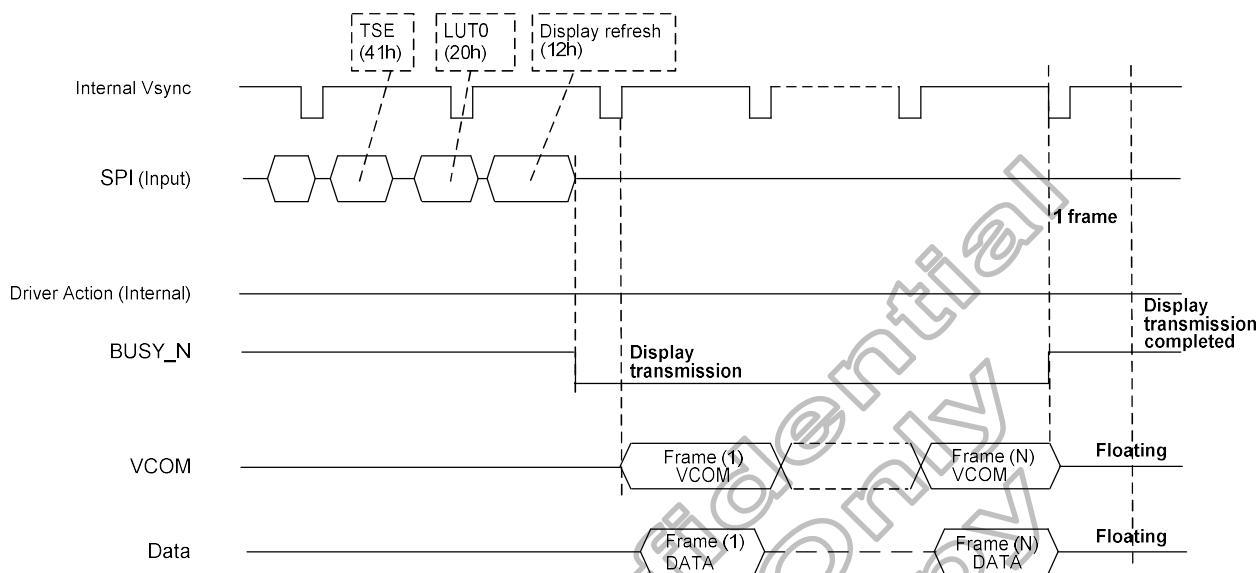


Figure 6.18: Display refresh example 2 waveform

6.8. OTP address mapping

OTP data/mapping address will be controlled by E Ink.

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6.9. Cascade application circuit

All commands sent to Master must be also sent to Slave except for data writing **DTM**. The display data must be separated to two parts, one is for Master and another is for Slave. They are transmitted to Master and Slave individually by using CSB1 and CSB2.

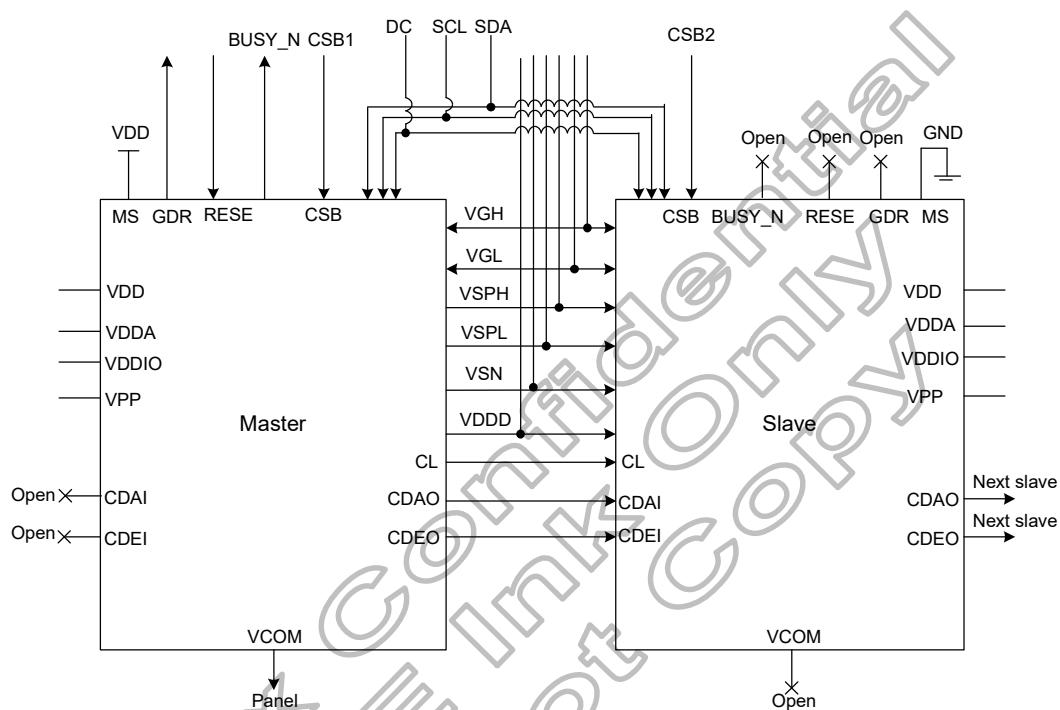


Figure 6.19: Cascade application circuit

7. DC Characteristics

7.1. Absolute maximum rating⁽¹⁾ (VSS=0V)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Logic supply voltage	VDD VDDIO VDDA	-0.3	-	+5.0	V
OTP programming voltage	VPP	-0.3	-	+9.0	V
Digital input range	V _I	-0.3	-	VDDIO+0.3	V
Supply range	VGH-VGL	-0.3	-	+42.0	V
Source					
Analog supply voltage – positive	VSPH	-0.3	-	VGH	V
Analog supply voltage – 1 st color P	VSPL	-0.3	-	VGH	V
Analog supply voltage – negative	VSN	VGL	-	+0.3	V
Gate					
Analog supply voltage – positive	VGH	-0.3	-	+22	V
Analog supply voltage – negative	VGL	-22	-	+0.3	V
Storage temperature range	T _{STG}	-55	-	+125	°C

Note: (1) If ICs are stressed beyond those listed above "absolute maximum ratings", they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

7.2. Recommended operating conditions⁽¹⁾ (VSS=0V)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Logic supply voltage	VDD, VDDIO, VDDA	+2.3	-	+3.6	V
OTP programming voltage	VPP	+8	-	+8.5	V
Digital input range	V _I	0	-	VDDIO	V
Supply range	VGH-VGL	0	-	+40.0	V
Source					
Analog supply voltage – positive	VSPH	0	-	+15	V
Analog supply voltage – 1 st color P	VSPL	0	-	+15	V
Analog supply voltage – negative	VSN	-15	-	0	V
Gate					
Analog supply voltage – positive	VGH	0	-	+20	V
Analog supply voltage – negative	VGL	-20	-	0	V
Operation temperature	T _A	-30	-	+85	°C

7.3. DC electrical characteristics

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
IO supply voltage	VDDIO	-	2.3	3.3	3.6	V
Supply voltage	VDD	-	2.3	3.3	3.6	V
DCDC driver supply voltage	VDDA	-	2.3	3.3	3.6	V
OTP program voltage	V _{pp}	-	8.0	8.25	8.5	V
High level input voltage	V _{IH}	Digital input pins	0.8xVDDIO	-	VDDIO	V
Low level input voltage	V _{IL}	Digital input pins	0	-	0.2xVDDIO	V
High level output voltage	V _{OH}	Digital input pins, I _{OH} =400μA	0.8xVDDIO	-	VDDIO	V
Low level output voltage	V _{OL}	Digital input pins, I _{OL} =-400μA	0	-	0.2xVDDIO	V
Input leakage current	I _{IN}	Digital input pins except pull-up, pull-down pin	-1	-	1	μA
Pull-up/down impedance	R _{IN}	-	-	200	-	KΩ
Voltage range of VGH - VGL	VGH-VGL	-	0	-	40	V
VGH supply voltage dev	dVGH	-	-200	0	+200	mV
VGL supply voltage dev	dVGL	-	-200	0	+200	mV
Supply voltage dev	dVS _{PH}	-	-200	0	+200	mV
Supply voltage dev	dVS _{PL}	-	-200	0	+200	mV
Supply voltage dev	dVS _N	-	-200	0	+200	mV
Supply voltage dev	dV _{COM}	-	-200	0	+200	mV
Driver output resistance	R _{ON}	For source driver, T _A =25°C, V _{OUT} =±15V	-	10	-	KΩ
		For gate driver, T _A =25°C, V _{OUT} =±20V	-	10	-	

(VDD=VDDA=VDDIO=3.0V, T_A=25°C)

Parameter	Symbol	Condition	Spec.			Unit	
			Min.	Typ.	Max.		
Digital deep sleep current	I _{VDD}	VDDD OFF	-	0.3	0.5	μA	
Digital stand-by current		All stopped	-	8.2	10.0	μA	
Digital operating current		-	-	-	0.1	mA	
IO deep sleep current	I _{VDDIO}	VDDD OFF	-	0.1	0.3	μA	
IO stand-by current		Booster OFF	-	2.5	4.0	μA	
IO operating current		No load	-	-	0.1	mA	
DCDC deep sleep current	I _{VDDA}	VDDD OFF	-	0.1	0.3	μA	
DCDC stand-by current		Booster OFF	-	15.5	20.0	μA	
DCDC operating current		Source output VS _{PH} /VS _N , Period =126μs V _{COM} No load	-	-	5.0	mA	
		Source output VS _{PH} /VS _N , Duty=0.5, Period =126μs, V _{COM} =415pF, Boost MOS=340pF	-	-	25.0	mA	

8. AC Characteristics

8.1. Display AC characteristics

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
OSC	F_{osc}	IC Internal OSC	1.98	2	2.02	MHz
Frame Rate	F_{VSYNC}	Default frame rate (400*300)	49.5	50	50.5	Hz

8.2. 3-wire AC characteristics

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
CSB	T_{CSS}	Chip select setup time	60	-	-	ns
	T_{CSH}	Chip select hold time	65	-	-	ns
	T_{SCC}	Chip select setup time	60	-	-	ns
	T_{CHW}	Chip select setup time	40	-	-	ns
SCL	T_{SCYCW}	Serial clock cycle (Write)	100	-	-	ns
	T_{SHW}	SCL "H" pulse width (Write)	35	-	-	ns
	T_{SLW}	SCL "L" pulse width (Write)	35	-	-	ns
	T_{SCYCR}	Serial clock cycle (Read)	150	-	-	ns
	T_{SHR}	SCL "H" pulse width (Read)	60	-	-	ns
	T_{SLR}	SCL "L" pulse width (Read)	60	-	-	ns
SDA (D_{IN})	T_{SDS}	Data setup time	30	-	-	ns
	T_{SDH}	Data hold time	30	-	-	ns
SDA (D_{OUT})	T_{ACC}	Access time	-	-	10	ns
	T_{TOH}	Output disable time	15	-	-	ns

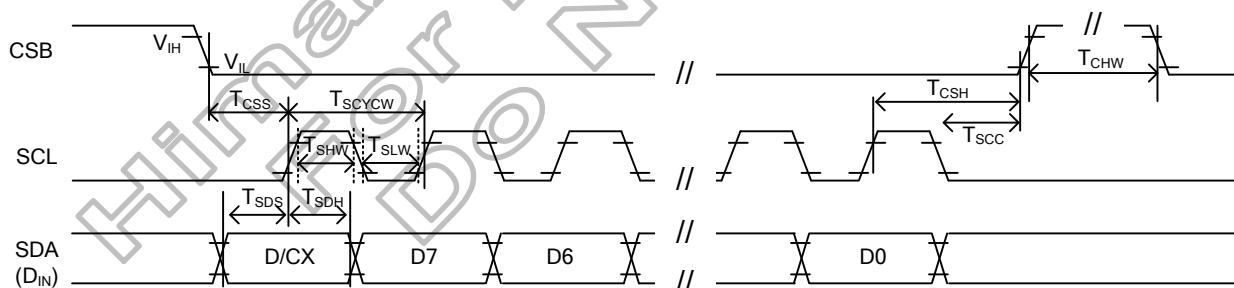


Figure 8.1: 3-wire serial internal characteristics (write mode)

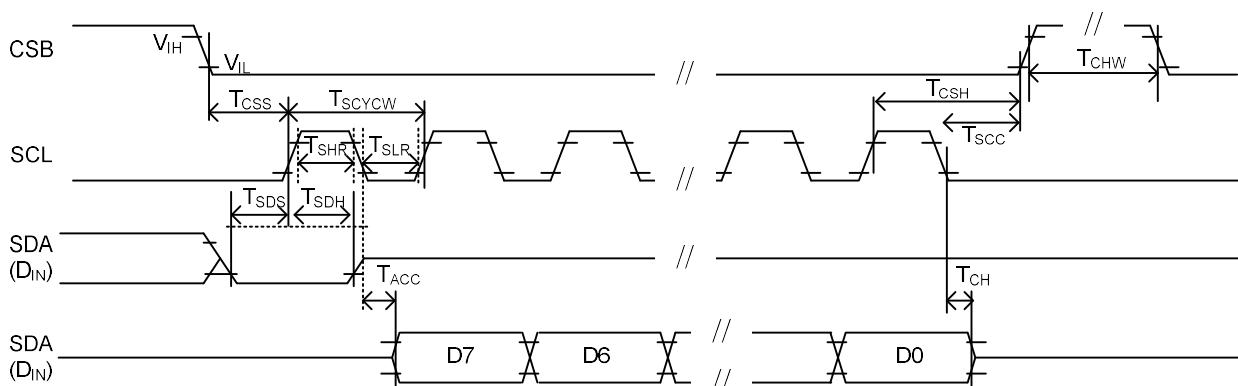


Figure 8.2: 3-wire serial internal characteristics (read mode)

8.3. 4-wire AC characteristics

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
CSB	T _{CS} S	Chip select setup time	60	-	-	ns
	T _{CS} H	Chip select hold time	65	-	-	ns
	T _{SC} C	Chip select setup time	60	-	-	ns
	T _{CH} W	Chip select setup time	40	-	-	ns
SCL	T _{SCYCW}	Serial clock cycle (Write)	100	-	-	ns
	T _{SHW}	SCL "H" pulse width (Write)	35	-	-	ns
	T _{SLW}	SCL "L" pulse width (Write)	35	-	-	ns
	T _{SCYCR}	Serial clock cycle (Read)	150	-	-	ns
	T _{SHR}	SCL "H" pulse width (Read)	60	-	-	ns
	T _{SLR}	SCL "L" pulse width (Read)	60	-	-	ns
DC	T _{DCS}	DC setup time	30	-	-	ns
	T _{DCH}	DC hold time	30	-	-	ns
SDA (D _{IN})	T _{SDS}	Data setup time	30	-	-	ns
	T _{SDH}	Data hold time	30	-	-	ns
SDA (D _{OUT})	T _{ACC}	Access time	-	-	50	ns
	T _{OH}	Output disable time	15	-	-	ns

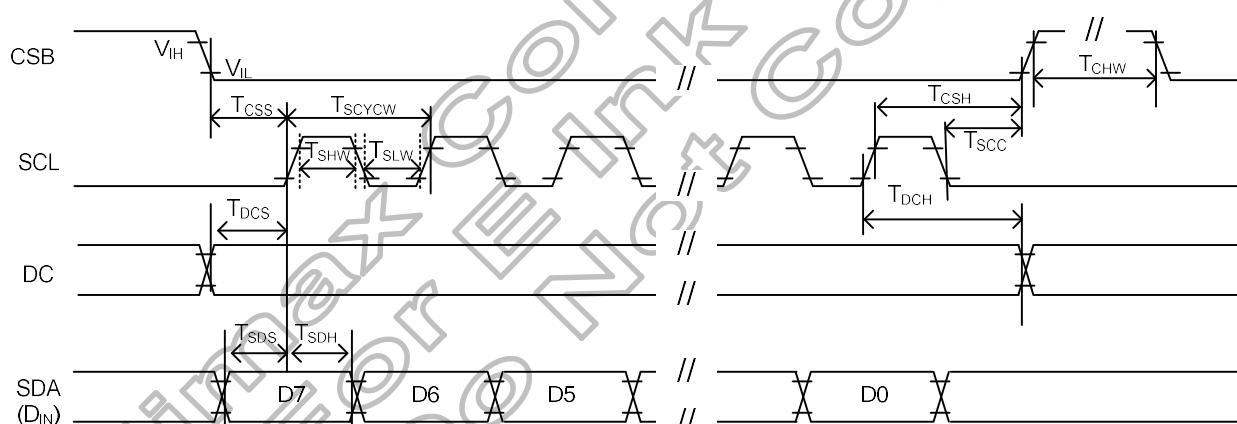


Figure 8.3: 4-wire serial internal characteristics (Write mode)

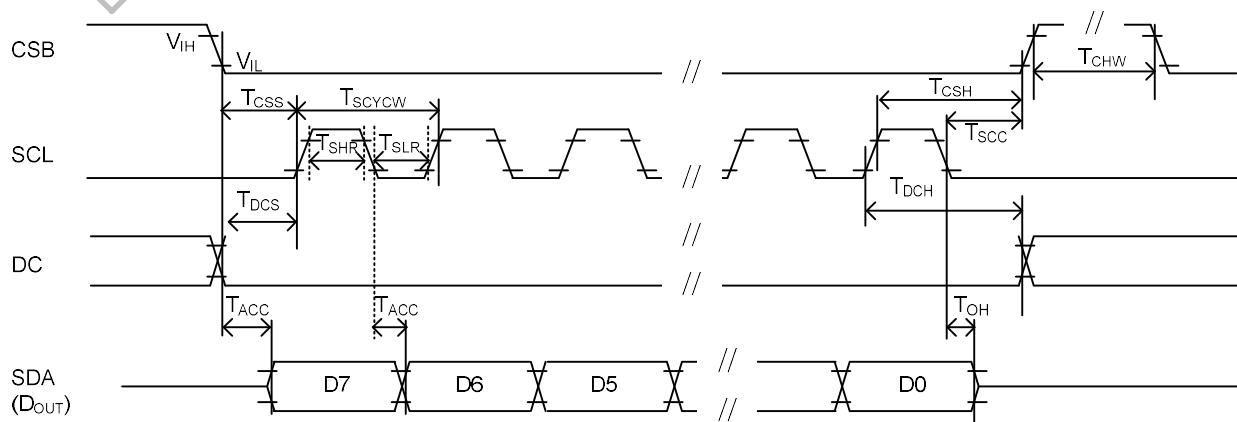
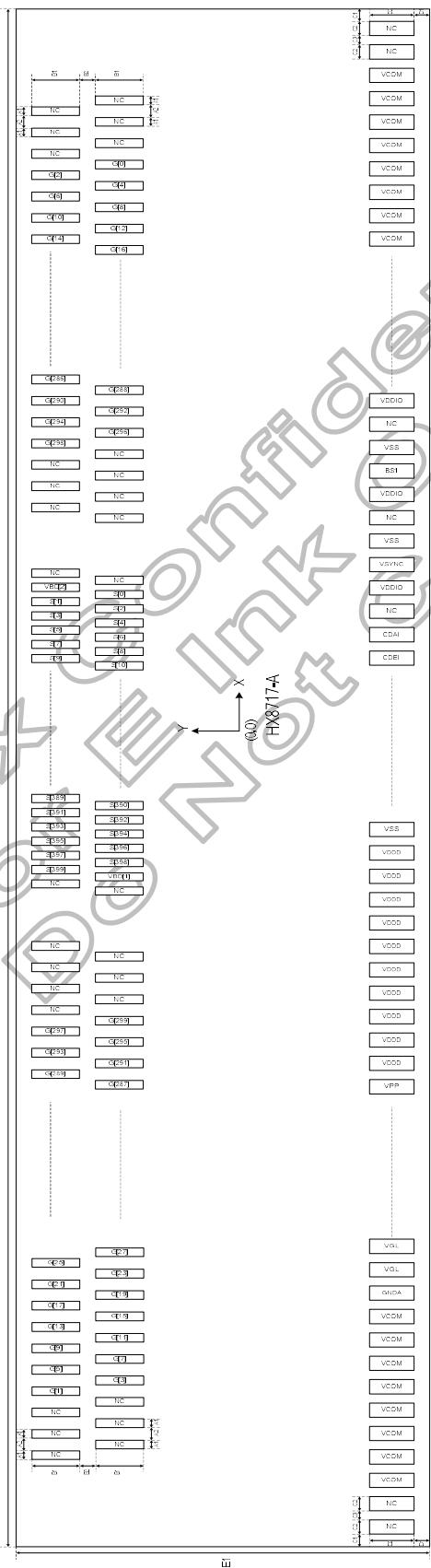


Figure 8.4: 4-wire serial internal characteristics (Read mode)

9. Pad Coordinates

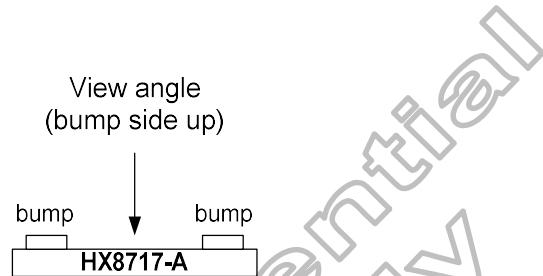
9.1. HX8717-A bump location and outline dimensions



NC (2)	NC (1)	NC (1)
VCOM (8)	G[3] (1)	G[1] (1)
GNDA (1)	G[7] (1)	G[5] (1)
VGL (16)	G[11] (1)	G[9] (1)
GNDA (1)	G[15] (1)	G[13] (1)
VSN (10)	G[19] (1)	G[17] (1)
GNDA (1)	G[23] (1)	G[21] (1)
VGH (14)	G[27] (1)	G[25] (1)
GNDA (1)	G[31] (1)	G[29] (1)
VSPH (10)	G[35] (1)	G[33] (1)
GNDA (1)	G[39] (1)	G[37] (1)
VPP (7)	G[43] (1)	G[41] (1)
VDDD (10)	G[47] (1)	G[45] (1)
VSS (2)	G[51] (1)	G[49] (1)
GNDA (10)	G[55] (1)	G[53] (1)
VDM (6)	G[59] (1)	G[57] (1)
GNDA (1)	G[63] (1)	G[61] (1)
VSS (5)		G[65] (1)
VDD (10)		
VDDA (7)		
NC (36)		
TEST[1] (1)		
TEST[2] (1)		
VSS (1)		
NC (3)		
VDDIO (4)		
TEST[3] (1)		
NC (6)		
SDA (1)		
SCL (1)		
VSS (1)		
CSB (1)		
VDDIO (1)		
NC (2)		
VSS (1)		
DC (1)		
VDDIO (1)		
NC (4)		
RST_N (1)		
BUSY_N (1)		
VSS (1)		
NC (3)		
CDAO (1)		
CDEO (1)		
CL (1)		
CDEI (1)		
CDAI (1)		
NC (1)		
VDDIO (1)		
BS1 (1)		
VSS (1)		
NC (1)		
VDDIO (1)		
CHKGI (1)		
VSS (1)		
MS (1)		
VDDIO (1)		
VSS (1)		
TSDA (2)		
TSCL (2)		
VSS (1)		
CHKGO (1)		
NC (1)		
VSS (1)		
TEST[6] (1)		
NC (1)		
VSS (1)		
NC (2)		
VSS (1)		
NC (2)		
VSS (1)		
NC (10)		
VSPL (8)		
NC (1)		
TEST[7] (1)		
NC (4)		
VSS (1)	G[44] (1)	G[46] (1)
FB (2)	G[40] (1)	G[42] (1)
VSS (1)	G[36] (1)	G[38] (1)
RESE (2)	G[32] (1)	G[34] (1)
VSS (1)	G[28] (1)	G[30] (1)
GDR (8)	G[24] (1)	G[26] (1)
VSS (1)	G[20] (1)	G[22] (1)
VCOM (8)	G[16] (1)	G[18] (1)
NC (2)	G[12] (1)	G[14] (1)
	G[8] (1)	G[10] (1)
	G[4] (1)	G[6] (1)
	G[0] (1)	G[2] (1)
	NC (1)	NC (1)
	NC (1)	NC (1)
	NC (1)	NC (1)

Symbol	Dimension (μm)
A1	17
A2	25
B1	75
B2	25
E1	925

Symbol	Dimension (μm)
C2	28
C3	18
D1	37.5
D2	70
E2	13100

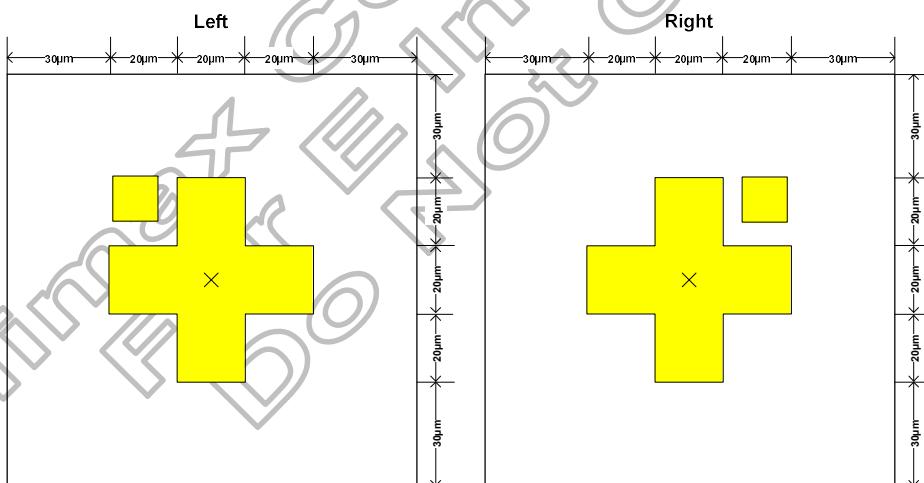


Chip size: 13100 x 925 (without scribe line)

Scribe line: 70x70 μm

Total area of IC bump: 1457530 μm^2

9.2. Alignment mark



9.3. Bump center coordinates

No.	Name	X	Y	Bump size (μm)
1	NC	-6486	-390	28 x 70
2	NC	-6440	-390	28 x 70
3	VCOM	-6394	-390	28 x 70
4	VCOM	-6348	-390	28 x 70
5	VCOM	-6302	-390	28 x 70
6	VCOM	-6256	-390	28 x 70
7	VCOM	-6210	-390	28 x 70
8	VCOM	-6164	-390	28 x 70
9	VCOM	-6118	-390	28 x 70
10	VCOM	-6072	-390	28 x 70
11	GNDA	-6026	-390	28 x 70
12	VGL	-5980	-390	28 x 70
13	VGL	-5934	-390	28 x 70
14	VGL	-5888	-390	28 x 70
15	VGL	-5842	-390	28 x 70
16	VGL	-5796	-390	28 x 70
17	VGL	-5750	-390	28 x 70
18	VGL	-5704	-390	28 x 70
19	VGL	-5658	-390	28 x 70
20	VGL	-5612	-390	28 x 70
21	VGL	-5566	-390	28 x 70
22	VGL	-5520	-390	28 x 70
23	VGL	-5474	-390	28 x 70
24	VGL	-5428	-390	28 x 70
25	VGL	-5382	-390	28 x 70
26	VGL	-5336	-390	28 x 70
27	VGL	-5290	-390	28 x 70
28	GNDA	-5244	-390	28 x 70
29	VSN	-5198	-390	28 x 70
30	VSN	-5152	-390	28 x 70
31	VSN	-5106	-390	28 x 70
32	VSN	-5060	-390	28 x 70
33	VSN	-5014	-390	28 x 70
34	VSN	-4968	-390	28 x 70
35	VSN	-4922	-390	28 x 70
36	VSN	-4876	-390	28 x 70
37	VSN	-4830	-390	28 x 70
38	VSN	-4784	-390	28 x 70
39	GNDA	-4738	-390	28 x 70
40	VGH	-4692	-390	28 x 70
41	VGH	-4646	-390	28 x 70
42	VGH	-4600	-390	28 x 70
43	VGH	-4554	-390	28 x 70
44	VGH	-4508	-390	28 x 70
45	VGH	-4462	-390	28 x 70
46	VGH	-4416	-390	28 x 70
47	VGH	-4370	-390	28 x 70
48	VGH	-4324	-390	28 x 70
49	VGH	-4278	-390	28 x 70
50	VGH	-4232	-390	28 x 70

No.	Name	X	Y	Bump size (μm)
51	VGH	-4186	-390	28 x 70
52	VGH	-4140	-390	28 x 70
53	VGH	-4094	-390	28 x 70
54	GNDA	-4048	-390	28 x 70
55	VSPH	-4002	-390	28 x 70
56	VSPH	-3956	-390	28 x 70
57	VSPH	-3910	-390	28 x 70
58	VSPH	-3864	-390	28 x 70
59	VSPH	-3818	-390	28 x 70
60	VSPH	-3772	-390	28 x 70
61	VSPH	-3726	-390	28 x 70
62	VSPH	-3680	-390	28 x 70
63	VSPH	-3634	-390	28 x 70
64	VSPH	-3588	-390	28 x 70
65	GNDA	-3542	-390	28 x 70
66	VPP	-3496	-390	28 x 70
67	VPP	-3450	-390	28 x 70
68	VPP	-3404	-390	28 x 70
69	VPP	-3358	-390	28 x 70
70	VPP	-3312	-390	28 x 70
71	VPP	-3266	-390	28 x 70
72	VPP	-3220	-390	28 x 70
73	VDDD	-3174	-390	28 x 70
74	VDDD	-3128	-390	28 x 70
75	VDDD	-3082	-390	28 x 70
76	VDDD	-3036	-390	28 x 70
77	VDDD	-2990	-390	28 x 70
78	VDDD	-2944	-390	28 x 70
79	VDDD	-2898	-390	28 x 70
80	VDDD	-2852	-390	28 x 70
81	VDDD	-2806	-390	28 x 70
82	VDDD	-2760	-390	28 x 70
83	VSS	-2714	-390	28 x 70
84	VSS	-2668	-390	28 x 70
85	GNDA	-2622	-390	28 x 70
86	GNDA	-2576	-390	28 x 70
87	GNDA	-2530	-390	28 x 70
88	GNDA	-2484	-390	28 x 70
89	GNDA	-2438	-390	28 x 70
90	GNDA	-2392	-390	28 x 70
91	GNDA	-2346	-390	28 x 70
92	GNDA	-2300	-390	28 x 70
93	GNDA	-2254	-390	28 x 70
94	GNDA	-2208	-390	28 x 70
95	VDM	-2162	-390	28 x 70
96	VDM	-2116	-390	28 x 70
97	VDM	-2070	-390	28 x 70
98	VDM	-2024	-390	28 x 70
99	VDM	-1978	-390	28 x 70
100	VDM	-1932	-390	28 x 70

No.	Name	X	Y	Bump size (μm)	No.	Name	X	Y	Bump size (μm)
101	GNDA	-1886	-390	28 x 70	151	NC	414	-390	28 x 70
102	VSS	-1840	-390	28 x 70	152	NC	460	-390	28 x 70
103	VSS	-1794	-390	28 x 70	153	NC	506	-390	28 x 70
104	VSS	-1748	-390	28 x 70	154	NC	552	-390	28 x 70
105	VSS	-1702	-390	28 x 70	155	NC	598	-390	28 x 70
106	VSS	-1656	-390	28 x 70	156	NC	644	-390	28 x 70
107	VDD	-1610	-390	28 x 70	157	NC	690	-390	28 x 70
108	VDD	-1564	-390	28 x 70	158	NC	736	-390	28 x 70
109	VDD	-1518	-390	28 x 70	159	NC	782	-390	28 x 70
110	VDD	-1472	-390	28 x 70	160	TEST[1]	828	-390	28 x 70
111	VDD	-1426	-390	28 x 70	161	TEST[2]	874	-390	28 x 70
112	VDD	-1380	-390	28 x 70	162	VSS	920	-390	28 x 70
113	VDD	-1334	-390	28 x 70	163	NC	966	-390	28 x 70
114	VDD	-1288	-390	28 x 70	164	NC	1012	-390	28 x 70
115	VDD	-1242	-390	28 x 70	165	NC	1058	-390	28 x 70
116	VDD	-1196	-390	28 x 70	166	VDDIO	1104	-390	28 x 70
117	VDDA	-1150	-390	28 x 70	167	VDDIO	1150	-390	28 x 70
118	VDDA	-1104	-390	28 x 70	168	VDDIO	1196	-390	28 x 70
119	VDDA	-1058	-390	28 x 70	169	VDDIO	1242	-390	28 x 70
120	VDDA	-1012	-390	28 x 70	170	TEST[3]	1288	-390	28 x 70
121	VDDA	-966	-390	28 x 70	171	NC	1334	-390	28 x 70
122	VDDA	-920	-390	28 x 70	172	NC	1380	-390	28 x 70
123	VDDA	-874	-390	28 x 70	173	NC	1426	-390	28 x 70
124	NC	-828	-390	28 x 70	174	NC	1472	-390	28 x 70
125	NC	-782	-390	28 x 70	175	NC	1518	-390	28 x 70
126	NC	-736	-390	28 x 70	176	NC	1564	-390	28 x 70
127	NC	-690	-390	28 x 70	177	SDA	1610	-390	28 x 70
128	NC	-644	-390	28 x 70	178	SCL	1656	-390	28 x 70
129	NC	-598	-390	28 x 70	179	VSS	1702	-390	28 x 70
130	NC	-552	-390	28 x 70	180	CSB	1748	-390	28 x 70
131	NC	-506	-390	28 x 70	181	VDDIO	1794	-390	28 x 70
132	NC	-460	-390	28 x 70	182	NC	1840	-390	28 x 70
133	NC	-414	-390	28 x 70	183	NC	1886	-390	28 x 70
134	NC	-368	-390	28 x 70	184	VSS	1932	-390	28 x 70
135	NC	-322	-390	28 x 70	185	DC	1978	-390	28 x 70
136	NC	-276	-390	28 x 70	186	VDDIO	2024	-390	28 x 70
137	NC	-230	-390	28 x 70	187	NC	2070	-390	28 x 70
138	NC	-184	-390	28 x 70	188	NC	2116	-390	28 x 70
139	NC	-138	-390	28 x 70	189	NC	2162	-390	28 x 70
140	NC	-92	-390	28 x 70	190	NC	2208	-390	28 x 70
141	NC	-46	-390	28 x 70	191	RST_N	2254	-390	28 x 70
142	NC	0	-390	28 x 70	192	BUSY_N	2300	-390	28 x 70
143	NC	46	-390	28 x 70	193	VSS	2346	-390	28 x 70
144	NC	92	-390	28 x 70	194	NC	2392	-390	28 x 70
145	NC	138	-390	28 x 70	195	NC	2438	-390	28 x 70
146	NC	184	-390	28 x 70	196	NC	2484	-390	28 x 70
147	NC	230	-390	28 x 70	197	CDAO	2530	-390	28 x 70
148	NC	276	-390	28 x 70	198	CDEO	2576	-390	28 x 70
149	NC	322	-390	28 x 70	199	CL	2622	-390	28 x 70
150	NC	368	-390	28 x 70	200	CDEI	2668	-390	28 x 70

No.	Name	X	Y	Bump size (μm)
201	CDAI	2714	-390	28 x 70
202	NC	2760	-390	28 x 70
203	VDDIO	2806	-390	28 x 70
204	VSYNC	2852	-390	28 x 70
205	VSS	2898	-390	28 x 70
206	NC	2944	-390	28 x 70
207	VDDIO	2990	-390	28 x 70
208	BS1	3036	-390	28 x 70
209	VSS	3082	-390	28 x 70
210	NC	3128	-390	28 x 70
211	VDDIO	3174	-390	28 x 70
212	CHKGI	3220	-390	28 x 70
213	VSS	3266	-390	28 x 70
214	MS	3312	-390	28 x 70
215	VDDIO	3358	-390	28 x 70
216	VSS	3404	-390	28 x 70
217	TSDA	3450	-390	28 x 70
218	TSDA	3496	-390	28 x 70
219	TSCL	3542	-390	28 x 70
220	TSCL	3588	-390	28 x 70
221	VSS	3634	-390	28 x 70
222	CHKGO	3680	-390	28 x 70
223	NC	3726	-390	28 x 70
224	VSS	3772	-390	28 x 70
225	TEST[6]	3818	-390	28 x 70
226	NC	3864	-390	28 x 70
227	VSS	3910	-390	28 x 70
228	NC	3956	-390	28 x 70
229	NC	4002	-390	28 x 70
230	VSS	4048	-390	28 x 70
231	NC	4094	-390	28 x 70
232	NC	4140	-390	28 x 70
233	VSS	4186	-390	28 x 70
234	NC	4232	-390	28 x 70
235	NC	4278	-390	28 x 70
236	NC	4324	-390	28 x 70
237	NC	4370	-390	28 x 70
238	NC	4416	-390	28 x 70
239	NC	4462	-390	28 x 70
240	NC	4508	-390	28 x 70
241	NC	4554	-390	28 x 70
242	NC	4600	-390	28 x 70
243	NC	4646	-390	28 x 70
244	VSPL	4692	-390	28 x 70
245	VSPL	4738	-390	28 x 70
246	VSPL	4784	-390	28 x 70
247	VSPL	4830	-390	28 x 70
248	VSPL	4876	-390	28 x 70
249	VSPL	4922	-390	28 x 70
250	VSPL	4968	-390	28 x 70

No.	Name	X	Y	Bump size (μm)
251	VSPL	5014	-390	28 x 70
252	NC	5060	-390	28 x 70
253	TEST[7]	5106	-390	28 x 70
254	NC	5152	-390	28 x 70
255	NC	5198	-390	28 x 70
256	NC	5244	-390	28 x 70
257	NC	5290	-390	28 x 70
258	VSS	5336	-390	28 x 70
259	FB	5382	-390	28 x 70
260	FB	5428	-390	28 x 70
261	VSS	5474	-390	28 x 70
262	RESE	5520	-390	28 x 70
263	RESE	5566	-390	28 x 70
264	VSS	5612	-390	28 x 70
265	GDR	5658	-390	28 x 70
266	GDR	5704	-390	28 x 70
267	GDR	5750	-390	28 x 70
268	GDR	5796	-390	28 x 70
269	GDR	5842	-390	28 x 70
270	GDR	5888	-390	28 x 70
271	GDR	5934	-390	28 x 70
272	GDR	5980	-390	28 x 70
273	VSS	6026	-390	28 x 70
274	VCOM	6072	-390	28 x 70
275	VCOM	6118	-390	28 x 70
276	VCOM	6164	-390	28 x 70
277	VCOM	6210	-390	28 x 70
278	VCOM	6256	-390	28 x 70
279	VCOM	6302	-390	28 x 70
280	VCOM	6348	-390	28 x 70
281	VCOM	6394	-390	28 x 70
282	NC	6440	-390	28 x 70
283	NC	6486	-390	28 x 70
284	NC	6345	294.5	17 x 75
285	NC	6324	394.5	17 x 75
286	NC	6303	294.5	17 x 75
287	NC	6282	394.5	17 x 75
288	NC	6261	294.5	17 x 75
289	NC	6240	394.5	17 x 75
290	G[0]	6219	294.5	17 x 75
291	G[2]	6198	394.5	17 x 75
292	G[4]	6177	294.5	17 x 75
293	G[6]	6156	394.5	17 x 75
294	G[8]	6135	294.5	17 x 75
295	G[10]	6114	394.5	17 x 75
296	G[12]	6093	294.5	17 x 75
297	G[14]	6072	394.5	17 x 75
298	G[16]	6051	294.5	17 x 75
299	G[18]	6030	394.5	17 x 75
300	G[20]	6009	294.5	17 x 75

No.	Name	X	Y	Bump size (μm)
301	G[22]	5988	394.5	17 x 75
302	G[24]	5967	294.5	17 x 75
303	G[26]	5946	394.5	17 x 75
304	G[28]	5925	294.5	17 x 75
305	G[30]	5904	394.5	17 x 75
306	G[32]	5883	294.5	17 x 75
307	G[34]	5862	394.5	17 x 75
308	G[36]	5841	294.5	17 x 75
309	G[38]	5820	394.5	17 x 75
310	G[40]	5799	294.5	17 x 75
311	G[42]	5778	394.5	17 x 75
312	G[44]	5757	294.5	17 x 75
313	G[46]	5736	394.5	17 x 75
314	G[48]	5715	294.5	17 x 75
315	G[50]	5694	394.5	17 x 75
316	G[52]	5673	294.5	17 x 75
317	G[54]	5652	394.5	17 x 75
318	G[56]	5631	294.5	17 x 75
319	G[58]	5610	394.5	17 x 75
320	G[60]	5589	294.5	17 x 75
321	G[62]	5568	394.5	17 x 75
322	G[64]	5547	294.5	17 x 75
323	G[66]	5526	394.5	17 x 75
324	G[68]	5505	294.5	17 x 75
325	G[70]	5484	394.5	17 x 75
326	G[72]	5463	294.5	17 x 75
327	G[74]	5442	394.5	17 x 75
328	G[76]	5421	294.5	17 x 75
329	G[78]	5400	394.5	17 x 75
330	G[80]	5379	294.5	17 x 75
331	G[82]	5358	394.5	17 x 75
332	G[84]	5337	294.5	17 x 75
333	G[86]	5316	394.5	17 x 75
334	G[88]	5295	294.5	17 x 75
335	G[90]	5274	394.5	17 x 75
336	G[92]	5253	294.5	17 x 75
337	G[94]	5232	394.5	17 x 75
338	G[96]	5211	294.5	17 x 75
339	G[98]	5190	394.5	17 x 75
340	G[100]	5169	294.5	17 x 75
341	G[102]	5148	394.5	17 x 75
342	G[104]	5127	294.5	17 x 75
343	G[106]	5106	394.5	17 x 75
344	G[108]	5085	294.5	17 x 75
345	G[110]	5064	394.5	17 x 75
346	G[112]	5043	294.5	17 x 75
347	G[114]	5022	394.5	17 x 75
348	G[116]	5001	294.5	17 x 75
349	G[118]	4980	394.5	17 x 75
350	G[120]	4959	294.5	17 x 75

No.	Name	X	Y	Bump size (μm)
351	G[122]	4938	394.5	17 x 75
352	G[124]	4917	294.5	17 x 75
353	G[126]	4896	394.5	17 x 75
354	G[128]	4875	294.5	17 x 75
355	G[130]	4854	394.5	17 x 75
356	G[132]	4833	294.5	17 x 75
357	G[134]	4812	394.5	17 x 75
358	G[136]	4791	294.5	17 x 75
359	G[138]	4770	394.5	17 x 75
360	G[140]	4749	294.5	17 x 75
361	G[142]	4728	394.5	17 x 75
362	G[144]	4707	294.5	17 x 75
363	G[146]	4686	394.5	17 x 75
364	G[148]	4665	294.5	17 x 75
365	G[150]	4644	394.5	17 x 75
366	G[152]	4623	294.5	17 x 75
367	G[154]	4602	394.5	17 x 75
368	G[156]	4581	294.5	17 x 75
369	G[158]	4560	394.5	17 x 75
370	G[160]	4539	294.5	17 x 75
371	G[162]	4518	394.5	17 x 75
372	G[164]	4497	294.5	17 x 75
373	G[166]	4476	394.5	17 x 75
374	G[168]	4455	294.5	17 x 75
375	G[170]	4434	394.5	17 x 75
376	G[172]	4413	294.5	17 x 75
377	G[174]	4392	394.5	17 x 75
378	G[176]	4371	294.5	17 x 75
379	G[178]	4350	394.5	17 x 75
380	G[180]	4329	294.5	17 x 75
381	G[182]	4308	394.5	17 x 75
382	G[184]	4287	294.5	17 x 75
383	G[186]	4266	394.5	17 x 75
384	G[188]	4245	294.5	17 x 75
385	G[190]	4224	394.5	17 x 75
386	G[192]	4203	294.5	17 x 75
387	G[194]	4182	394.5	17 x 75
388	G[196]	4161	294.5	17 x 75
389	G[198]	4140	394.5	17 x 75
390	G[200]	4119	294.5	17 x 75
391	G[202]	4098	394.5	17 x 75
392	G[204]	4077	294.5	17 x 75
393	G[206]	4056	394.5	17 x 75
394	G[208]	4035	294.5	17 x 75
395	G[210]	4014	394.5	17 x 75
396	G[212]	3993	294.5	17 x 75
397	G[214]	3972	394.5	17 x 75
398	G[216]	3951	294.5	17 x 75
399	G[218]	3930	394.5	17 x 75
400	G[220]	3909	294.5	17 x 75

No.	Name	X	Y	Bump size (μm)
401	G[222]	3888	394.5	17 x 75
402	G[224]	3867	294.5	17 x 75
403	G[226]	3846	394.5	17 x 75
404	G[228]	3825	294.5	17 x 75
405	G[230]	3804	394.5	17 x 75
406	G[232]	3783	294.5	17 x 75
407	G[234]	3762	394.5	17 x 75
408	G[236]	3741	294.5	17 x 75
409	G[238]	3720	394.5	17 x 75
410	G[240]	3699	294.5	17 x 75
411	G[242]	3678	394.5	17 x 75
412	G[244]	3657	294.5	17 x 75
413	G[246]	3636	394.5	17 x 75
414	G[248]	3615	294.5	17 x 75
415	G[250]	3594	394.5	17 x 75
416	G[252]	3573	294.5	17 x 75
417	G[254]	3552	394.5	17 x 75
418	G[256]	3531	294.5	17 x 75
419	G[258]	3510	394.5	17 x 75
420	G[260]	3489	294.5	17 x 75
421	G[262]	3468	394.5	17 x 75
422	G[264]	3447	294.5	17 x 75
423	G[266]	3426	394.5	17 x 75
424	G[268]	3405	294.5	17 x 75
425	G[270]	3384	394.5	17 x 75
426	G[272]	3363	294.5	17 x 75
427	G[274]	3342	394.5	17 x 75
428	G[276]	3321	294.5	17 x 75
429	G[278]	3300	394.5	17 x 75
430	G[280]	3279	294.5	17 x 75
431	G[282]	3258	394.5	17 x 75
432	G[284]	3237	294.5	17 x 75
433	G[286]	3216	394.5	17 x 75
434	G[288]	3195	294.5	17 x 75
435	G[290]	3174	394.5	17 x 75
436	G[292]	3153	294.5	17 x 75
437	G[294]	3132	394.5	17 x 75
438	G[296]	3111	294.5	17 x 75
439	G[298]	3090	394.5	17 x 75
440	NC	3069	294.5	17 x 75
441	NC	3048	394.5	17 x 75
442	NC	3027	294.5	17 x 75
443	NC	3006	394.5	17 x 75
444	NC	2985	294.5	17 x 75
445	NC	2964	394.5	17 x 75
446	NC	2943	294.5	17 x 75
447	NC	2835	394.5	16 x 75
448	NC	2821	294.5	16 x 75
449	VBD[2]	2807	394.5	16 x 75
450	S[0]	2793	294.5	16 x 75

No.	Name	X	Y	Bump size (μm)
451	S[1]	2779	394.5	16 x 75
452	S[2]	2765	294.5	16 x 75
453	S[3]	2751	394.5	16 x 75
454	S[4]	2737	294.5	16 x 75
455	S[5]	2723	394.5	16 x 75
456	S[6]	2709	294.5	16 x 75
457	S[7]	2695	394.5	16 x 75
458	S[8]	2681	294.5	16 x 75
459	S[9]	2667	394.5	16 x 75
460	S[10]	2653	294.5	16 x 75
461	S[11]	2639	394.5	16 x 75
462	S[12]	2625	294.5	16 x 75
463	S[13]	2611	394.5	16 x 75
464	S[14]	2597	294.5	16 x 75
465	S[15]	2583	394.5	16 x 75
466	S[16]	2569	294.5	16 x 75
467	S[17]	2555	394.5	16 x 75
468	S[18]	2541	294.5	16 x 75
469	S[19]	2527	394.5	16 x 75
470	S[20]	2513	294.5	16 x 75
471	S[21]	2499	394.5	16 x 75
472	S[22]	2485	294.5	16 x 75
473	S[23]	2471	394.5	16 x 75
474	S[24]	2457	294.5	16 x 75
475	S[25]	2443	394.5	16 x 75
476	S[26]	2429	294.5	16 x 75
477	S[27]	2415	394.5	16 x 75
478	S[28]	2401	294.5	16 x 75
479	S[29]	2387	394.5	16 x 75
480	S[30]	2373	294.5	16 x 75
481	S[31]	2359	394.5	16 x 75
482	S[32]	2345	294.5	16 x 75
483	S[33]	2331	394.5	16 x 75
484	S[34]	2317	294.5	16 x 75
485	S[35]	2303	394.5	16 x 75
486	S[36]	2289	294.5	16 x 75
487	S[37]	2275	394.5	16 x 75
488	S[38]	2261	294.5	16 x 75
489	S[39]	2247	394.5	16 x 75
490	S[40]	2233	294.5	16 x 75
491	S[41]	2219	394.5	16 x 75
492	S[42]	2205	294.5	16 x 75
493	S[43]	2191	394.5	16 x 75
494	S[44]	2177	294.5	16 x 75
495	S[45]	2163	394.5	16 x 75
496	S[46]	2149	294.5	16 x 75
497	S[47]	2135	394.5	16 x 75
498	S[48]	2121	294.5	16 x 75
499	S[49]	2107	394.5	16 x 75
500	S[50]	2093	294.5	16 x 75

No.	Name	X	Y	Bump size (μm)
501	S[51]	2079	394.5	16 x 75
502	S[52]	2065	294.5	16 x 75
503	S[53]	2051	394.5	16 x 75
504	S[54]	2037	294.5	16 x 75
505	S[55]	2023	394.5	16 x 75
506	S[56]	2009	294.5	16 x 75
507	S[57]	1995	394.5	16 x 75
508	S[58]	1981	294.5	16 x 75
509	S[59]	1967	394.5	16 x 75
510	S[60]	1953	294.5	16 x 75
511	S[61]	1939	394.5	16 x 75
512	S[62]	1925	294.5	16 x 75
513	S[63]	1911	394.5	16 x 75
514	S[64]	1897	294.5	16 x 75
515	S[65]	1883	394.5	16 x 75
516	S[66]	1869	294.5	16 x 75
517	S[67]	1855	394.5	16 x 75
518	S[68]	1841	294.5	16 x 75
519	S[69]	1827	394.5	16 x 75
520	S[70]	1813	294.5	16 x 75
521	S[71]	1799	394.5	16 x 75
522	S[72]	1785	294.5	16 x 75
523	S[73]	1771	394.5	16 x 75
524	S[74]	1757	294.5	16 x 75
525	S[75]	1743	394.5	16 x 75
526	S[76]	1729	294.5	16 x 75
527	S[77]	1715	394.5	16 x 75
528	S[78]	1701	294.5	16 x 75
529	S[79]	1687	394.5	16 x 75
530	S[80]	1673	294.5	16 x 75
531	S[81]	1659	394.5	16 x 75
532	S[82]	1645	294.5	16 x 75
533	S[83]	1631	394.5	16 x 75
534	S[84]	1617	294.5	16 x 75
535	S[85]	1603	394.5	16 x 75
536	S[86]	1589	294.5	16 x 75
537	S[87]	1575	394.5	16 x 75
538	S[88]	1561	294.5	16 x 75
539	S[89]	1547	394.5	16 x 75
540	S[90]	1533	294.5	16 x 75
541	S[91]	1519	394.5	16 x 75
542	S[92]	1505	294.5	16 x 75
543	S[93]	1491	394.5	16 x 75
544	S[94]	1477	294.5	16 x 75
545	S[95]	1463	394.5	16 x 75
546	S[96]	1449	294.5	16 x 75
547	S[97]	1435	394.5	16 x 75
548	S[98]	1421	294.5	16 x 75
549	S[99]	1407	394.5	16 x 75
550	S[100]	1393	294.5	16 x 75

No.	Name	X	Y	Bump size (μm)
551	S[101]	1379	394.5	16 x 75
552	S[102]	1365	294.5	16 x 75
553	S[103]	1351	394.5	16 x 75
554	S[104]	1337	294.5	16 x 75
555	S[105]	1323	394.5	16 x 75
556	S[106]	1309	294.5	16 x 75
557	S[107]	1295	394.5	16 x 75
558	S[108]	1281	294.5	16 x 75
559	S[109]	1267	394.5	16 x 75
560	S[110]	1253	294.5	16 x 75
561	S[111]	1239	394.5	16 x 75
562	S[112]	1225	294.5	16 x 75
563	S[113]	1211	394.5	16 x 75
564	S[114]	1197	294.5	16 x 75
565	S[115]	1183	394.5	16 x 75
566	S[116]	1169	294.5	16 x 75
567	S[117]	1155	394.5	16 x 75
568	S[118]	1141	294.5	16 x 75
569	S[119]	1127	394.5	16 x 75
570	S[120]	1113	294.5	16 x 75
571	S[121]	1099	394.5	16 x 75
572	S[122]	1085	294.5	16 x 75
573	S[123]	1071	394.5	16 x 75
574	S[124]	1057	294.5	16 x 75
575	S[125]	1043	394.5	16 x 75
576	S[126]	1029	294.5	16 x 75
577	S[127]	1015	394.5	16 x 75
578	S[128]	1001	294.5	16 x 75
579	S[129]	987	394.5	16 x 75
580	S[130]	973	294.5	16 x 75
581	S[131]	959	394.5	16 x 75
582	S[132]	945	294.5	16 x 75
583	S[133]	931	394.5	16 x 75
584	S[134]	917	294.5	16 x 75
585	S[135]	903	394.5	16 x 75
586	S[136]	889	294.5	16 x 75
587	S[137]	875	394.5	16 x 75
588	S[138]	861	294.5	16 x 75
589	S[139]	847	394.5	16 x 75
590	S[140]	833	294.5	16 x 75
591	S[141]	819	394.5	16 x 75
592	S[142]	805	294.5	16 x 75
593	S[143]	791	394.5	16 x 75
594	S[144]	777	294.5	16 x 75
595	S[145]	763	394.5	16 x 75
596	S[146]	749	294.5	16 x 75
597	S[147]	735	394.5	16 x 75
598	S[148]	721	294.5	16 x 75
599	S[149]	707	394.5	16 x 75
600	S[150]	693	294.5	16 x 75

No.	Name	X	Y	Bump size (μm)
601	S[151]	679	394.5	16 x 75
602	S[152]	665	294.5	16 x 75
603	S[153]	651	394.5	16 x 75
604	S[154]	637	294.5	16 x 75
605	S[155]	623	394.5	16 x 75
606	S[156]	609	294.5	16 x 75
607	S[157]	595	394.5	16 x 75
608	S[158]	581	294.5	16 x 75
609	S[159]	567	394.5	16 x 75
610	S[160]	553	294.5	16 x 75
611	S[161]	539	394.5	16 x 75
612	S[162]	525	294.5	16 x 75
613	S[163]	511	394.5	16 x 75
614	S[164]	497	294.5	16 x 75
615	S[165]	483	394.5	16 x 75
616	S[166]	469	294.5	16 x 75
617	S[167]	455	394.5	16 x 75
618	S[168]	441	294.5	16 x 75
619	S[169]	427	394.5	16 x 75
620	S[170]	413	294.5	16 x 75
621	S[171]	399	394.5	16 x 75
622	S[172]	385	294.5	16 x 75
623	S[173]	371	394.5	16 x 75
624	S[174]	357	294.5	16 x 75
625	S[175]	343	394.5	16 x 75
626	S[176]	329	294.5	16 x 75
627	S[177]	315	394.5	16 x 75
628	S[178]	301	294.5	16 x 75
629	S[179]	287	394.5	16 x 75
630	S[180]	273	294.5	16 x 75
631	S[181]	259	394.5	16 x 75
632	S[182]	245	294.5	16 x 75
633	S[183]	231	394.5	16 x 75
634	S[184]	217	294.5	16 x 75
635	S[185]	203	394.5	16 x 75
636	S[186]	189	294.5	16 x 75
637	S[187]	175	394.5	16 x 75
638	S[188]	161	294.5	16 x 75
639	S[189]	147	394.5	16 x 75
640	S[190]	133	294.5	16 x 75
641	S[191]	119	394.5	16 x 75
642	S[192]	105	294.5	16 x 75
643	S[193]	91	394.5	16 x 75
644	S[194]	77	294.5	16 x 75
645	S[195]	63	394.5	16 x 75
646	S[196]	49	294.5	16 x 75
647	S[197]	35	394.5	16 x 75
648	S[198]	21	294.5	16 x 75
649	S[199]	7	394.5	16 x 75
650	S[200]	-7	294.5	16 x 75

No.	Name	X	Y	Bump size (μm)
651	S[201]	-21	394.5	16 x 75
652	S[202]	-35	294.5	16 x 75
653	S[203]	-49	394.5	16 x 75
654	S[204]	-63	294.5	16 x 75
655	S[205]	-77	394.5	16 x 75
656	S[206]	-91	294.5	16 x 75
657	S[207]	-105	394.5	16 x 75
658	S[208]	-119	294.5	16 x 75
659	S[209]	-133	394.5	16 x 75
660	S[210]	-147	294.5	16 x 75
661	S[211]	-161	394.5	16 x 75
662	S[212]	-175	294.5	16 x 75
663	S[213]	-189	394.5	16 x 75
664	S[214]	-203	294.5	16 x 75
665	S[215]	-217	394.5	16 x 75
666	S[216]	-231	294.5	16 x 75
667	S[217]	-245	394.5	16 x 75
668	S[218]	-259	294.5	16 x 75
669	S[219]	-273	394.5	16 x 75
670	S[220]	-287	294.5	16 x 75
671	S[221]	-301	394.5	16 x 75
672	S[222]	-315	294.5	16 x 75
673	S[223]	-329	394.5	16 x 75
674	S[224]	-343	294.5	16 x 75
675	S[225]	-357	394.5	16 x 75
676	S[226]	-371	294.5	16 x 75
677	S[227]	-385	394.5	16 x 75
678	S[228]	-399	294.5	16 x 75
679	S[229]	-413	394.5	16 x 75
680	S[230]	-427	294.5	16 x 75
681	S[231]	-441	394.5	16 x 75
682	S[232]	-455	294.5	16 x 75
683	S[233]	-469	394.5	16 x 75
684	S[234]	-483	294.5	16 x 75
685	S[235]	-497	394.5	16 x 75
686	S[236]	-511	294.5	16 x 75
687	S[237]	-525	394.5	16 x 75
688	S[238]	-539	294.5	16 x 75
689	S[239]	-553	394.5	16 x 75
690	S[240]	-567	294.5	16 x 75
691	S[241]	-581	394.5	16 x 75
692	S[242]	-595	294.5	16 x 75
693	S[243]	-609	394.5	16 x 75
694	S[244]	-623	294.5	16 x 75
695	S[245]	-637	394.5	16 x 75
696	S[246]	-651	294.5	16 x 75
697	S[247]	-665	394.5	16 x 75
698	S[248]	-679	294.5	16 x 75
699	S[249]	-693	394.5	16 x 75
700	S[250]	-707	294.5	16 x 75

No.	Name	X	Y	Bump size (μm)
701	S[251]	-721	394.5	16 x 75
702	S[252]	-735	294.5	16 x 75
703	S[253]	-749	394.5	16 x 75
704	S[254]	-763	294.5	16 x 75
705	S[255]	-777	394.5	16 x 75
706	S[256]	-791	294.5	16 x 75
707	S[257]	-805	394.5	16 x 75
708	S[258]	-819	294.5	16 x 75
709	S[259]	-833	394.5	16 x 75
710	S[260]	-847	294.5	16 x 75
711	S[261]	-861	394.5	16 x 75
712	S[262]	-875	294.5	16 x 75
713	S[263]	-889	394.5	16 x 75
714	S[264]	-903	294.5	16 x 75
715	S[265]	-917	394.5	16 x 75
716	S[266]	-931	294.5	16 x 75
717	S[267]	-945	394.5	16 x 75
718	S[268]	-959	294.5	16 x 75
719	S[269]	-973	394.5	16 x 75
720	S[270]	-987	294.5	16 x 75
721	S[271]	-1001	394.5	16 x 75
722	S[272]	-1015	294.5	16 x 75
723	S[273]	-1029	394.5	16 x 75
724	S[274]	-1043	294.5	16 x 75
725	S[275]	-1057	394.5	16 x 75
726	S[276]	-1071	294.5	16 x 75
727	S[277]	-1085	394.5	16 x 75
728	S[278]	-1099	294.5	16 x 75
729	S[279]	-1113	394.5	16 x 75
730	S[280]	-1127	294.5	16 x 75
731	S[281]	-1141	394.5	16 x 75
732	S[282]	-1155	294.5	16 x 75
733	S[283]	-1169	394.5	16 x 75
734	S[284]	-1183	294.5	16 x 75
735	S[285]	-1197	394.5	16 x 75
736	S[286]	-1211	294.5	16 x 75
737	S[287]	-1225	394.5	16 x 75
738	S[288]	-1239	294.5	16 x 75
739	S[289]	-1253	394.5	16 x 75
740	S[290]	-1267	294.5	16 x 75
741	S[291]	-1281	394.5	16 x 75
742	S[292]	-1295	294.5	16 x 75
743	S[293]	-1309	394.5	16 x 75
744	S[294]	-1323	294.5	16 x 75
745	S[295]	-1337	394.5	16 x 75
746	S[296]	-1351	294.5	16 x 75
747	S[297]	-1365	394.5	16 x 75
748	S[298]	-1379	294.5	16 x 75
749	S[299]	-1393	394.5	16 x 75
750	S[300]	-1407	294.5	16 x 75

No.	Name	X	Y	Bump size (μm)
751	S[301]	-1421	394.5	16 x 75
752	S[302]	-1435	294.5	16 x 75
753	S[303]	-1449	394.5	16 x 75
754	S[304]	-1463	294.5	16 x 75
755	S[305]	-1477	394.5	16 x 75
756	S[306]	-1491	294.5	16 x 75
757	S[307]	-1505	394.5	16 x 75
758	S[308]	-1519	294.5	16 x 75
759	S[309]	-1533	394.5	16 x 75
760	S[310]	-1547	294.5	16 x 75
761	S[311]	-1561	394.5	16 x 75
762	S[312]	-1575	294.5	16 x 75
763	S[313]	-1589	394.5	16 x 75
764	S[314]	-1603	294.5	16 x 75
765	S[315]	-1617	394.5	16 x 75
766	S[316]	-1631	294.5	16 x 75
767	S[317]	-1645	394.5	16 x 75
768	S[318]	-1659	294.5	16 x 75
769	S[319]	-1673	394.5	16 x 75
770	S[320]	-1687	294.5	16 x 75
771	S[321]	-1701	394.5	16 x 75
772	S[322]	-1715	294.5	16 x 75
773	S[323]	-1729	394.5	16 x 75
774	S[324]	-1743	294.5	16 x 75
775	S[325]	-1757	394.5	16 x 75
776	S[326]	-1771	294.5	16 x 75
777	S[327]	-1785	394.5	16 x 75
778	S[328]	-1799	294.5	16 x 75
779	S[329]	-1813	394.5	16 x 75
780	S[330]	-1827	294.5	16 x 75
781	S[331]	-1841	394.5	16 x 75
782	S[332]	-1855	294.5	16 x 75
783	S[333]	-1869	394.5	16 x 75
784	S[334]	-1883	294.5	16 x 75
785	S[335]	-1897	394.5	16 x 75
786	S[336]	-1911	294.5	16 x 75
787	S[337]	-1925	394.5	16 x 75
788	S[338]	-1939	294.5	16 x 75
789	S[339]	-1953	394.5	16 x 75
790	S[340]	-1967	294.5	16 x 75
791	S[341]	-1981	394.5	16 x 75
792	S[342]	-1995	294.5	16 x 75
793	S[343]	-2009	394.5	16 x 75
794	S[344]	-2023	294.5	16 x 75
795	S[345]	-2037	394.5	16 x 75
796	S[346]	-2051	294.5	16 x 75
797	S[347]	-2065	394.5	16 x 75
798	S[348]	-2079	294.5	16 x 75
799	S[349]	-2093	394.5	16 x 75
800	S[350]	-2107	294.5	16 x 75

No.	Name	X	Y	Bump size (μm)
801	S[351]	-2121	394.5	16 x 75
802	S[352]	-2135	294.5	16 x 75
803	S[353]	-2149	394.5	16 x 75
804	S[354]	-2163	294.5	16 x 75
805	S[355]	-2177	394.5	16 x 75
806	S[356]	-2191	294.5	16 x 75
807	S[357]	-2205	394.5	16 x 75
808	S[358]	-2219	294.5	16 x 75
809	S[359]	-2233	394.5	16 x 75
810	S[360]	-2247	294.5	16 x 75
811	S[361]	-2261	394.5	16 x 75
812	S[362]	-2275	294.5	16 x 75
813	S[363]	-2289	394.5	16 x 75
814	S[364]	-2303	294.5	16 x 75
815	S[365]	-2317	394.5	16 x 75
816	S[366]	-2331	294.5	16 x 75
817	S[367]	-2345	394.5	16 x 75
818	S[368]	-2359	294.5	16 x 75
819	S[369]	-2373	394.5	16 x 75
820	S[370]	-2387	294.5	16 x 75
821	S[371]	-2401	394.5	16 x 75
822	S[372]	-2415	294.5	16 x 75
823	S[373]	-2429	394.5	16 x 75
824	S[374]	-2443	294.5	16 x 75
825	S[375]	-2457	394.5	16 x 75
826	S[376]	-2471	294.5	16 x 75
827	S[377]	-2485	394.5	16 x 75
828	S[378]	-2499	294.5	16 x 75
829	S[379]	-2513	394.5	16 x 75
830	S[380]	-2527	294.5	16 x 75
831	S[381]	-2541	394.5	16 x 75
832	S[382]	-2555	294.5	16 x 75
833	S[383]	-2569	394.5	16 x 75
834	S[384]	-2583	294.5	16 x 75
835	S[385]	-2597	394.5	16 x 75
836	S[386]	-2611	294.5	16 x 75
837	S[387]	-2625	394.5	16 x 75
838	S[388]	-2639	294.5	16 x 75
839	S[389]	-2653	394.5	16 x 75
840	S[390]	-2667	294.5	16 x 75
841	S[391]	-2681	394.5	16 x 75
842	S[392]	-2695	294.5	16 x 75
843	S[393]	-2709	394.5	16 x 75
844	S[394]	-2723	294.5	16 x 75
845	S[395]	-2737	394.5	16 x 75
846	S[396]	-2751	294.5	16 x 75
847	S[397]	-2765	394.5	16 x 75
848	S[398]	-2779	294.5	16 x 75
849	S[399]	-2793	394.5	16 x 75
850	VBD[1]	-2807	294.5	16 x 75

No.	Name	X	Y	Bump size (μm)
851	NC	-2821	394.5	16 x 75
852	NC	-2835	294.5	16 x 75
853	NC	-2943	394.5	17 x 75
854	NC	-2964	294.5	17 x 75
855	NC	-2985	394.5	17 x 75
856	NC	-3006	294.5	17 x 75
857	NC	-3027	394.5	17 x 75
858	NC	-3048	294.5	17 x 75
859	NC	-3069	394.5	17 x 75
860	G[299]	-3090	294.5	17 x 75
861	G[297]	-3111	394.5	17 x 75
862	G[295]	-3132	294.5	17 x 75
863	G[293]	-3153	394.5	17 x 75
864	G[291]	-3174	294.5	17 x 75
865	G[289]	-3195	394.5	17 x 75
866	G[287]	-3216	294.5	17 x 75
867	G[285]	-3237	394.5	17 x 75
868	G[283]	-3258	294.5	17 x 75
869	G[281]	-3279	394.5	17 x 75
870	G[279]	-3300	294.5	17 x 75
871	G[277]	-3321	394.5	17 x 75
872	G[275]	-3342	294.5	17 x 75
873	G[273]	-3363	394.5	17 x 75
874	G[271]	-3384	294.5	17 x 75
875	G[269]	-3405	394.5	17 x 75
876	G[267]	-3426	294.5	17 x 75
877	G[265]	-3447	394.5	17 x 75
878	G[263]	-3468	294.5	17 x 75
879	G[261]	-3489	394.5	17 x 75
880	G[259]	-3510	294.5	17 x 75
881	G[257]	-3531	394.5	17 x 75
882	G[255]	-3552	294.5	17 x 75
883	G[253]	-3573	394.5	17 x 75
884	G[251]	-3594	294.5	17 x 75
885	G[249]	-3615	394.5	17 x 75
886	G[247]	-3636	294.5	17 x 75
887	G[245]	-3657	394.5	17 x 75
888	G[243]	-3678	294.5	17 x 75
889	G[241]	-3699	394.5	17 x 75
890	G[239]	-3720	294.5	17 x 75
891	G[237]	-3741	394.5	17 x 75
892	G[235]	-3762	294.5	17 x 75
893	G[233]	-3783	394.5	17 x 75
894	G[231]	-3804	294.5	17 x 75
895	G[229]	-3825	394.5	17 x 75
896	G[227]	-3846	294.5	17 x 75
897	G[225]	-3867	394.5	17 x 75
898	G[223]	-3888	294.5	17 x 75
899	G[221]	-3909	394.5	17 x 75
900	G[219]	-3930	294.5	17 x 75

No.	Name	X	Y	Bump size (μm)
901	G[217]	-3951	394.5	17 x 75
902	G[215]	-3972	294.5	17 x 75
903	G[213]	-3993	394.5	17 x 75
904	G[211]	-4014	294.5	17 x 75
905	G[209]	-4035	394.5	17 x 75
906	G[207]	-4056	294.5	17 x 75
907	G[205]	-4077	394.5	17 x 75
908	G[203]	-4098	294.5	17 x 75
909	G[201]	-4119	394.5	17 x 75
910	G[199]	-4140	294.5	17 x 75
911	G[197]	-4161	394.5	17 x 75
912	G[195]	-4182	294.5	17 x 75
913	G[193]	-4203	394.5	17 x 75
914	G[191]	-4224	294.5	17 x 75
915	G[189]	-4245	394.5	17 x 75
916	G[187]	-4266	294.5	17 x 75
917	G[185]	-4287	394.5	17 x 75
918	G[183]	-4308	294.5	17 x 75
919	G[181]	-4329	394.5	17 x 75
920	G[179]	-4350	294.5	17 x 75
921	G[177]	-4371	394.5	17 x 75
922	G[175]	-4392	294.5	17 x 75
923	G[173]	-4413	394.5	17 x 75
924	G[171]	-4434	294.5	17 x 75
925	G[169]	-4455	394.5	17 x 75
926	G[167]	-4476	294.5	17 x 75
927	G[165]	-4497	394.5	17 x 75
928	G[163]	-4518	294.5	17 x 75
929	G[161]	-4539	394.5	17 x 75
930	G[159]	-4560	294.5	17 x 75
931	G[157]	-4581	394.5	17 x 75
932	G[155]	-4602	294.5	17 x 75
933	G[153]	-4623	394.5	17 x 75
934	G[151]	-4644	294.5	17 x 75
935	G[149]	-4665	394.5	17 x 75
936	G[147]	-4686	294.5	17 x 75
937	G[145]	-4707	394.5	17 x 75
938	G[143]	-4728	294.5	17 x 75
939	G[141]	-4749	394.5	17 x 75
940	G[139]	-4770	294.5	17 x 75
941	G[137]	-4791	394.5	17 x 75
942	G[135]	-4812	294.5	17 x 75
943	G[133]	-4833	394.5	17 x 75
944	G[131]	-4854	294.5	17 x 75
945	G[129]	-4875	394.5	17 x 75
946	G[127]	-4896	294.5	17 x 75
947	G[125]	-4917	394.5	17 x 75
948	G[123]	-4938	294.5	17 x 75
949	G[121]	-4959	394.5	17 x 75
950	G[119]	-4980	294.5	17 x 75

No.	Name	X	Y	Bump size (μm)
951	G[117]	-5001	394.5	17 x 75
952	G[115]	-5022	294.5	17 x 75
953	G[113]	-5043	394.5	17 x 75
954	G[111]	-5064	294.5	17 x 75
955	G[109]	-5085	394.5	17 x 75
956	G[107]	-5106	294.5	17 x 75
957	G[105]	-5127	394.5	17 x 75
958	G[103]	-5148	294.5	17 x 75
959	G[101]	-5169	394.5	17 x 75
960	G[99]	-5190	294.5	17 x 75
961	G[97]	-5211	394.5	17 x 75
962	G[95]	-5232	294.5	17 x 75
963	G[93]	-5253	394.5	17 x 75
964	G[91]	-5274	294.5	17 x 75
965	G[89]	-5295	394.5	17 x 75
966	G[87]	-5316	294.5	17 x 75
967	G[85]	-5337	394.5	17 x 75
968	G[83]	-5358	294.5	17 x 75
969	G[81]	-5379	394.5	17 x 75
970	G[79]	-5400	294.5	17 x 75
971	G[77]	-5421	394.5	17 x 75
972	G[75]	-5442	294.5	17 x 75
973	G[73]	-5463	394.5	17 x 75
974	G[71]	-5484	294.5	17 x 75
975	G[69]	-5505	394.5	17 x 75
976	G[67]	-5526	294.5	17 x 75
977	G[65]	-5547	394.5	17 x 75
978	G[63]	-5568	294.5	17 x 75
979	G[61]	-5589	394.5	17 x 75
980	G[59]	-5610	294.5	17 x 75
981	G[57]	-5631	394.5	17 x 75
982	G[55]	-5652	294.5	17 x 75
983	G[53]	-5673	394.5	17 x 75
984	G[51]	-5694	294.5	17 x 75
985	G[49]	-5715	394.5	17 x 75
986	G[47]	-5736	294.5	17 x 75
987	G[45]	-5757	394.5	17 x 75
988	G[43]	-5778	294.5	17 x 75
989	G[41]	-5799	394.5	17 x 75
990	G[39]	-5820	294.5	17 x 75
991	G[37]	-5841	394.5	17 x 75
992	G[35]	-5862	294.5	17 x 75
993	G[33]	-5883	394.5	17 x 75
994	G[31]	-5904	294.5	17 x 75
995	G[29]	-5925	394.5	17 x 75
996	G[27]	-5946	294.5	17 x 75
997	G[25]	-5967	394.5	17 x 75
998	G[23]	-5988	294.5	17 x 75
999	G[21]	-6009	394.5	17 x 75
1000	G[19]	-6030	294.5	17 x 75

No.	Name	X	Y	Bump size (μm)
1001	G[17]	-6051	394.5	17 x 75
1002	G[15]	-6072	294.5	17 x 75
1003	G[13]	-6093	394.5	17 x 75
1004	G[11]	-6114	294.5	17 x 75
1005	G[9]	-6135	394.5	17 x 75
1006	G[7]	-6156	294.5	17 x 75
1007	G[5]	-6177	394.5	17 x 75
1008	G[3]	-6198	294.5	17 x 75
1009	G[1]	-6219	394.5	17 x 75
1010	NC	-6240	294.5	17 x 75
1011	NC	-6261	394.5	17 x 75
1012	NC	-6282	294.5	17 x 75
1013	NC	-6303	394.5	17 x 75
1014	NC	-6324	294.5	17 x 75
1015	NC	-6345	394.5	17 x 75

9.4 Alignment mark center coordinates

Name	X	Y
L_AMK	-6465	371
R_AMK	6465	371

10. Ordering Information

Part no. ⁽¹⁾	Package
HX8717-A00XP <u>D</u> xxxxy	00: mean chip version X: mean fab code PD: mean COG xxx: mean chip thickness y: mean value of bump compensation

Note: (1) Part no. HX8717-A00PPD3002 is Ver. A IC,

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