JADARD

JD79651C

Data Sheet

All-in-one driver with
TCON for Color application

Version 1.0.1
2021/04/09

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All-in-one driver with TCON for Color application

1. GENERAL DESCRIPTION

This driver is an all-in-one driver with timing controller for color application. The outputs have 1-bit white/black and 1-bit red resolution output per pixel. The timing controller provides control signals for the source driver and gate drivers.

The DC-DC controller allows to generate the source output voltage VSH/VSL (+/-6.4V~+/-15V). The chip also includes an output buffer for the supply of the common electrode (VCOMAC or VCOMDC). The system is configurable through a 3-wire/4-wire(SPI) serial.

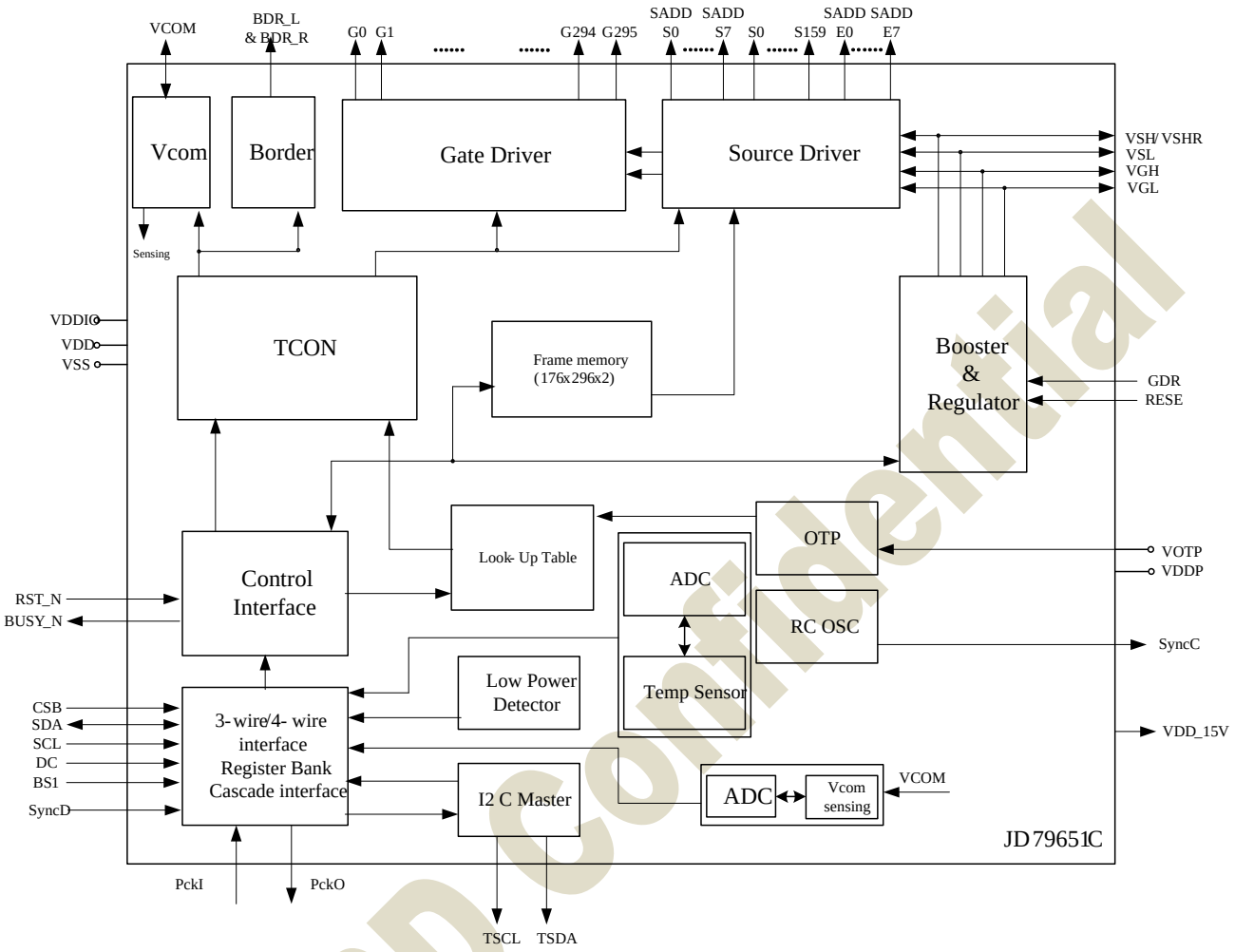
2. FEATURES

- System-on-chip (SOC) for color application
- Timing controller support several all resolution (maximum resolution 176x296)
- Support source & gate driver function:
  - 176 Outputs source driver with 1-bit white/black & 1-bit red per pixel:
    - Output dynamic range: VSH (+6.4V~+15V) and VSL (-6.4V~-15V) (programmable, black/white)

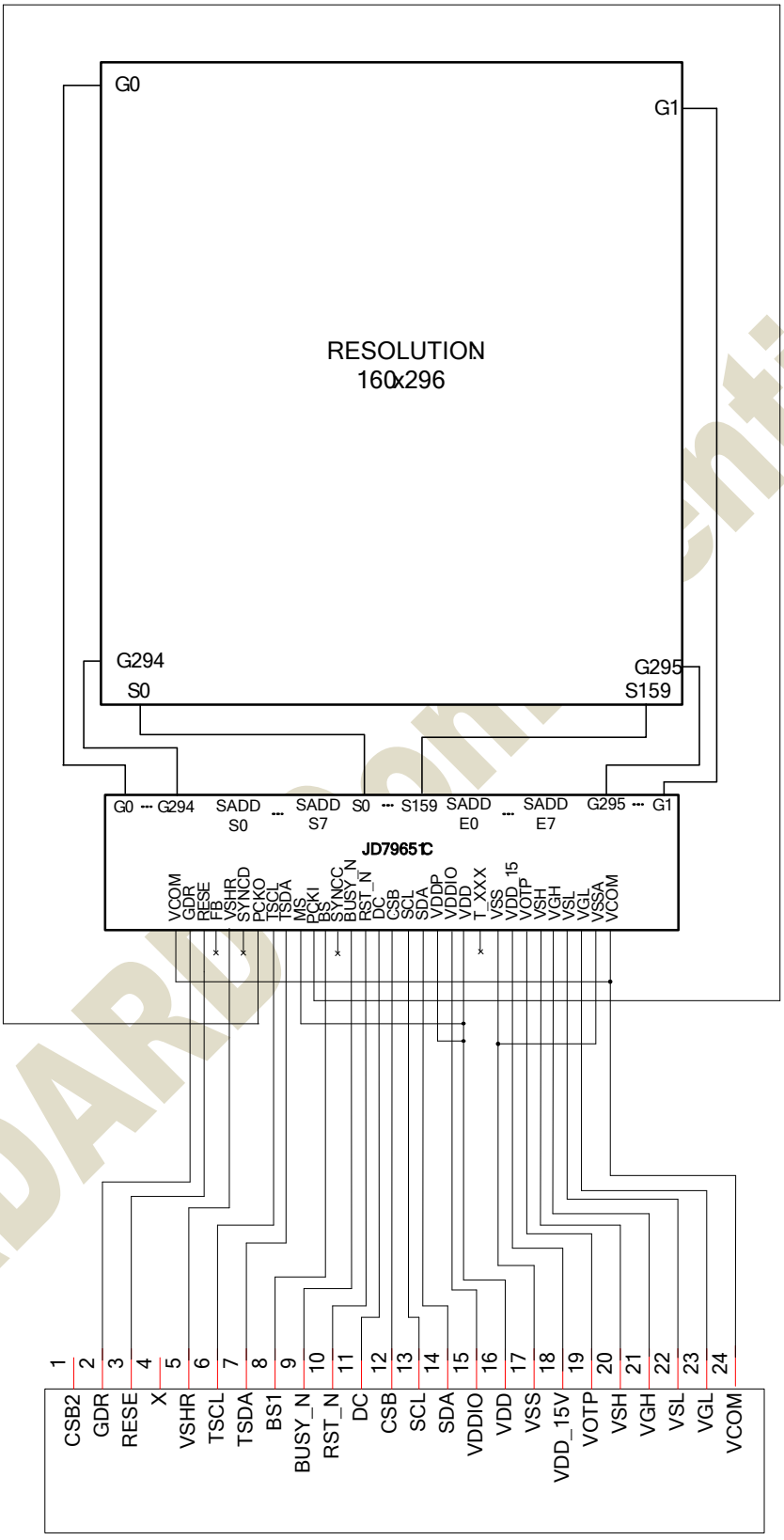
      VSHR (+2.4V~+15V) (programmable, red)
    - Left and Right shift capability
  - 296 Output gate driver:
    - Output dynamic range: VGH (+15V~+20V) and VGL (-15V~-20V)
    - Up and Down shift capability
- Common electrode level
  - AC-VCOM and DC-VCOM
  - Support sensing function (6-bit digital status)
  - Support LUT
- Charge Pump: On-chip booster and regulator
- Built in Frame memory maximum: (176x 296 x 1 bit) x 2 SRAM
- Built in temperature sensor:
  - On-Chip: -25~0 ^{o}C & 30~50 ^{o}C ± 2.0^{o}C, 0~30^{o}C ± 1.0^{o}C / 10-bit status
  - Off-Chip: -55~125^{o}C ± 2.0^{o}C / 11-bit status (I^2C/LM75)
- Support LPD, Low Power detection (V_{DD}< 2.2V~2.5V)
- PLL : On-chip RC oscillator
- 3-wire/4-wire (SPI) serial interface for system configuration
- Digital supply voltage: 2.3~3.6V
- OTP: 6K-byte OTP for LUT
- Partial update

- Support cascade
- Package-COG

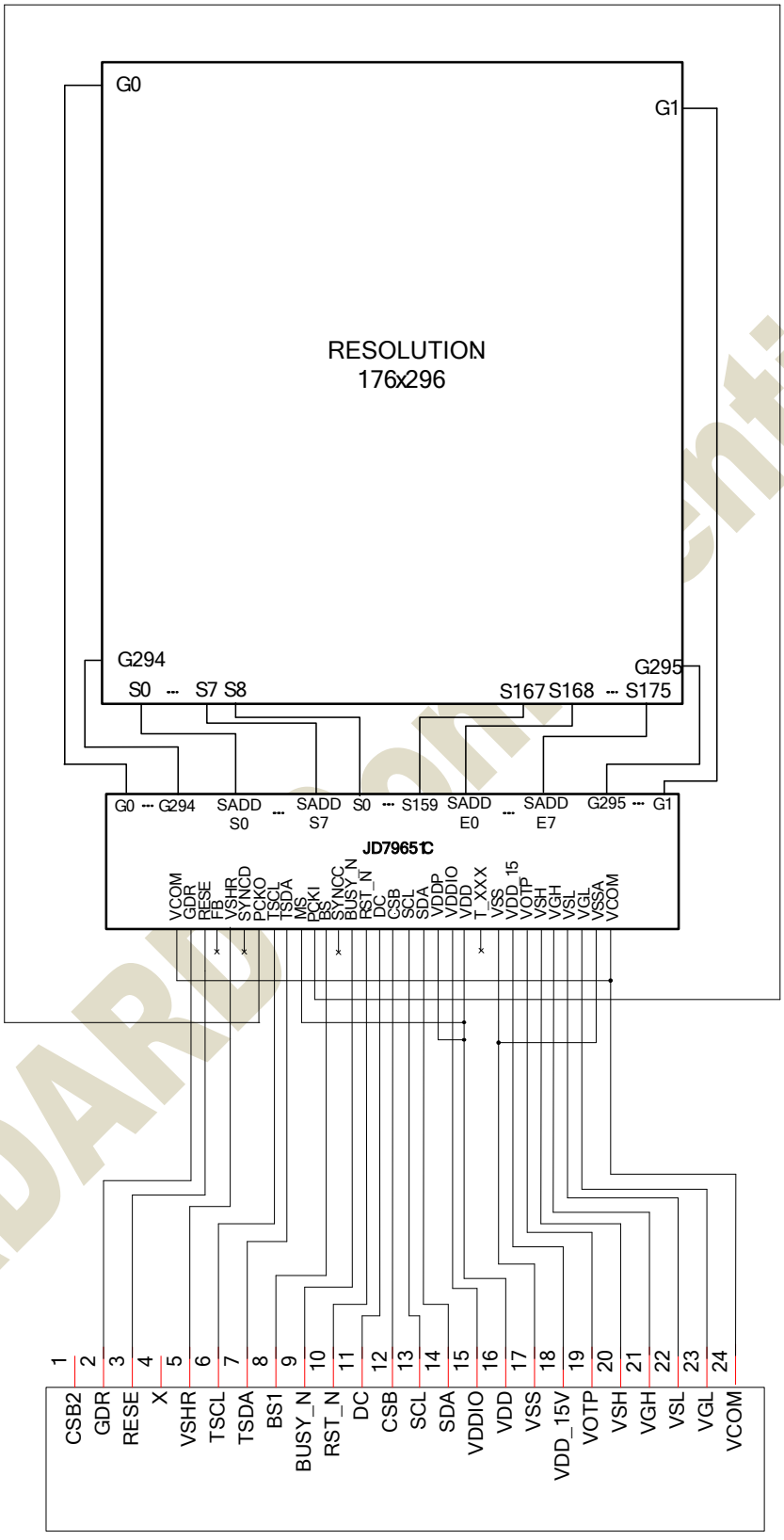
3. BLOCK DIAGRAM



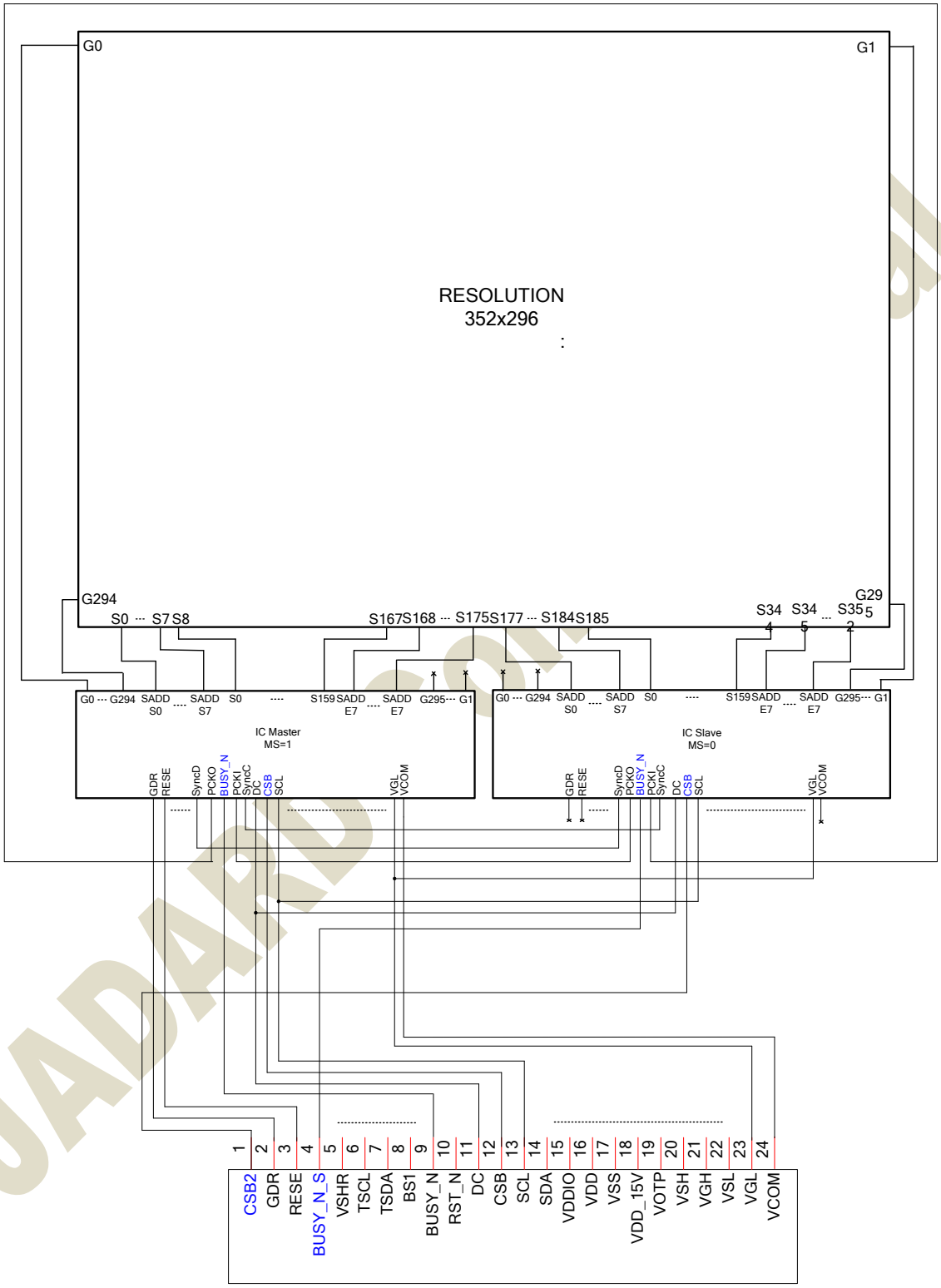
Normal type 1 (source resolution below 160ch.)



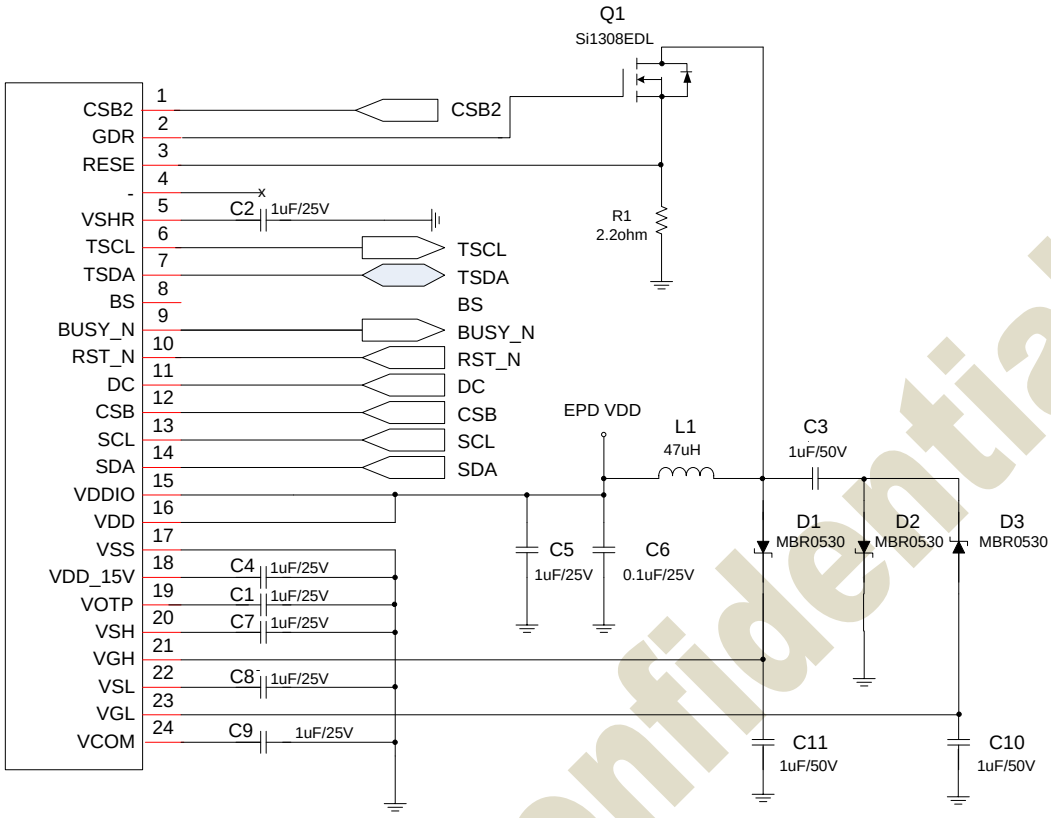
Normal type 2 (source resolution 176ch.)

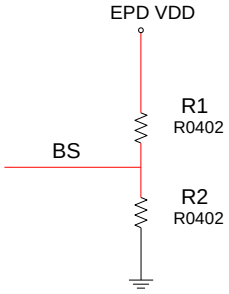


Cascade type



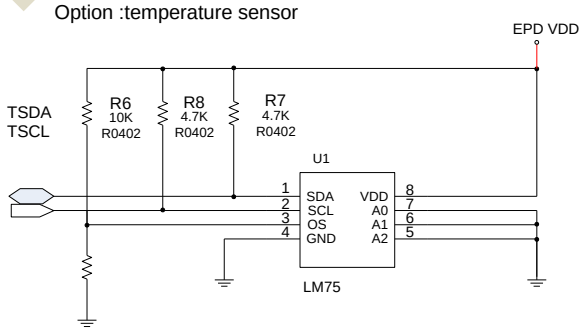
4. APPLICATION CIRCUIT





	R1	R2
3- wire SPI (CSB, SDA, SCL)	10K	NC
4-wire SPI (DC, CSB, SDA, SCL)	NC	10K

Option :temperature sensor

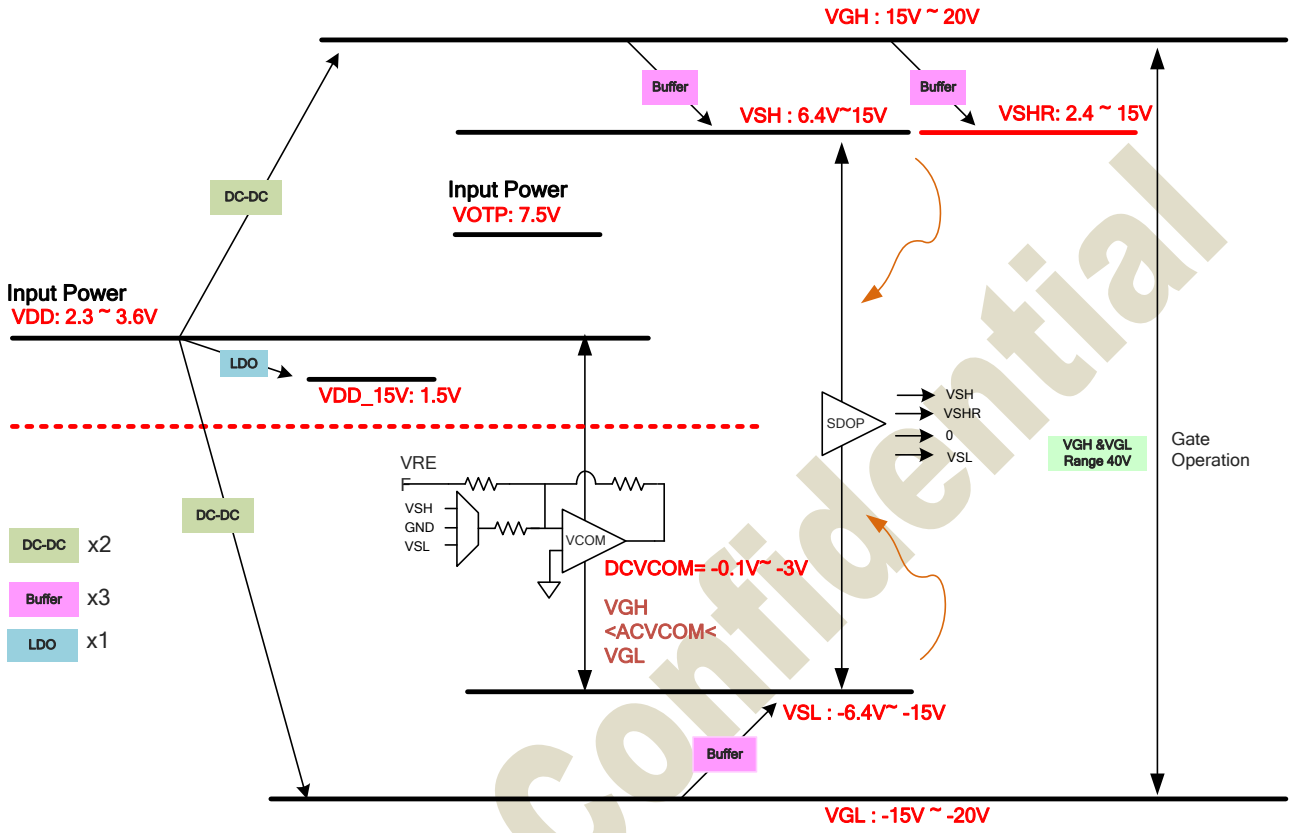


Reference table of the device:

Device no.	Value	Reference
C1, C2, C4, C5, C7, C8	1uF	0603, X5R/X7R, voltage rating : 25V
C3, C10, C11	1uF	0603, X5R/X7R, voltage rating : 50V
C6	0.1uF	0603, X5R/X7R, voltage rating : 25V
C9	1uF	0603, X5R/X7R, voltage rating : 25V
R1	2.2Ω	0603, +/-1% variation
Q1	NMOS	Si1308EDL、Si1304BDL - Drain-source break volatage≧30V - Gate-source threshold voltage≦1.5V - Drain-source on-state resistance<400mΩ
L1	47uH	NR4018T470M、CDRH2D18/LDNP-470NC - Fixed - Maximum DC current~420mA - Maximum DC resistance~650mΩ
D1~D3	Diode	MBR0530 - Reverse DC voltage≧30V - Forward current≧500mA - Forward voltage≦430mV

5. APPLICATION POWER CIRCUIT

5.1 Power Generation



6. PIN DESCRIPTION

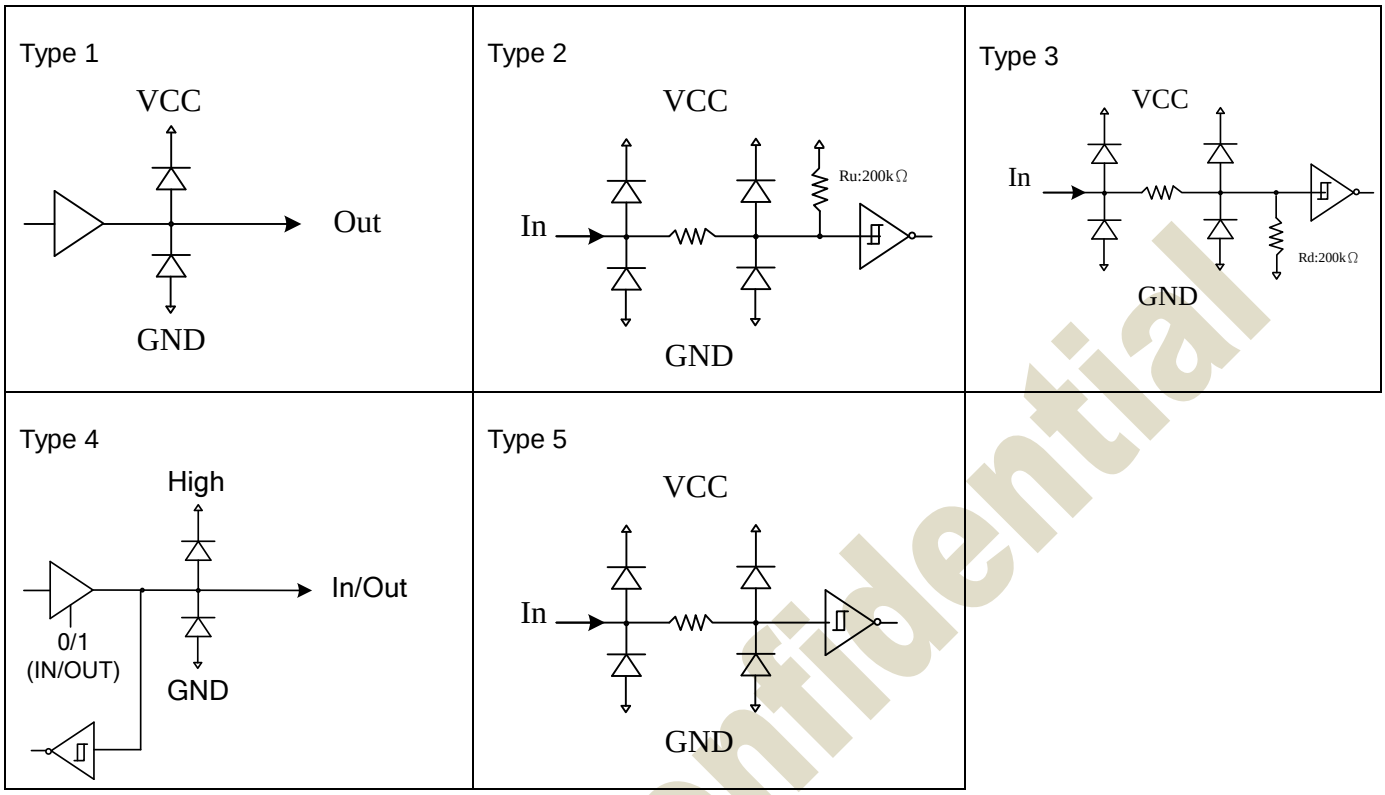
6.1 Pin define

Pin Name	Pin Type	I/O Structure	Description
Serial Communication Interface			
CSB	I	Type 5	Serial communication chip select.
SDA	I/O	Type 4	Serial communication data input.
SCL	I	Type 5	Serial communication clock input.
DC	I	Type 5	Serial communication Command/Data input L: Command H: data Connect to VDD if BS=High.
Control Interface			
RST_N	I	Type 2	Global reset pin. Low reset. **(normal pull high)** When RST_N become low, driver will reset. All register will reset to default value. all driver function will disable. SD output and VCOM will be released to floating.
BUSY_N	O	Type1	This pin indicates the driver status. BUSY_N= ”0” : Driver is busy, data/VCOM is transforming. BUSY_N= ”1” : non-busy. Host side can send command/data to driver.
BS	I	Type 5	Input interface setting. Select 3 wire/ 4 wire SPI interface L: 4-wire IF H:3-wire IF
TSCL	O	Type1	I^2C clock for external temperature sensor
TSDA	I/O	Type 4	I^2C data for external temperature sensor
MS	I	Type 5	Master/Slave selection for cascade mode Low: Slave High: Master In single-chip mode, MS should be connect to VDD
Output Driver			
S[159:0]	O	-	Source driver output signals.
S_ADDS/E[7:0]	O	-	Source driver output signals.
G[295:0]	O	-	Gate driver output signals..
Border			
VBD[4:1]	O	-	Border output pins. It outputs black WF.
VCOM GENERATOR			
VCOM	O	Type 1	VCOM output. VCOM has follow four voltage state: 1. (-VCM_DC) v 2. (VSH-VCM_DC) 3. (VSL-VCM_DC) v. 4. Floating
Power Circuit			
GDR	O	-	This pin is N-MOS gate control.
RESE	P	-	Current sense input for control loop.
FB	P	-	Keep open
VGH	P	Type 5	Positive gate voltage
VGL	P	Type 4	Negative gate voltage.
VSH	P	Type 1	Positive source voltage
VSL	P	Type 1	Negative source voltage.
VSHR	P	Type 1	Positive source voltage for Red
Power Supply			

Pin Name	Pin Type	I/O Structure	Description
VDDP	P	-	DCDC power input
VDD	P	-	Digital/Analog power.
VSS	P	-	Digital ground
VSSA	P		Analog Ground
VDDIO	P	-	IO voltage supply
VDD_15V	P	-	1.5V voltage input &output
VOTP	P	-	OTP program power (8.25V)
Reserved Pins			
TP [21:0]	I/O	-	Test pin
SyncD	I/O	Type 4	Cascade Data signal
SyncC	I/O	Type 4	Cascade Clock signal
PckI	I	Type 3	Break panel check input. Leave open if it is not used.
PckO	O	Type 1	Break panel check output. Leave open if it is not used.

Note: I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output, I/O: Input / Output. PS: Power Setting, C: Capacitor pin.

6.2 I/O Pin Structure



6.3 Value of wiring resistance to each pin

Pin name	Wiring resistance value(Ω)	Pin name	Wiring resistance value(Ω)
VCOM	5ohm	TSDA	100ohm
VGL	5ohm	TSCL	100ohm
VSHR	5ohm	BUSY_N	100ohm
VGH	5ohm	BS	100ohm
VSH	5ohm	RESE	5ohm
VOTP	5ohm	GDR	5ohm
VDD_15V	5ohm	SDA	100ohm
VSSA	5ohm	SCL	100ohm
VDDIO	5ohm	CSB	100ohm
VSS	5ohm	DC	100ohm
VDDP	5ohm	RST_N	100ohm
VDD	5ohm	SyncD	100ohm
VSL	5ohm	SyncC	100ohm
MS	100ohm	PCKI	100ohm
TP [21:0]	100ohm	PCKO	100ohm

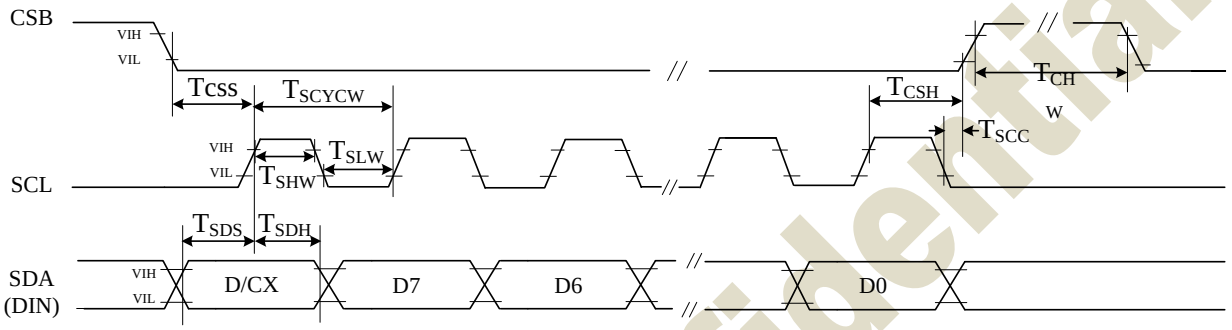
7. SPI COMMAND DESCRIPTION

JD79651 use the 3-wire/4-wire serial port as communication interface for all the function and command setting.

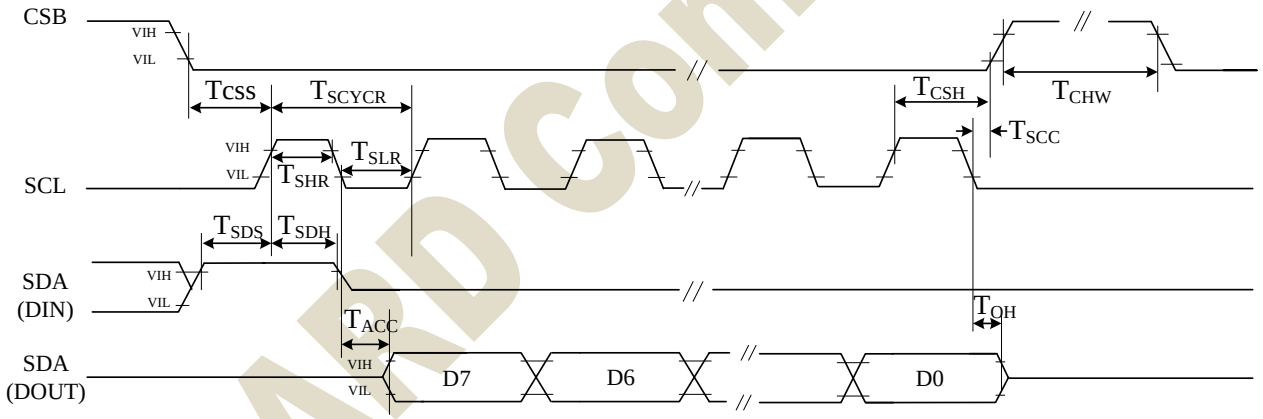
JD79651 3-wire/4-wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-wire/4-wire bus itself.

Under read mode, 3-wire/4-wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-wire/4-wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.

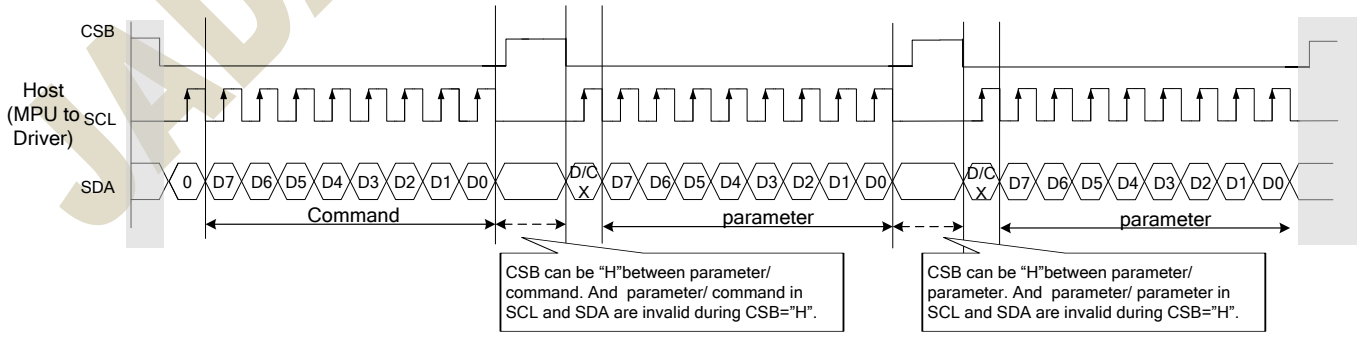
7.1 “3-Wire” Serial Port Interface



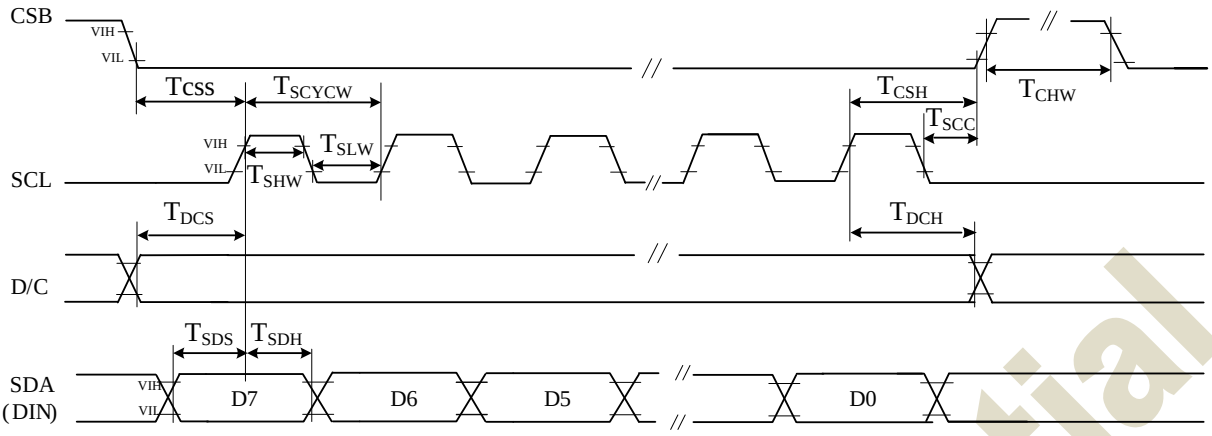
3 pin serial interface characteristics (write mode)



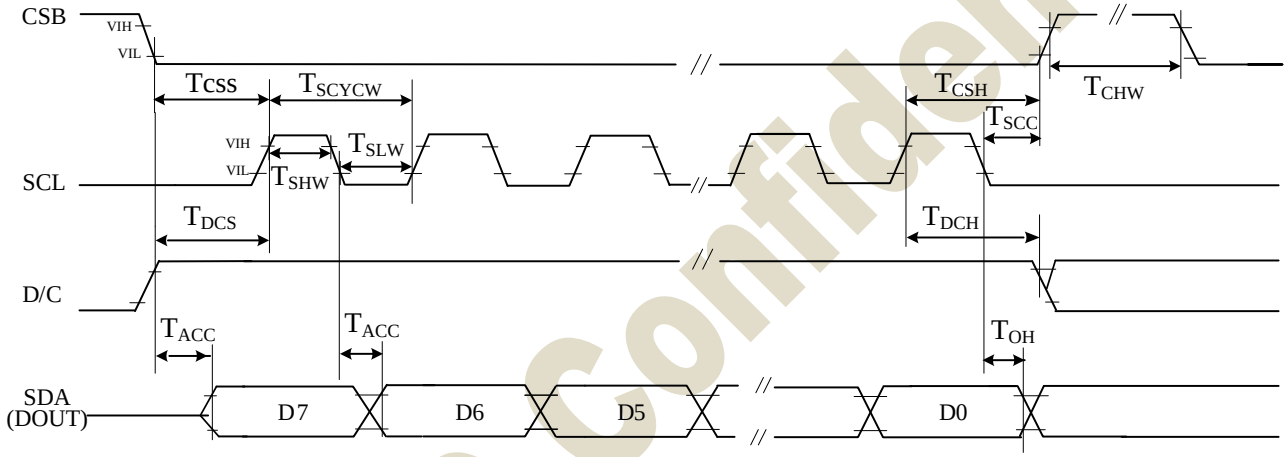
3 pin serial interface characteristics (read mode)



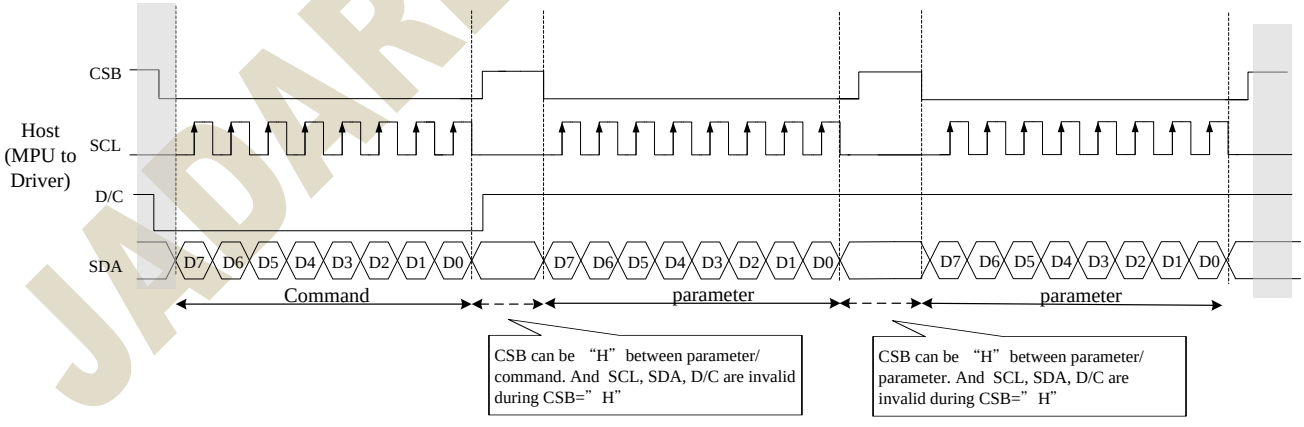
7.2 "4-Wire" Serial Port Interface



4 pin serial interface characteristics(write mode)



4 pin serial interface characteristics(read mode)



8. SPI CONTROL REGISTERS:

8.1 Register Table

Following table list all the SPI control registers and bit name definition for JD79651. Refer to the next section for detail register function description.

Address	command	Bit										
		R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
R00H	Panel setting (PSR)	W	0		0	0	0	0	0	0	0	00H
		W	1	RES[1]	RES[0]	REG_EN	BWR	UD	SHL	SHD_N	RST_N	0Fh
		W	1	-	-	-	VCMZ	TS_AUTO	VGLTIEG	NORG	VC_LUTZ	09h
R01H	Power setting (PWR)	W	0	0	0	0	0	0	0	0	1	01H
		W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03h
		W	1			-	-	-	VCOM_HV	VGHL_LV [1]	VGHL_LV [0]	00h
		W	1			VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	26h
		W	1			VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	26h
		W	1	OPTEN	VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	06h
R02H	Power OFF(POF)	W	0	0	0	0	0	0	0	1	0	02H
R03H	Power off Sequence Setting(PFS)	W	0	0	0	0	0	0	0	1	1	03H
		W	1	-	-	T_VDS_OFF [1]	T_VDS_OFF [0]	T_VSHR_OFF [1]	T_VSHR_OFF [0]	-	-	00h
R04H	Power ON (PON)	W	0	0	0	0	0	0	1	0	0	04H
R05H	Power ON Measure (PMES)	W	0	0	0	0	0	0	1	0	1	05H
R06H	Booster Soft Start (BTST)	W	0	0	0	0	0	0	1	1	0	06H
		W	1	BT_PHA[7]	BT_PHA[6]	BT_PHA[5]	BT_PHA[4]	BT_PHA[3]	BT_PHA[2]	BT_PHA[1]	BT_PHA[0]	17h
		W	1	BT_PHB[7]	BT_PHB[6]	BT_PHB[5]	BT_PHB[4]	BT_PHB[3]	BT_PHB[2]	BT_PHB[1]	BT_PHB[0]	17h
		W	1	-	-	BT_PHC[5]	BT_PHC[4]	BT_PHC[3]	BT_PHC[2]	BT_PHC[1]	BT_PHC[0]	17h
R07H	Deep Sleep(DSLP)	W	0	0	0	0	0	0	1	1	1	07H
		W	1	1	0	1	0	0	1	0	1	A5h
R10H	Data Start transmission1 (DTM1)	W	0	0	0	0	1	0	0	0	0	10H
		W	1	#	#	#	#	#	#	#	#	00H
R11H	Data Stop (DSP)	W	0	0	0	0	1	0	0	0	1	11H
		R	1	Data_flag	-	-	-	-	-	-	-	--
R12H	Display Refresh (DRF)	W	0	0	0	0	1	0	0	1	0	12H
R13H	Data Start transmission 2(DTM2)	W	0	0	0	0	1	0	0	1	1	13H
		W	1	#	#	#	#	#	#	#	#	00h
R17H	Auto sequence (AUTO)	W	0	0	0	0	1	0	1	1	1	17H
		W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h
R20H	LUT for VCOM (LUT1)	W	0	0	0	1	0	0	0	0	0	20H
		W	1	#	#	#	#	#	#	#	#	00h
R21H	White to White LUT (LUTWW)	W	0	0	0	1	0	0	0	0	1	21H
		W	1	#	#	#	#	#	#	#	#	00h
R22H	Black to White LUT (LUTBW/LUTR)	W	0	0	0	1	0	0	0	1	0	22H
		W	1	#	#	#	#	#	#	#	#	00h
R23H	White to Black LUT (LUTWB/LUTW)	W	0	0	0	1	0	0	0	1	1	23H
		W	1	#	#	#	#	#	#	#	#	00h
R24H	Black to Black LUT (LUTBB/LUTB)	W	0	0	0	1	0	0	1	0	0	24H
		W	1	#	#	#	#	#	#	#	#	00h
R26H	Set LUT States (SET_GROUP)	W	0	0	0	1	0	0	1	1	0	26H
		W	1	0	0	0	0	0	0	0	0	00h
R2AH	LUTC option	W	0	0	0	1	0	0	1	0	1	2AH
		W	1	EOPT	-	-	-	-	-	-	-	00h
		W	1	STATE_XON[7:0]								00h
		W	1	STATE_XON[15:8]								00h
R30H	PLL control (PLL)	W	0	0	0	1	1	0	0	0	0	30H

		W	1	-		M[2:0]			N[2:0]			3Ah
R40H	Temperature Sensor Command (TSC)	W	0	0	1	0	0	0	0	0	0	40H
		R	1	D10/TS[9]	D9/TS[8]	D8/TS[7]	D7/TS[6]	D6/TS[5]	D5/TS[4]	D4/TS[3]	D3/TS[2]	--
		R	1	D2/TS[1]	D1/ TS[0]	D0	-	-	-	-	-	--
R41H	Temperature Sensor Calibration (TSE)	W	0	0	1	0	0	0	0	0	1	41H
		W	1	TSE	-	-	-	TO[3]	TO[2]	TO[1]	TO0]	00h
R42H	Temperature Sensor Write (TSW)	W	0	0	1	0	0	0	0	1	0	42H
		W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
		W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
		W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h
R43H	Temperature Sensor Read (TSR)	W	0	0	1	0	0	0	0	1	1	43H
		R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	--
		R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	--
R44H	Panel Glass Check (PBC)	W	0	0	1	0	0	0	1	0	0	44H
		R	1	-	-	-	-	-	-	-	PSTA	-
R50H	VCOM and DATA interval setting (CDI)	W	0	0	1	0	1	0	0	0	0	50H
		W	1	VBD[1]	VBD[0]	DDX[1]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	D7h
R51H	Lower Power Detection (LPD)	W	0	0	1	0	1	0	0	0	1	51H
		R	1	-	-	-	-	-	-	-	LPD	--
R60H	TCON setting (TCON)	W	0	0	1	1	0	0	0	0	0	60H
		W	1	S2G[3]	S2G[2]	S2G[1]-	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	22h
R61H	Resolution setting(TRES)	W	0	0	1	1	0	0	0	0	1	61H
		W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	-	-	-	00h
		W	1	-	-	-	-	-	-	-	VRES(8)	00h
		W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h
R65H	Gate/Source Start Setting (GSST)	W	0	0	1	1	0	0	0	1	0	65H
		W	1	S_start (7)	S_start (6)	S_start (5)	S_start (4)	S_start (3)	-	-	-	00h
		W	1				gscan				G_start [8]	00h
		W	1	G_start (7)	G_start (6)	G_start (6)	G_start (4)	G_start (3)	G_start (2)	G_start (1)	G_start (0)	00h
R70H	REVISION (REV)	W	0	0	1	1	1	0	0	0	0	70H
		R	1	REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]	--
		R	1	REV[15]	REV[14]	REV[13]	REV[12]	REV[11]	REV10]	REV[09]	REV[08]	--
		R	1					CHIP_REV				--
R71H	Status register(FLG)	W	0	0	1	1	1	0	0	0	1	71H
		R	1	-	PTL_flag	I^2C_ERR	I^2C_ BUSYN	Data_flag	PON	POF	BUSY_N	-
R80H	Auto Measure Vcom (AMV)	W	0	1	0	0	0	0	0	0	0	80 H
		W	1	-	-	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	10h
R81H	Vcom Value (VV)	W	0	1	0	0	0	0	0	0	1	81H
		R	1	-	-	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--
R82H	Vcom_DC Setting register(VDCS)	W	0	1	0	0	0	0	0	1	0	82H
		W	1	-	-	VDCS[5]	VDCS[4]	VDCS[3]	VDCS[2]	VDCS[1]	VDCS[0]	00h
R90H	Partial Window (PTL)	W	0	1	0	0	1	0	0	0	0	90H
		W	1	HRST[7:3]				0	0	0	00h	00h
		W	1	HRED[7:3]				1	1	1	00h	00h
		W	1	-	-	-	-	-	-	-	VRST[8]	00h
		W	1	VRST[7:0]								00h
		W	1	-	-	-	-	-	-	-	VRED[8]	00h
		W	1	VRED[7:0]								00h
		W	1	-	-	-	-	-	-	-	PT_SCA	00h
R91H	Partial In(PTIN)	W	0	1	0	0	1	0	0	0	1	91H
R92H	Partial Out(PTOUT)	W	0	1	0	0	1	0	0	1	0	92H
RA0H	Program Mode(PGM)	W	0	1	0	1	0	0	0	0	0	A0H
RA1H	Active Program (APG)	W	0	1	0	1	0	0	0	0	1	A1H
RA2H	Read OTP Data (ROTP)	W	0	1	0	1	0	0	0	1	0	A2H
		R	1	#	#	#	#	#	#	#	#	--

RE0H	CASCADE setting (CCSET)	W	0	1	1	1	0	0	0	0	0	E0H
		W	1	-	-	-	-	-	-	TSFIX	CCEIN	00h
RE1H	Set OTP program bank (SET_OTP_BANK)	W	0	1	1	1	0	0	0	0	1	E1H
		W	1	-	-	-	-	-	-	LUT_bank0	reg_bank0	03h
RE3H	Power saving	W	0	1	1	1	0	0	0	1	1	E3H
		W	1	VCOM_W [3]	VCOM_W [2]	VCOM_W [1]	VCOM_W [0]	SD_W[3]	SD_W[2]	SD_W[2]	SD_W[0]	00h
RE4H	LVD voltage Select	W	0	1	1	1	0	0	1	0	0	E4H
		W	1	-	-	-	-	-	-	LVD_SEL [1]	LVD_SEL [0]	03h
RE5H	Force Temperature	W	0	1	1	1	0	0	1	0	1	E5H
		W	1	TS_SET[7]	TS_SET[6]	TS_SET[5]	TS_SET[4]	TS_SET[3]	TS_SET[2]	TS_SET[1]	TS_SET[0]	00h

8.2 Register Description

R/W: 0:Write Cycle 1:Read Cycle
D/CX:0:Command/1:Data
D7~D0:-:Don't Care

8.2.1R00H (PSR): Panel setting Register

R00H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PSR	W	0	0	0	0	0	0	0	0	0	00H
1st Parameter	W	1	RES[1]	RES[0]	REG_EN	BWR	UD	SHL	SHD_N	RST_N	0Fh
2nd Parameter	W	1	-	-	-	VCMZ	TS_AUTO	VGLTIEG	NORG	VC_LUTZ	09h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st parameter

Bit	Name	Description
0	RST_N	RST_N function 1: no effect. (default) 0: Booster OFF, Register data are set to their default values, and SEG/BG/VCOM:floating
1	SHD_N	SHD_N function 0 : Booster OFF, register data are kept, and SEG/BG/VCOM are kept floating. 1 : Booster on. (default)
2	SHL	SHL function 0: Shift left; First data=Sn→Sn-1 →…→S2→Last data=S1. 1: Shift right: First data=S1→S2 →…→Sn-1→Last data=Sn. (default)
3	UD	UD function 0:Scan down; First line=Gn→Gn-1 →…→G2→Last line=G1. 1:Scan up; First line=G1→G2 →…→Gn-1→Last line=Gn. (default)
4	BWR	Color selection setting 0: Pixel with B/W/Red. Run both LU1 and LU2. (default) 1: Pixel with B/W. Run LU1 only
5	REG_EN	LUT selection setting 0 : Using LUT from OTP(default) 1 : Using LUT from register
7-6	RES[1,0]	Resolution setting 00: Display resolution is 96x230 (default) 01: Display resolution is 96x252 10: Display resolution is 128x296 11: Display resolution is 160x296

Notes:
1. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turn off. SD output and VCOM will base on previous condition and keep floating.
2. When RST_N become low, driver will reset. All register will reset to default value. All of the driver's functions will disable. SD output and VCOM will base on previous condition and keep floating.

2nd parameter

	<table><tr><th>Bit</th><th>Name</th><th>Description</th></tr><tr><td>0</td><td>VC_LUTZ</td><td>VCOM status function 0 : Display off, VCOM keep to power off 1 : Display off, VCOM is set to floating (default)</td></tr><tr><td>1</td><td>NORG</td><td>VCOM status function 0 : No effect (default) 1 : Expect refreshing display, VCOM is tied to GND</td></tr><tr><td>2</td><td>VGLTIEG</td><td>VGL power off status function 0 : Power off, VGL will be floating (default) 1 : Power off, VGL will be tied to GND</td></tr><tr><td>3</td><td>TS_AUTO</td><td>Temperature sensing will be activated automatically one time 0 : Before enabling refresh, temperature sensing on 1 : Before enabling booster, temperature sensing on (default)</td></tr><tr><td>4</td><td>VCMZ</td><td>VCOM status function 0 : No effect (default) 1 : VCOM is always floating</td></tr></table> Priority of VCOM setting: VCMZ > NORG > VC_LUTZ
Restriction	

8.2.2 R01H (PWR): Power setting Register

R01H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWR	W	0	0	0	0	0	0	0	0	1	01h
1st Parameter	W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03h
2nd Parameter	W	1	VGHL_LV [2]	-	-	-	-	VCOM_HV	VGHL_LV [1]	VGHL_LV [0]	00h
3rd Parameter	W	1	-	-	VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	26h
4th Parameter	W	1	-	-	VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	26h
5th Parameter	W	1	OPTEN	VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	06h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st Parameter:

Bit	Name	Description
0	VDG_EN	Gate power selection. 0 : External VDNS power from VGH/VGL pins. (VDNG_EN open) 1 : Internal DCDC function for generate VGH/VGL. (default)
1	VDS_EN	Source power selection. 0 : External source power from VSH/VSL/VSHR pins. 1 : Internal DC/DC function for generate VSH/VSL/VSHR (default)

2nd Parameter:

Bit	Name	Description
1-0	VGHL_LV	VGHL_LV Voltage Level. 00: VGH=20 v, VGL=-20v (default) 01: VGH=19 v, VGL=-19v 10: VGH=18 v, VGL=-18v 11: VGH=17 v, VGL=-17v
2	VCOM_HV	VCOM Voltage Level 0: VCOMH=VSH-VCOMDC (default) VCOML=VSL-VCOMDC 1: VCOMH=VGH VCOML=VGL
7	VGHL_LV[2]	VGHL_LV Voltage Level. 000: VGH=20 v, VGL=-20v 001: VGH=19 v, VGL=-19v 010: VGH=18 v, VGL=-18v 011: VGH=17 v, VGL=-17v 100: VGH=16 v, VGL=-16v 101: VGH=15 v, VGL=-15v

3rd Parameter: Internal VSH power selection for B/W LUT.

Bit	Name	Description
5-0	VSH	**Internal VSH power selection.**

VSH[5:0]		Voltage(V)	VSH[5:0]		Voltage(V)	VSH[5:0]		Voltage(V)
000000	00h	6.4	010000	10h	9.6	100000	20h	12.8
000001	01h	6.6	010001	11h	9.8	100001	21h	13
000010	02h	6.8	010010	12h	10	100010	22h	13.2
000011	03h	7	010011	13h	10.2	100011	23h	13.4
000100	04h	7.2	010100	14h	10.4	100100	24h	13.6
000101	05h	7.4	010101	15h	10.6	100101	25h	13.8
000110	06h	7.6	010110	16h	10.8	100110	26h	14
000111	07h	7.8	010111	17h	11	100111	27h	14.2
001000	08h	8	011000	18h	11.2	101000	28h	14.4
001001	09h	8.2	011001	19h	11.4	101001	29h	14.6
001010	0Ah	8.4	011010	1Ah	11.6	101010	2Ah	14.8
001011	0Bh	8.6	011011	1Bh	11.8	101011	2Bh	15
001100	0Ch	8.8	011100	1Ch	12			
001101	0Dh	9	011101	1Dh	12.2			
001110	0Eh	9.2	011110	1Eh	12.4			
001111	0Fh	9.4	011111	1Fh	12.6			

4th Parameter: Internal VSL power selection for B/W LUT.

Bit	Name	Description
5-0	VSL	**Internal VSL power selection.**

VSL[5:0]		Voltage(V)	VSL[5:0]		Voltage(V)	VSL[5:0]		Voltage(V)
000000	00h	-6.4	010000	10h	-9.6	100000	20h	-12.8
000001	01h	-6.6	010001	11h	-9.8	100001	21h	-13
000010	02h	-6.8	010010	12h	-10	100010	22h	-13.2
000011	03h	-7	010011	13h	-10.2	100011	23h	-13.4
000100	04h	-7.2	010100	14h	-10.4	100100	24h	-13.6
000101	05h	-7.4	010101	15h	-10.6	100101	25h	-13.8
000110	06h	-7.6	010110	16h	-10.8	100110	26h	-14
000111	07h	-7.8	010111	17h	-11	100111	27h	-14.2
001000	08h	-8	011000	18h	-11.2	101000	28h	-14.4
001001	09h	-8.2	011001	19h	-11.4	101001	29h	-14.6
001010	0Ah	-8.4	011010	1Ah	-11.6	101010	2Ah	-14.8
001011	0Bh	-8.6	011011	1Bh	-11.8	101011	2Bh	-15
001100	0Ch	-8.8	011100	1Ch	-12			
001101	0Dh	-9	011101	1Dh	-12.2			
001110	0Eh	-9.2	011110	1Eh	-12.4			
001111	0Fh	-9.4	011111	1Fh	-12.6			

5th Parameter:

Bit	Name	Description
5-0	VSHR	**Internal VSHR power selection.**

VSH[5:0]		Voltage(V)	VSH[5:0]		Voltage(V)	VSH[5:0]		Voltage(V)
000000	00h	2.4	010110	16h	6.8	101100	2Ch	11.2
000001	01h	2.6	010111	17h	7	101101	2Dh	11.4
000010	02h	2.8	011000	18h	7.2	101110	2Eh	11.6
000011	03h	3.0	011001	19h	7.4	101111	2Fh	11.8
000100	04h	3.2	011010	1Ah	7.6	110000	30h	12
000101	05h	3.4	011011	1Bh	7.8	110001	31h	12.2
000110	06h	3.6	011100	1Ch	8	110010	32h	12.4
000111	07h	3.8	011101	1Dh	8.2	110011	33h	12.6
001000	08h	4	011110	1Eh	8.4	110100	34h	12.8
001001	09h	4.2	011111	1Fh	8.6	110101	35h	13
001010	0Ah	4.4	100000	20h	8.8	110110	36h	13.2
001011	0Bh	4.6	100001	21h	9	110111	37h	13.4
001100	0Ch	4.8	100010	22h	9.2	111000	38h	13.6
001101	0Dh	5	100011	23h	9.4	111001	39h	13.8
001110	0Eh	5.2	100100	24h	9.6	111010	3Ah	14
001111	0Fh	5.4	100101	25h	9.8	111011	3Bh	14.2
010000	10h	5.6	100110	26h	10	111100	3Ch	14.4
010001	11h	5.8	100111	27h	10.2	111101	3Dh	14.6
010010	12h	6	101000	28h	10.4	111110	3Eh	14.8
010011	13h	6.2	101001	29h	10.6	111111	3Fh	15
010100	14h	6.4	101010	2Ah	10.8			
010101	15h	6.6	101011	2Bh	11			

OPTEN=1:enable step -0.1 voltage selection(2.4~15V)

Internal VSHR power selection for Red LUT.

Bit	Name	Description
6-0	VSHR	**Internal VSHR power selection.**

VSHR[7:0]		Voltage(V)	VSHR[7:0]		Voltage(V)	VSHR[7:0]		Voltage(V)
10000000	80h	2.4	10101011	ABh	6.7	11010110	D6h	11
10000001	81h	2.5	10101100	ACh	6.8	11010111	D7h	11.1
10000010	82h	2.6	10101101	ADh	6.9	11011000	D8h	11.2
10000011	83h	2.7	10101110	AEh	7	11011001	D9h	11.3
10000100	84h	2.8	10101111	AFh	7.1	11011010	DAh	11.4
10000101	85h	2.9	10110000	B0h	7.2	11011011	DBh	11.5
10000110	86h	3	10110001	B1h	7.3	11011100	DCh	11.6
10000111	87h	3.1	10110010	B2h	7.4	11011101	DDh	11.7
10001000	88h	3.2	10110011	B3h	7.5	11011110	DEh	11.8
10001001	89h	3.3	10110100	B4h	7.6	11011111	DFh	11.9
10001010	8Ah	3.4	10110101	B5h	7.7	11100000	E0h	12
10001011	8Bh	3.5	10110110	B6h	7.8	11100001	E1h	12.1
10001100	8Ch	3.6	10110111	B7h	7.9	11100010	E2h	12.2
10001101	8Dh	3.7	10111000	B8h	8	11100011	E3h	12.3
10001110	8Eh	3.8	10111001	B9h	8.1	11100100	E4h	12.4
10001111	8Fh	3.9	10111010	BAh	8.2	11100101	E5h	12.5
10010000	90h	4	10111011	BBh	8.3	11100110	E6h	12.6
10010001	91h	4.1	10111100	BCh	8.4	11100111	E7h	12.7
10010010	92h	4.2	10111101	BDh	8.5	11101000	E8h	12.8
10010011	93h	4.3	10111110	BEh	8.6	11101001	E9h	12.9
10010100	94h	4.4	10111111	BFh	8.7	11101010	EAh	13
10010101	95h	4.5	11000000	C0h	8.8	11101011	EBh	13.1
10010110	96h	4.6	11000001	C1h	8.9	11101100	ECh	13.2
10010111	97h	4.7	11000010	C2h	9	11101101	EDh	13.3
10011000	98h	4.8	11000011	C3h	9.1	11101110	EEh	13.4
10011001	99h	4.9	11000100	C4h	9.2	11101111	EFh	13.5
10011010	9Ah	5	11000101	C5h	9.3	11110000	F0h	13.6
10011011	9Bh	5.1	11000110	C6h	9.4	11110001	F1h	13.7
10011100	9Ch	5.2	11000111	C7h	9.5	11110010	F2h	13.8
10011101	9Dh	5.3	11001000	C8h	9.6	11110011	F3h	13.9
10011110	9Eh	5.4	11001001	C9h	9.7	11110100	F4h	14
10011111	9Fh	5.5	11001010	CAh	9.8	11110101	F5h	14.1
10100000	A0h	5.6	11001011	CBh	9.9	11110110	F6h	14.2
10100001	A1h	5.7	11001100	CCh	10	11110111	F7h	14.3
10100010	A2h	5.8	11001101	CDh	10.1	11111000	F8h	14.4
10100011	A3h	5.9	11001110	CEh	10.2	11111001	F9h	14.5
10100100	A4h	6	11001111	CFh	10.3	11111010	FAh	14.6
10100101	A5h	6.1	11010000	D0h	10.4	11111011	FBh	14.7
10100110	A6h	6.2	11010001	D1h	10.5	11111100	FCh	14.8
10100111	A7h	6.3	11010010	D2h	10.6	11111101	FDh	14.9
10101000	A8h	6.4	11010011	D3h	10.7	11111110	FEh	15
10101001	A9h	6.5	11010100	D4h	10.8			
10101010	AAh	6.6	11010101	D5h	10.9			

Note: VSH>VSHR

Restriction	

8.2.3 R02H (POF): Power OFF Command

R02H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
POF	W	0	0	0	0	0	0	0	1	0	02H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power off command, driver will power off base on power off sequence. ● After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high. ● Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. ● SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.
Restriction	This command only active when BUSY_N = "1".

8.2.4 R03H (PFS): Power off Sequence Setting Register

R03H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PFS	W	0	0	0	0	0	0	0	1	1	03H
1st Parameter	W	1	-	-	T_VDS_OFF [1]	T_VDS_OFF [0]	-	-	-	-	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : 1st Parameter:

Bit	Name	Description
5-4	T_VDS_OFF	00: 1 frame (default) 01: 2 frame 10: 3 frame 11: 4 frame

Restriction	

8.2.5 R04H (PON): Power ON Command

R04H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PON	W	0	0	0	0	0	0	1	0	0	04H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power on command, driver will power on base on power on sequence. ● After power on command, BUSY_N signal will drop from high to low. When finishing the power on sequence, BUSY_N signal will rise from low to high.
Restriction	This command only active when BUSY_N = "1".

8.2.6 R05H (PMES): Power ON Measure Command

R05H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PMES	W	0	0	0	0	0	0	1	0	1	05H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■ If user wants to read temperature sensor or detect low power in power off mode, user has to send this command. After power on measure command, driver will switch on relevant commend with Low Power detection (R51H) and temperature measurement. (R40H).
Restriction	This command only active when BUSY_N = "1".

8.2.7 R06H (BTST): Booster Soft Start Command

R06H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BTST	W	0	0	0	0	0	0	1	1	0	06H
1st Parameter	W	1	BT_PHA[7]	BT_PHA[6]	BT_PHA[5]	BT_PHA[4]	BT_PHA[3]	BT_PHA[2]	BT_PHA[1]	BT_PHA[0]	17h
2nd Parameter	W	1	BT_PHB[7]	BT_PHB[6]	BT_PHB[5]	BT_PHB[4]	BT_PHB[3]	BT_PHB[2]	BT_PHB[1]	BT_PHB[0]	17h
3rd Parameter	W	1	-	-	BT_PHC[5]	BT_PHC[4]	BT_PHC[3]	BT_PHC[2]	BT_PHC[1]	BT_PHC[0]	17h

Description

-The command define as follows:

1st Parameter:

Bit	Name	Description
2-0	Driving strength of phase A	000: period 1 001: period 2 010: period 3 011: period 4 100: period 5 101: period 6 110: period 7 111: period 8 (default)
5-3		000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8
7-6	Soft start period of phase A	00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

2nd Parameter:

Bit	Name	Description
2-0	Driving strength of phase B	000: period 1 001: period 2 010: period 3 011: period 4 100: period 5 101: period 6 110: period 7 111: period 8 (default)
5-3		000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8
7-6	Soft start period of phase B	00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

<table>
<tr><td>Description</td><td>3rd Parameter:
<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>2-0</td><td>Minimum OFF time setting of GDR in phase C</td><td>000: period 1
001: period 2
010: period 3
011: period 4
100: period 5
101: period 6
110: period 7
111: period 8 (default)</td></tr>
<tr><td>5-3</td><td>Driving strength of phase C</td><td>000: Strength 1
001: Strength 2
010: Strength 3 (default)
011: Strength 4
100: Strength 5
101: Strength 6
110: Strength 7
111: Strength 8</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td></td></tr>
</table>

8.2.8 R07H (DSLP): Deep Sleep Command

R07H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSLP	W	0	0	0	0	0	0	1	1	1	07H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset. The only one parameter is a check code, the command would be excited if check code = 0xA5.
Restriction	This command only active when BUSY_N = "1".

8.2.9 R10H (DTM1): Data Start transmission 1 Register

R10H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM1	W	0	0	0	0	1	0	0	0	0	10H
1st Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
2nd Parameter	W	1									00h
…	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "OLD" data to SRAM. In B/W/Red mode, this command writes "B/W" data to SRAM. In Program mode, this command writes "OTP" data to SRAM for programming.
Restriction	

8.2.10 R11H (DSP): Data Stop Command

R11H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSP	W	0	0	0	0	1	0	0	0	1	11H
1st Parameter	R	1	Data_flag	-	-	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■While finished the data transmitting, user must send this command to driver and read Data_flag information. 1st Parameter: Bit / Name / Description 7 / Data_flag / 0: Driver didn't receive all the data. 1: Driver has already received all of the one frame data. After "Data Start" (10h) or "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts.
Restriction	This command only actives when BUSY_N = "1".

8.2.11 R12H (DRF): Display Refresh Command

R12H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DRF	W	0	0	0	0	1	0	0	1	0	12H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■While users send this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. After display refresh command, BUSY_N signal will become "0".
Restriction	This command only actives when BUSY_N = "1"

8.2.12 R13H (DTM2): Data Start transmission 2 Register

R13H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM2	W	0	0	0	0	1	0	0	1	1	13H
1st Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
2nd Parameter	W	1									00h
…	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "NEW" data to SRAM. In B/W/Red mode, this command writes "RED" data to SRAM.
Restriction	

8.2.13 R17H (AUTO): Auto Sequence

R17H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Auto Sequence	W	0	0	0	0	1	0	1	1	1	17H
1st Parameter	W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h

Description	The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP. AUTO (0x17) + Code(0xA5) = (PON→DRF→POF) AUTO (0x17) + Code(0xA7) = (PON→DRF→POF→DSLP)
Restriction	This command only actives when BUSY_N = "1".

8.2.14 R20H (LUTC): LUT for Vcom

R20H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTC	W	0	0	0	1	0	0	0	0	0	20H
1st Parameter	W	1	Group repeat times[7:0]								00h
2nd Parameter	W	1	level selection1-1 [1:0]		Frame Number1-1 [5:0]						00h
3rd Parameter	W	1	level selection1-2 [1:0]		Frame Number1-2 [5:0]						00h
4th Parameter	W	1	level selection2-1 [1:0]		Frame Number2-1 [5:0]						00h
5th Parameter	W	1	level selection2-2 [1:0]		Frame Number2-2 [5:0]						00h
6th Parameter	W	1	State 1 repeat times[7:0]								00h
7th Parameter	W	1	State 2 repeat times[7:0]								00h
8th~14th Parameter	W	1	2nd group								00h
15th~21th Parameter	W	1	3rd group								00h
…	W	1	4th~7th group								00h
50th~56th Parameter	W	1	8th group								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-This command builds up VCOM Look-Up Table (LUT). This LUT includes 8 kinds of groups; each group is of 7 bytes, as above. Each Group is divided to 2 states and "Group Repeat Number". Each state made up 2 phases. And each phase is combined with "Repeat Number", "Level selection", and "Frame Number". Byte 2: Group repeat times. Byte 3-6: [D7:D6]: Level selection of each phase. [D5:D0]: Frame number of each phase (state1 & state 2) Bytes 7~8: state repeat times (state1 & state 2) Bytes 2,9,16,23,30,…: Group repeat times 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 times Bytes 3~6,10~13,17~20, 24~27, 31~ 34 Level Selection. [D7:D6]: Level Selection. 00b:-VCM_DC 01b:VSH-VCM_DC(VCOMH) 10b:VSL -VCM_DC(VCOML) 11b:Floating [D5:D0]: Number of frames (state1 & state 2) 00 0000b~11 1111b: 0~63 times Bytes 7~8,14~15,21~22,28~29,35~36,…: :repeat times (state1 & state 2) 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 frames If BWR=0(BWR mode),all 8 groups are used. If BWR=1(BW mode),only 6 groups are used.
Restriction	

8.2.15 R21H (LUTWW): W2W LUT

R21H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTWW	W	0	0	0	1	0	0	0	0	1	21H
1st Parameter	W	1	Group repeat times[7:0]								00h
2nd Parameter	W	1	level selection1-1 [1:0]		Frame Number1-1 [5:0]						00h
3rd Parameter	W	1	level selection1-2 [1:0]		Frame Number1-2 [5:0]						00h
4th Parameter	W	1	level selection2-1 [1:0]		Frame Number2-1 [5:0]						00h
5th Parameter	W	1	level selection2-2 [1:0]		Frame Number2-2 [5:0]						00h
6th Parameter	W	1	State 1 repeat times[7:0]								00h
7th Parameter	W	1	State 2 repeat times[7:0]								00h
8th~14th Parameter	W	1	2nd group								00h
15th~21th Parameter	W	1	3rd group								00h
…	W	1	4th~5th group								00h
36th~42th Parameter	W	1	6th group								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-This command builds LUTWW for White-to- White. This LUT includes 6 kinds of groups; each group is of 7 bytes, as above. Each group is divided to 2 states and "Group Repeat Number". Each state made up 2 phases. And each phase is combined with "Repeat Number", "Level selection", and "Frame Number". Byte 2:Group repeat times. Byte 3-6: [D7:D6]: Level selection of each phase. [D5:D0]: Frame number of each phase (state1 & state 2) Bytes 7~8: state repeat times (state1 & state 2) Bytes 2,9,16,23,30,…: Group repeat times 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 times Bytes 3~6,10~13,17~20, 24~27, 31~ 34 Level Selection. [D7:D6]: Level Selection. 00b: GND 01b: VSH 10b: VSL 11b: VSHR [D5:D0]: Number of frames (state1 & state 2) 00 0000b~11 1111b: 0~63 times Bytes 7~8,14~15,21~22,28~29,35~36,…: :repeat times (state1 & state 2) 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 frames If BWR=0(BWR mode), LUTWW is not used. If BWR=1(BW mode), LUTWW is used.
Restriction	

8.2.16 R22H (LUTBW/LUTR): Black to White LUT or Red LUT Register

R22H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTBW/LUTR	W	0	0	0	1	0	0	0	1	0	22H
1st Parameter	W	1	Group repeat times[7:0]								00h
2nd Parameter	W	1	level selection1-1 [1:0]		Frame Number1-1 [5:0]						00h
3rd Parameter	W	1	level selection1-2 [1:0]		Frame Number1-2 [5:0]						00h
4th Parameter	W	1	level selection2-1 [1:0]		Frame Number2-1 [5:0]						00h
5th Parameter	W	1	level selection2-2 [1:0]		Frame Number2-2 [5:0]						00h
6th Parameter	W	1	State 1 repeat times[7:0]								00h
7th Parameter	W	1	State 2 repeat times[7:0]								00h
8th~14th Parameter	W	1	2nd group								00h
15tn~21tn Parameter	W	1	3rd group								00h
…	W	1	4th~7th group								00h
50th~56th Parameter	W	1	8th group								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	This command builds Look-up Table for LUTBW / LUTR. This LUT includes 8 kinds of groups; each group is of 7 bytes, as above. Each Group is divided to 2 states and "Group Repeat Number". Each state made up 2 phases. And each phase is combined with "Repeat Number", "Level selection", and "Frame Number". Byte 2:Group repeat times. Byte 3-6: [D7:D6]: Level selection of each phase. [D5:D0]: Frame number of each phase (state1 & state 2) Bytes 7~8: state repeat times (state1 & state 2) Bytes 2,9,16,23,30,…: Group repeat times 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 times Bytes 3~6,10~13,17~20, 24~27, 31~ 34 Level Selection. [D7:D6]: Level Selection. 00b: GND 01b: VSH 10b: VSL 11b: VSHR [D5:D0]: Number of frames (state1 & state 2) 00 0000b~11 1111b: 0~63 times Bytes 7~8,14~15,21~22,28~29,35~36,…: :repeat times (state1 & state 2) 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 frames If BWR=0(BWR mode),all 8 groups are used. If BWR=1(BW mode),only 6 groups are used.
Restriction	

8.2.17 R23H (LUTWB/LUTW): White to Black LUT or White LUT Register

R23H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTWB/LUTW	W	0	0	0	1	0	0	0	1	1	23H
1st Parameter	W	1	Group repeat times[7:0]								00h
2nd Parameter	W	1	level selection1-1 [1:0]		Frame Number1-1 [5:0]						00h
3rd Parameter	W	1	level selection1-2 [1:0]		Frame Number1-2 [5:0]						00h
4th Parameter	W	1	level selection2-1 [1:0]		Frame Number2-1 [5:0]						00h
5th Parameter	W	1	level selection2-2 [1:0]		Frame Number2-2 [5:0]						00h
6th Parameter	W	1	State 1 repeat times[7:0]								00h
7th Parameter	W	1	State 2 repeat times[7:0]								00h
8th~14th Parameter	W	1	2nd group								00h
15th~21th Parameter	W	1	3rd group								00h
…	W	1	4th~7th group								00h
50th~56th Parameter	W	1	8th group								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- This command builds Look-up Table for LUTWB/LUTW. This LUT includes 8 kinds of groups; each group is of 7 bytes, as above. Each Group is divided to 2 states and "Group Repeat Number". Each state made up 2 phases. And each phase is combined with "Repeat Number", "Level selection", and "Frame Number". Byte 2:Group repeat times. Byte 3-6: [D7:D6]: Level selection of each phase. [D5:D0]: Frame number of each phase (state1 & state 2) Bytes 7~8: state repeat times (state1 & state 2) Bytes 2,9,16,23,30,…: Group repeat times 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 times Bytes 3~6,10~13,17~20, 24~27, 31~ 34 Level Selection. [D7:D6]: Level Selection. 00b: GND 01b: VSH 10b: VSL 11b: VSHR [D5:D0]: Number of frames (state1 & state 2) 00 0000b~11 1111b: 0~63 times Bytes 7~8,14~15,21~22,28~29,35~36,…: :repeat times (state1 & state 2) 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 frames If BWR=0(BWR mode),all 8 groups are used. If BWR=1(BW mode),only 6 groups are used.
Restriction	-

8.2.18 R24H (LUTBB/LUTB): Black to Black LUT or Black LUT Register

R24H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTBB/LUTB	W	0	0	0	1	0	0	1	0	0	24H
1st Parameter	W	1	Group repeat times[7:0]								00h
2nd Parameter	W	1	level selection1-1 [1:0]		Frame Number1-1 [5:0]						00h
3rd Parameter	W	1	level selection1-2 [1:0]		Frame Number1-2 [5:0]						00h
4th Parameter	W	1	level selection2-1 [1:0]		Frame Number2-1 [5:0]						00h
5th Parameter	W	1	level selection2-2 [1:0]		Frame Number2-2 [5:0]						00h
6th Parameter	W	1	State 1 repeat times[7:0]								00h
7th Parameter	W	1	State 2 repeat times[7:0]								00h
8th~14th Parameter	W	1	2nd group								00h
15th~21th Parameter	W	1	3rd group								00h
…	W	1	4th~7th group								00h
50th~56th Parameter	W	1	8th group								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- This command builds Look-up Table for LUTBB/LUTB. This LUT includes 8 kinds of groups; each group is of 7 bytes, as above. Each Group is divided to 2 states and "Group Repeat Number". Each state made up 2 phases. And each phase is combined with "Repeat Number", "Level selection", and "Frame Number". Byte 2: Group repeat times. Byte 3-6: [D7:D6]: Level selection of each phase. [D5:D0]: Frame number of each phase (state1 & state 2) Bytes 7~8: state repeat times (state1 & state 2) Bytes 2,9,16,23,30,…: Group repeat times 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 times Bytes 3~6,10~13,17~20, 24~27, 31~ 34 Level Selection. [D7:D6]: Level Selection. 00b: GND 01b: VSH 10b: VSL 11b: VSHR [D5:D0]: Number of frames (state1 & state 2) 00 0000b~11 1111b: 0~63 times Bytes 7~8,14~15,21~22,28~29,35~36,…: :repeat times (state1 & state 2) 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 frames If BWR=0(BWR mode),all 8 groups are used. If BWR=1(BW mode),only 6 groups are used.
Restriction	

Note: All LUTs are independent of each other and could be deal with separately. If waveform time is different for each LUT, IC would select longest LUT as refresh time and fill 0 (GND) to remaining refresh time for other LUT.

8.2.19 R26H (SET_GROUP): Set LUT States

R26H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
SET_ GROUP	W	0	0	0	1	0	0	1	1	0	26H
1st Parameter	W	1	-	-	-	-	-	-	group_sel[1:0]		00h

Description	This command is used to set LUT states Function of group_sel [1:0] are shown below B/W/Red mode(BWR=0)

Value	Group
00	8
01	7
10	6
11	5

B/W mode (BWR=1)

Value	Group
00	6
01	5
10	4
11	3

Restriction	

8.2.20 R2AH (LUTOPT): LUT Option Register

R2AH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUT Option	W	0	0	0	1	0	1	0	1	0	2AH
1st Parameter	W	1	EOPT	-	-	-	-	-	-	-	00h
2nd Parameter	W	1	STATE_XON[7:0]								00h
3rd Parameter	W	1	STATE_XON[15:8]								00h

Description

- This command sets XON and ending options of source output STATE_XON[15:0]:

  All Gate ON (Each bit controls one sub-state, STATE_XON [0] for state-1, STATE_XON [1] for state-2 …..)
  0000 0000 0000 0000b: no All-Gate-ON
  0000 0000 0000 0001b: State1 All-Gate-ON
  0000 0000 0000 0011b: State1 and State2 All-Gate-ON
  …

EOPT:
Option for LUT ending

1st Parameter:

Bit	Name	Description
7	EOPT	0: Normal.(Default) 1: Source output level keep previous output before power off

Restriction

8.2.21 R30H (PLL): PLL Control Register

R30H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PLL	W	0	0	0	1	1	0	0	0	0	30H
1st Parameter	W	1	-	-	M[2:0]			N[2:0]			3Ch

NOTE: "-" Don't care, can be set to VDD or GND level

Description

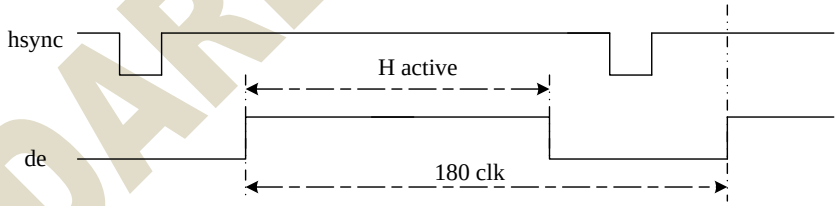
-The command defines as:

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

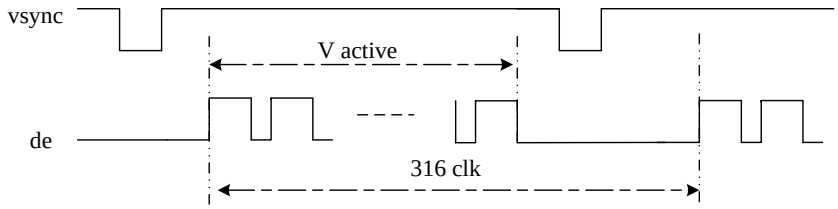
M	N	Frame rate	M	N	Frame rate	M	N	Frame rate	M	N	Frame rate
1	1	29HZ	3	1	86HZ	5	1	150HZ	7	1	200HZ
	2	14HZ		2	43HZ		2	72HZ		2	100HZ
	3	10HZ		3	29HZ		3	48HZ		3	67HZ
	4	7HZ		4	21HZ		4	36HZ		4	50HZ
	5	6HZ		5	17HZ		5	29HZ		5	40HZ
	6	5HZ		6	14HZ		6	24HZ		6	33HZ
	7	4HZ		7	12HZ		7	20HZ		7	29HZ
2	1	57HZ	4	1	114HZ	6	1	171HZ			
	2	29HZ		2	57HZ		2	86HZ			
	3	19HZ		3	38HZ		3	57HZ			
	4	14HZ		4	29HZ		4	43HZ			
	5	11HZ		5	23HZ		5	34HZ			
	6	10HZ		6	19HZ		6	29HZ			
	7	8HZ		7	16HZ		7	24HZ			

remark

-Horizental



-Vertical



Restriction

8.2.22 R40H (TSC): Temperature Sensor Command

R40H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	0	40H
1st Parameter	R	1	D10/TS[9]	D9/TS[8]	D8/TS[7]	D7/TS[6]	D6/TS[5]	D5/TS[4]	D4/TS[3]	D3/TS[2]	-
2nd Parameter	R	1	D2/TS[1]	D1/ TS[0]	D0	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

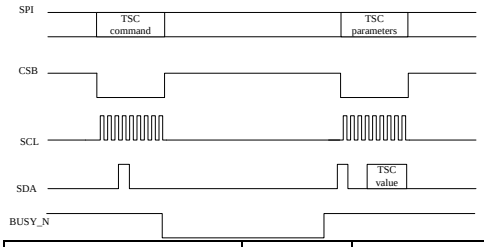
Description

-The command define as follows:

This command indicates the temperature value.

If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value.

If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value



TS[9:2]/D[10:3]	T (°C)	TS[9:2]/D[10:3]	T (°C)	TS[9:2]/D[10:3]	T (°C)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27
11101010	-22	00000011	3	00011100	28
11101011	-21	00000100	4	00011101	29
11101100	-20	00000101	5	00011110	30
11101101	-19	00000110	6	00011111	31
11101110	-18	00000111	7	00100000	32
11101111	-17	00001000	8	00100001	33
11110000	-16	00001001	9	00100010	34
11110001	-15	00001010	10	00100011	35
11110010	-14	00001011	11	00100100	36
11110011	-13	00001100	12	00100101	37
11110100	-12	00001101	13	00100110	38
11110101	-11	00001110	14	00100111	39
11110110	-10	00001111	15	00101000	40
11110111	-9	00010000	16	00101001	41
11111000	-8	00010001	17	00101010	42
11111001	-7	00010010	18	00101011	43
11111010	-6	00010011	19	00101100	44
11111011	-5	00010100	20	00101101	45
11111100	-4	00010101	21	00101110	46
11111101	-3	00010110	22	00101111	47
11111110	-2	00010111	23	00110000	48
11111111	-1	00011000	24	00110001	49

TS[1:0]	T (°C)
00	+0
01	+0.25
10	+0.5
11	+0.75

Restriction: This command only actives when BUSY_N = "1".

8.2.23 R41H (TSE): Temperature Sensor Calibration Register

R41H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSE	W	0	0	1	0	0	0	0	0	1	41H
1st Parameter	W	1	TSE	-	TO[5]	TO[4]	TO[3]	TO[2]	TO[1]	TO[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the driver IC temperature sensor enable and calibration function.

Reserve one temperature offset TO[3:0] for calibration
1. TO[3]: mean '+' or '-' , while 0 is '+' ; 1 is '-'
2. TO[2:0]: mean temperature offset value

Bit	Name	Description
3-0	TO[3:0]	Temperature level: 0000: +0℃ (default) 0001: +1℃ 0010: +2℃ 0011: +3℃ 0100: +4℃ 0101: +5℃ 0110: +6℃ 0111: +7℃ 1000: -8℃ 1001: -7℃ 1010: -6℃ 1011: -5℃ 1100: -4℃ 1101: -3℃ 1110: -2℃ 1111: -1℃
5-4	TO[5:4]	00: +0.0℃ (default) 01: +0.25℃ 10: +0.5℃ 11: +0.75℃
7	TSE	Internal temperature sensor enable 0: Internal temperature sensor enable.(default) 1: Internal temperature sensor disable, using external temperature sensor.

Restriction: This command only actives after R04H(PON) or R05H(PMES)

8.2.24 R42H (TSW): Temperature Sensor Write Register

R42H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSW	W	0	0	1	0	0	0	0	1	0	42H
1st Parameter	W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
2nd Parameter	W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
3rd Parameter	W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

This command writes the temperature.

1st Parameter:

Bit	Name	Description
2-0	WATTR[2:0]	Pointer setting
5-3	WATTR[5:3]	User-defined address bits (A2, A1, A0)
7-6	WATTR[7:6]	I2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1st parameter) 11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

2nd Parameter:

Bit	Name	Description
7-0	WMSB[7:0]	MSByte of write-data to external temperature sensor

3nd Parameter:

Bit	Name	Description
7-0	WLSB[7:0]	LSByte of write-data to external temperature sensor

Restriction

This command only actives after R04H(PON) or R05H(PMES)

8.2.25 R43H (TSR): Temperature Sensor Read Register

R43H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	1	1	43H
1st Parameter	R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	-
2nd Parameter	R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

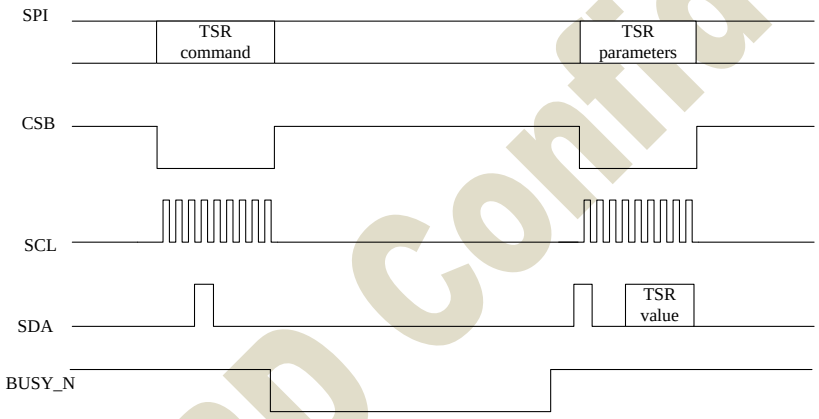
This command reads the temperature sensed by the temperature sensor.

1st Parameter:

Bit	Name	Description
7-0	RMSB[7:0]	MSByte of read-data from external temperature sensor

2nd Parameter:

Bit	Name	Description
7-0	RLSB[7:0]	LSByte of write-data from external temperature sensor



Restriction

This command only actives after R04H(PON) or R05H(PMES)

8.2.26 R44H (PBC): Panel Glass Check Register

R44H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PBC	W	0	0	1	0	0	0	1	0	0	44H
1st Parameter	R	1	-	-	-	-	-	-	-	PSTA	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- This command is used to enable panel check, and to disable after reading result. Bit / Name / Description 0 / PSTA / 0 : Panel check fail (panel broken) 1 : Panel check pass
Restriction	This command only actives when BUSY_N = "1".

8.2.27 R50H (CDI): VCOM and DATA interval setting Register

R50H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CDI	W	0	0	1	0	1	0	0	0	0	50H
1st Parameter	W	1	VBD[1]	VBD[0]	DDX[1]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	D7h

NOTE: "-" Don't care, can be set to VDD or GND level

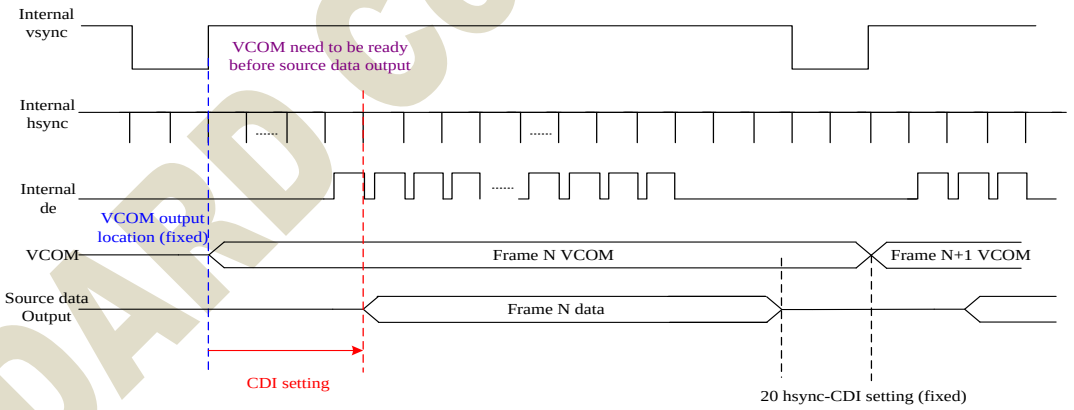
Description

-The command defines as:

1st Parameter:

CDI[1:0]: This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be keep (20hsync).

Bit	Name	Description
3-0	CDI[3:0]	Vcom and data interval 0000: 17 hsync 0001:16 hsync 0010:15 hsync 0011:14 hsync 0100:13 hsync 0101:12 hsync 0110:11 hsync 0111:10 hsync 1000:9 hsync 1001:8 hsync 1010:7 hsync 1011:6 hsync 1100:5 hsync 1101:4 hsync 1110:3 hsync 1111:2 hsync



VBD[1:0]: Border data selection.

B/W/Red mode(BWR=0)

Bit 4	Bit7-6	Description
DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTB
1 (default)	00	LUTB
	01	LUTW
	10	LUTR
	11 (default)	Floating

B/W mode (BWR=1)

Bit 4	Bit7-6	Description
DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTBW (1->0)
	10	LUTWB (0->1)
	11	Floating
1 (default)	00	Floating
	01	LUTWB (0->1)
	10	LUTBW (1->0)
	11	Floating

Border output voltage level: The level selection is based on mapping LUT data.
Level Selection:
00b: VCOM
01b: VSH
10b: VSL
11b: VSHR

DDX[1:0]: Data polarity
1. DDX[1] for RED data, DDX[0] for BW data in the B/W/Red mode
2. DDX[0] for B/W mode

B/W/Red mode(BWR=0)
DDX[1] is for RED data
DDX[0] is for B/W data

Bit 5-4	Description	
DDX[1:0]	Data (DTM2, DTM1)	LUT
00	00	LUTW
	01	LUTB
	10	LUTR
	11	LUTR
01 (default)	00	LUTB
	01	LUTW
	10	LUTR
	11	LUTR
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTB
11	00	LUTR
	01	LUTR
	10	LUTB
	11	LUTW

B/W mode (BWR=1)
DDX[1]=0 is for BW mode with NEW/OLD

Bit 5-4	Description	
DDX[1:0]	Data (DTM2, DTM1)	LUT
00	00	LUTWW (0->0)
	01	LUTBW(1->0)
	10	LUTWB(0->1)
	11	LUTBB(1->1)
01 (default)	00	LUTBB(0->0)
	01	LUTWB(1->0)
	10	LUTBW(0->1)
	11	LUTWW(1->1)

<table>
<tr><td></td><td>DDX[1]=1 is for BW mode without NEW/OLD
<table>
<tr><td>Bit 5-4</td><td colspan="2">Description</td></tr>
<tr><td>DDX[1:0]</td><td>Data (DTM2)</td><td>LUT</td></tr>
<tr><td rowspan="2">10</td><td>0</td><td>LUTBW(1->0)</td></tr>
<tr><td>1</td><td>LUTWB(0->1)</td></tr>
<tr><td rowspan="2">11</td><td>0</td><td>LUTWB(0->1)</td></tr>
<tr><td>1</td><td>LUTBW(1->0)</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td></td></tr>
</table>

8.2.28 R51H (LPD): Lower Power Detection Register

R51H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LPD	W	0	0	1	0	1	0	0	0	1	51H
1st Parameter	R	1	-	-	-	-	-	-	-	LPD	--

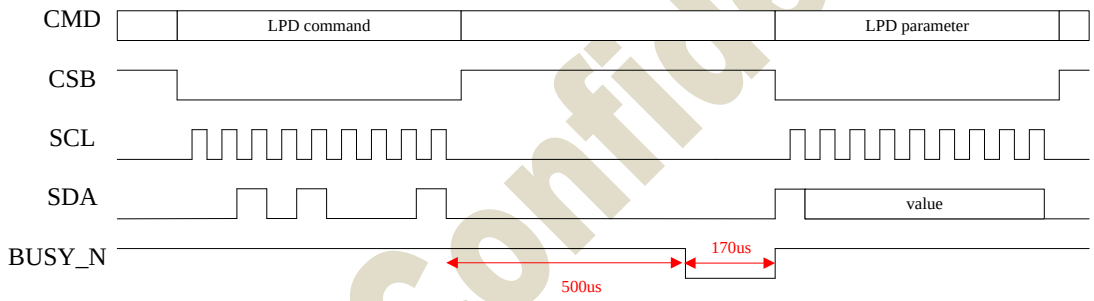
NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the input power condition. Host can read this data to understand the battery's condition.
When LPD="1", system input power is normal.
When LPD="0", system input power is lower (VDD<2.5v, which could be select in RE4H (LVSEL)).

1st Parameter:

Bit 0	LPD
0	Low power input.
1	Normal status.



Restriction

This command only actives when BUSY_N = "1".

8.2.29 R60H (TCON): TCON setting

R60H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TCON	W	0	0	1	1	0	0	0	0	0	60H
1st Parameter	W	1	S2G[3]	S2G[2]	S2G[1]-	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	22h

NOTE: "-" Don't care, can be set to VDD or GND level

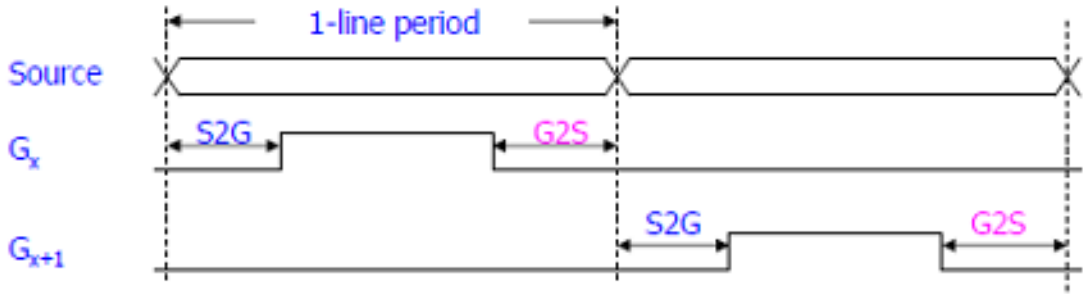
Description

- The command define Non-overlap period of gate and source as below:

1st Parameter:

Bit	Name	Description
7-0	S2G[3:0] G2S[3:0]	0000: 4 clock 0001: 8 clock 0010: 12 clock (default) 0011:16 clock 0100: 20 clock 0101: 24 clock 0110: 28 clock 0111: 32 clock 1000: 36 clock 1001: 40 clock 1010: 44 clock 1011: 48 clock 1100: 52 clock 1101: 56 clock 1110: 60 clock 1111: 64 clock

Period=660ns



Restriction

8.2.30 R61H (TRES): Resolution setting

R61H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TRES	W	0	0	1	1	0	0	0	0	1	61H
1st Parameter	W	1	HRES[7]	HRES[6]	HRES[5]	HRES[4]	HRES[3]	-	-	-	00h
2nd Parameter	W	1								VRES[8]	00h
3th Parameter	W	1	VRES[7]	VRES[6]	VRES[5]	VRES[4]	VRES[3]	VRES[2]	VRES[1]	VRES[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: When using register: Horizontal display resolution(source) = HRES Vertical display resolution(gate) = VRES Channel disable calculation: GD : First G active = G0; LAST active GD= first active +VRES[8:0] -1 SD : First active channel: =S0 ; LAST active SD= first active +HRES[7:3]*8-1 EX :128X272 GD: First G active = G0 LAST active GD= 0+272-1= 271; (G271) SD : First active channel: =S0 LAST active SD=0+16*8-1=127; (S127) Note : Only supports source 176.ch for source 160ch. above
Restriction	

8.2.31 R65H (GSST): Gate/Source Start Setting Register

R65H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
GSST	W	0	0	1	1	0	0	1	0	1	65H
1st Parameter	W	1	S_start[7]	S_start[6]	S_start[5]	S_start[4]	S_start[3]	--	--	--	00h
2nd Parameter	W	1				gscan				G_start[8]	00h
3rd Parameter	W	1	G_start[7]	G_start[6]	G_start[6]	G_start[4]	G_start[3]	G_start[2]	G_start[1]	G_start[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: 1.S_Start [8:0] describe which source output line is the first date line 2.G_Start[8:0] describe which gate line is the first scan line 3. gscan :Gate scan select 0: Normal scan 1: Cascade type 2 scan
Restriction	S_Start should be the multiple of 8

8.2.32 R70H (REV): REVISION register

R70H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
REV	W	0	0	1	1	1	0	0	0	0	70H
1st Parameter	R	1	REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]	FFh
2nd Parameter	R	1	REV[15]	REV[14]	REV[13]	REV[12]	REV[11]	REV[10]	REV[9]	REV[8]	FFh
3rd Parameter	R	1	Vendor ID				CHIP_REV				--

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: The LUT_REV is read from: OTP Bank0 address = 0xAED & 0xAEE OTP Bank1 address = 0x16ED & 0x16EE 3rd Parameter:
Restriction	

Bit	Description
3-0	CHIP_REV
7-4	Vendor ID: 'F'

8.2.33 R71H (FLG): Status register

R71H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
FLG	W	0	0	1	1	1	0	0	0	1	71H
1st Parameter	R	1	-	PTL_flag	I2C_ERR	I2C_ BUSYN	Data_flag	PON	POF	BUSY_N	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the IC status. Host can read this data to understand the IC status.

1st Parameter:

Bit	Name	Description
6	PTL_flag	Partial display status (high: partial mode)
5	2C_ERR	I2C master error status
4	I2C_BUSYN	I2C master busy status (low active)
3	Data_flag	Driver has already received one frame data
2	PON	PON 0: Not in PON mode 1: In PON mode
1	POF	POF 0: Not in POF mode(default) 1: In POF mode
0	BUSY_N	Driver busy status(low active)

Restriction: User can send this command in any time. It doesn't have restriction of BUSY_N.

8.2.34 R80H (AMV): Auto Measure VCOM register

R80H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AMV	W	0	1	0	0	0	0	0	0	0	80H
1st Parameter	W	1	-	-	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	10h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the IC status. Host can read this data to understand the IC status.

1st Parameter:

Bit	Name	Description
0	AMVE	AMVE: Auto Measure Vcom Setting 0: Auto measure VCOM disable (default) 1: Auto measure VCOM enable
1	AMV	AMV: Analog signal 0:Get Vcom value from R81h(default) 1:Get Vcom value in analog signal
2	AMVS	AMVS: setting for Source output of AMV 0: Source output 0V during Auto Measure VCOM period. (default) 1: Source output VSHR during Auto Measure VCOM period.
3	XON	XON: setting for all Gate ON of AMV 0: Gate normally scan during Auto Measure VCOM period. (default) 1: All Gate ON during Auto Measure VCOM period.
5-4	AMVT[1:0]	The sensing time of VCOM detection 00: 3s 01: 5s (default) 10: 8s 11: 10s

After VCOM sensing, use cmd. R81H to return VCOM value

Restriction: This command only actives when BUSY_N = "1".

8.2.35 R81H (VV): VCOM Value register

R81H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VV	W	0	1	0	0	0	0	0	0	1	81H
1st Parameter	R	1	-	-	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command could get the VCOM value

1st Parameter:

Bit	Name	Description
5-0	VV[5:0]	**VCOM value**

VCOM[5:0]		Voltage(V)	VCOM[5:0]		Voltage(V)	VCOM[5:0]		Voltage(V)
000000	00h	-0.1	010100	14h	-1.1	101000	28h	-2.1
000001	01h	-0.15	010101	15h	-1.15	101001	29h	-2.15
000010	02h	-0.2	010110	16h	-1.2	101010	2Ah	-2.2
000011	03h	-0.25	010111	17h	-1.25	101011	2Bh	-2.25
000100	04h	-0.3	011000	18h	-1.3	101100	2Ch	-2.3
000101	05h	-0.35	011001	19h	-1.35	101101	2Dh	-2.35
000110	06h	-0.4	011010	1Ah	-1.4	101110	2Eh	-2.4
000111	07h	-0.45	011011	1Bh	-1.45	101111	2Fh	-2.45
001000	08h	-0.5	011100	1Ch	-1.5	110000	30h	-2.5
001001	09h	-0.55	011101	1Dh	-1.55	110001	31h	-2.55
001010	0Ah	-0.6	011110	1Eh	-1.6	110010	32h	-2.6
001011	0Bh	-0.65	011111	1Fh	-1.65	110011	33h	-2.65
001100	0Ch	-0.7	100000	20h	-1.7	110100	34h	-2.7
001101	0Dh	-0.75	100001	21h	-1.75	110101	35h	-2.75
001110	0Eh	-0.8	100010	22h	-1.8	110110	36h	-2.8
001111	0Fh	-0.85	100011	23h	-1.85	110111	37h	-2.85
010000	10h	-0.9	100100	24h	-1.9	111000	38h	-2.9
010001	11h	-0.95	100101	25h	-1.95	111001	39h	-2.95
010010	12h	-1	100110	26h	-2	111010	3Ah	-3
010011	13h	-1.05	100111	27h	-2.05			

Restriction

8.2.36 R82H (VDCS): VCOM_DC Setting Register

R82H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VDCS	W	0	1	0	0	0	0	0	1	0	82H
1st Parameter	W	1	-	-	VDCS[5]	VDCS [4]	VDCS [3]	VDCS [2]	VDCS [1]	VDCS [0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command set the VCOM DC value. Driver will base on this value for VCM_DC.

1st Parameter:

Bit	Name	Function
5-0	VDCS[5:0]	**VCOM value**

VCOM[5:0]		Voltage(V)	VCOM[5:0]		Voltage(V)	VCOM[5:0]		Voltage(V)
000000	00h	-0.1	010100	14h	-1.1	101000	28h	-2.1
000001	01h	-0.15	010101	15h	-1.15	101001	29h	-2.15
000010	02h	-0.2	010110	16h	-1.2	101010	2Ah	-2.2
000011	03h	-0.25	010111	17h	-1.25	101011	2Bh	-2.25
000100	04h	-0.3	011000	18h	-1.3	101100	2Ch	-2.3
000101	05h	-0.35	011001	19h	-1.35	101101	2Dh	-2.35
000110	06h	-0.4	011010	1Ah	-1.4	101110	2Eh	-2.4
000111	07h	-0.45	011011	1Bh	-1.45	101111	2Fh	-2.45
001000	08h	-0.5	011100	1Ch	-1.5	110000	30h	-2.5
001001	09h	-0.55	011101	1Dh	-1.55	110001	31h	-2.55
001010	0Ah	-0.6	011110	1Eh	-1.6	110010	32h	-2.6
001011	0Bh	-0.65	011111	1Fh	-1.65	110011	33h	-2.65
001100	0Ch	-0.7	100000	20h	-1.7	110100	34h	-2.7
001101	0Dh	-0.75	100001	21h	-1.75	110101	35h	-2.75
001110	0Eh	-0.8	100010	22h	-1.8	110110	36h	-2.8
001111	0Fh	-0.85	100011	23h	-1.85	110111	37h	-2.85
010000	10h	-0.9	100100	24h	-1.9	111000	38h	-2.9
010001	11h	-0.95	100101	25h	-1.95	111001	39h	-2.95
010010	12h	-1	100110	26h	-2	111010	3Ah	-3
010011	13h	-1.05	100111	27h	-2.05			

Restriction

8.2.37 R90H (PTL): Partial Window Register

R90H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTL	W	0	1	0	0	1	0	0	0	0	90H
1st Parameter	W	1	HRST[7:3]					0	0	0	00h
2nd Parameter	W	1	HRED[7:3]					1	1	1	00h
3rd Parameter	W	1	-	-	-	-	-	-	-	VRST[8]	00h
4th Parameter	W	1	VRST[7:0]								00h
5th Parameter	W	1	-	-	-	-	-	-	-	VRED[8]	00h
6th Parameter	W	1	VRED[7:0]								00h
7th Parameter	W	1	-	-	-	-	-	-	-	PT_SCAN	00h

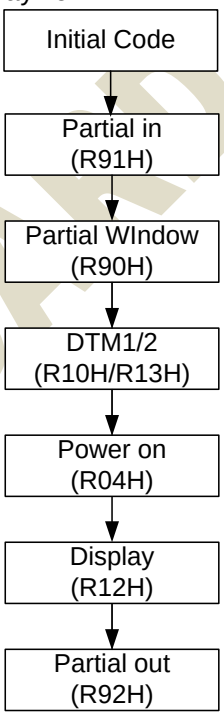
NOTE: "-" Don't care, can be set to VDD or GND level

Description

-This command sets partial window.

Name	Description
HRST[7:3]	Horizontal start channel bank. (value 00h~13h)
HRED[7:3]	Horizontal end channel bank. (value 00h~13h). HRED must be greater than HRST.
VRST[8:0]	Vertical start line. (value 000h~127h)
VRED[8:0]	Vertical end line. (value 000h~127h). VRED must be greater than VRST.
PT_SCAN	0: Gates scan only inside of the partial window. 1: Gates scan both inside and outside of the partial window. (default)

Partial display flow:



Restriction

8.2.38 R91H (PTIN): Partial In Register

R91H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTIN	W	0	1	0	0	1	0	0	0	1	91H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: This command makes the display enter partial mode.
Restriction	

8.2.39 R92H (PTOUT): Partial Out Register

R92H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTOUT	W	0	1	0	0	1	0	0	1	0	92H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: This command makes the display exit partial mode and enter normal mode.
Restriction	

8.2.40 RA0H (PGM): Program Mode

RA0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTIN	W	0	1	0	1	0	0	0	0	0	A0H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is issued, the chip would enter the program mode. The mode would return to standby by hardware reset.
Restriction	This command only actives when BUSY_N = "1".

8.2.41 RA1H (APG): Active Program

RA1H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
APG	W	0	1	0	1	0	0	0	0	1	A1H

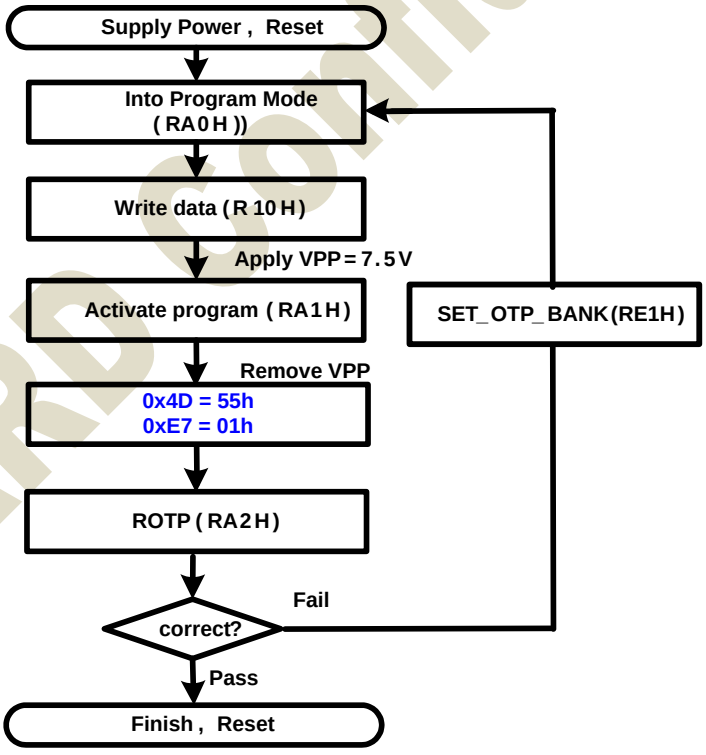
NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	The BUSY flag would change state from 0 to 1 while the programming is completed.

8.2.42 RA2H (ROTP): Read OTP Data

RA2H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
ROTP	W	0	1	0	1	0	0	0	1	0	A2H
1st Parameter	R	1	Dummy								-
2nd Parameter	R	1	The data of address 0x000 in the OTP								-
3rd Parameter	R	1	The data of address 0x001 in the OTP								-
4th Parameter	R	1	:								-
5th Parameter	R	1	The data of address (n-1) in the OTP								-
6th~(m-1)th Parameter	R	1	…..								-
mth Parameter	R	1	The data of address (n) in the OTP								-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: The command is used for reading the content of OTP for checking the data of programming. The value of (n) is depending on the amount of programmed data, the max address = 0xFFF.  The sequence of programming OTP
Restriction	This command only actives when BUSY_N = "1".

8.2.43 RE0H (CCSET): Cascade Setting

RE0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CCSET	W	0	1	1	1	0	0	0	0	0	E0H
1st Parameter	W	1	-	-	-	-	-	-	TSFIX	CCEIN	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	This command is used for cascade. 1st Parameter:

Bit	Name	Description
0	CCEIN	Output clock enable/disable. 0: Output 0V at CL pin. (default) 1: Output clock at CL pin for slave chip.
1	TSFIX	Let the value of slave's temperature is same as the master's. 0: Temperature value is defined by internal temperature sensor/external LM75. (default) 1: Temperature value is defined by TS_SET [7:0] registers.

Restriction	

8.2.44 RE1H (SET_OTP_BANK): Set OTP program bank

RE1H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
SET_OTP_BANK	W	0	1	1	1	0	0	0	0	1	E1H
1st Parameter	W	1	-	-	-	-	-	-	LUT_bank0	reg_bank0	03h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-This command is used to set program bank for registers and LUTs

OTP bank 0 (3K Bytes)		OTP bank 1 (3K Bytes)	
Address(Hex)	Content	Address(Hex)	Content
0x000~0x00B	Temp. segment	0xC00~0xC0B	Temp. segment
0x00C	Vcom DC voltage	0xC0C	Vcom DC voltage
0x00D~0x0BFF	LUTs / Reserved	0xC0D~0x17FF	LUTs / Reserved

1st Parameter:

Bit	Name	Description
0	reg_bank0	0: Program "Temp. segment" and "Default Setting" in bank 1 1: Program "Temp. segment" and "Default Setting" in bank 0
1	LUT_bank0	0: Program "LUTs" in bank 1 1: Program "LUTs" in bank 0

After this command is transmitted, the programming state machine would be activated.

Restriction: The BUSY flag would change state from 0 to 1 while the programming is completed

8.2.45 RE3H (PWS): Power Saving Register

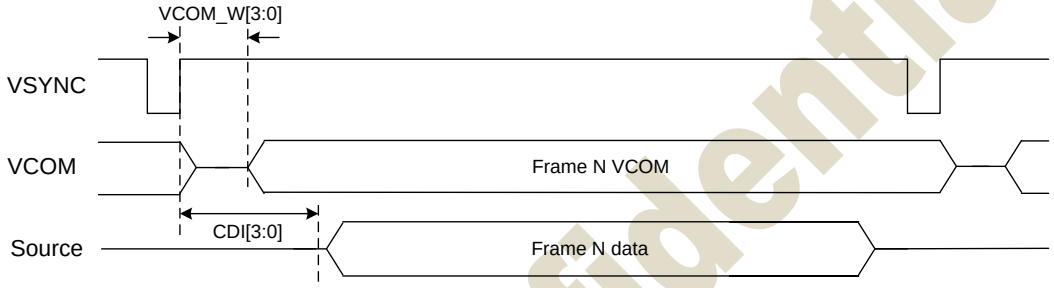
RE3H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWS	W	0	1	1	1	0	0	0	1	1	E3H
1st Parameter	W	1	VCOM_W[3:0]				SD_W[3:0]				00h

NOTE: "-" Don't care, can be set to VDD or GND level

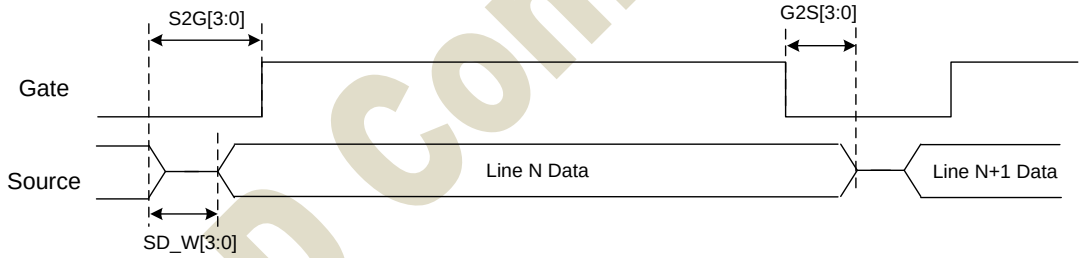
Description

- This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W: VCOM power saving width (unit = line period)



SD_W: Source power saving width (unit = 660nS)



Restriction

8.2.46 RE4H (LVSEL): LVD Voltage Select Register

RE4H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LVSEL	W	0	1	1	1	0	0	1	0	0	E4H
1st Parameter	W	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	LVD_SEL[1:0]: Low Power Voltage Selection
Restriction	

LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V

8.2.47 RE5H (TSSET): Force Temperature

RE5H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSSET	W	0	1	1	1	0	0	1	0	1	E5H
1st Parameter	W	1	TS_SET[7]	TS_SET[6]	TS_SET[5]	TS_SET[4]	TS_SET[3]	TS_SET[2]	TS_SET[1]	TS_SET[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command define as follows:

This command is used to fix the temperature value of master and slave chip in cascade

TS[9:2]/D[10:3]	T (°C)	TS[9:2]/D[10:3]	T (°C)	TS[9:2]/D[10:3]	T (°C)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27
11101010	-22	00000011	3	00011100	28
11101011	-21	00000100	4	00011101	29
11101100	-20	00000101	5	00011110	30
11101101	-19	00000110	6	00011111	31
11101110	-18	00000111	7	00100000	32
11101111	-17	00001000	8	00100001	33
11110000	-16	00001001	9	00100010	34
11110001	-15	00001010	10	00100011	35
11110010	-14	00001011	11	00100100	36
11110011	-13	00001100	12	00100101	37
11110100	-12	00001101	13	00100110	38
11110101	-11	00001110	14	00100111	39
11110110	-10	00001111	15	00101000	40
11110111	-9	00010000	16	00101001	41
11111000	-8	00010001	17	00101010	42
11111001	-7	00010010	18	00101011	43
11111010	-6	00010011	19	00101100	44
11111011	-5	00010100	20	00101101	45
11111100	-4	00010101	21	00101110	46
11111101	-3	00010110	22	00101111	47
11111110	-2	00010111	23	00110000	48
11111111	-1	00011000	24	00110001	49

Restriction

8.3 Register Restriction

Following table will indicate the register restriction:

Register	Refresh Restriction	BUSY_N flag
R00H(PSR)	X	No action
R01H(PWR)	X	No action
R02H(POF)	X	Flag
R03H(PFS)	X	No action
R04H(PON)	X	Flag
R05H(PMES)	X	No action
R06H(BTST)	X	No action
R07H(DSLP)	X	Flag
R10H(DTM1)	X	No action
R11H(DSP)	Valid only read	Flag
R12H(DRF)	X	Flag
R13H(DTM2)	X	No action
R17H(AUTO)	Valid in standby	Flag
R20H(LUTC)	X	No action
R21H(LUTWW)	X	No action
R22H(LUTBW/LUTR)	X	No action
R23H(LUTWB/LUTW)	X	No action
R24H(LUTBB/LUTB)	X	No action
R26H(SET_GROUP)	X	No action
R2AH(LUTOPT)	X	No action
R30H(PLL)	X	No action
R40H(TSC)	Valid only read	Flag
R41H(TSE)	X	No action
R42H(TSW)	X	Flag
R43H(TSR)	Valid only read	Flag
R44H(PBC)	Valid only read	Flag
R50H(CDI)	X	No action
R51H(LPD)	Valid only read	Flag
R60H(TCON)	X	No action
R61H(TRES)	X	No action
R65H(TSGS)	X	No action
R70H(REV)	Valid only read	No action
R71H(FLG)	Valid only read	No action
R80H(AMV)	X	Flag
R81H(VV)	Valid	No action
R82H(VDCS)	X	No action
R90H(PTL)	X	No action
R91H(PTIN)	X	No action
R92H(PTOUT)	X	No action
RA0H(PGM)	X	No action
RA1H(APG)	X	Flag
RA2H(ROTP)	X	Flag
RE0H(CCSET)	X	No action
RE3H(PWS)	X	No action
RE1H(SET_OTP_BANK)	X	No action
RE4H(LVSEL)	X	No action
RE5H(TSSET)	X	No action

9. FUNCTION DESCRIPTION

9.1 Power On/Off and DSLP Sequence

In order to prevent IC fail in power on resetting, the power sequence must be followed as below.

Power on Sequence

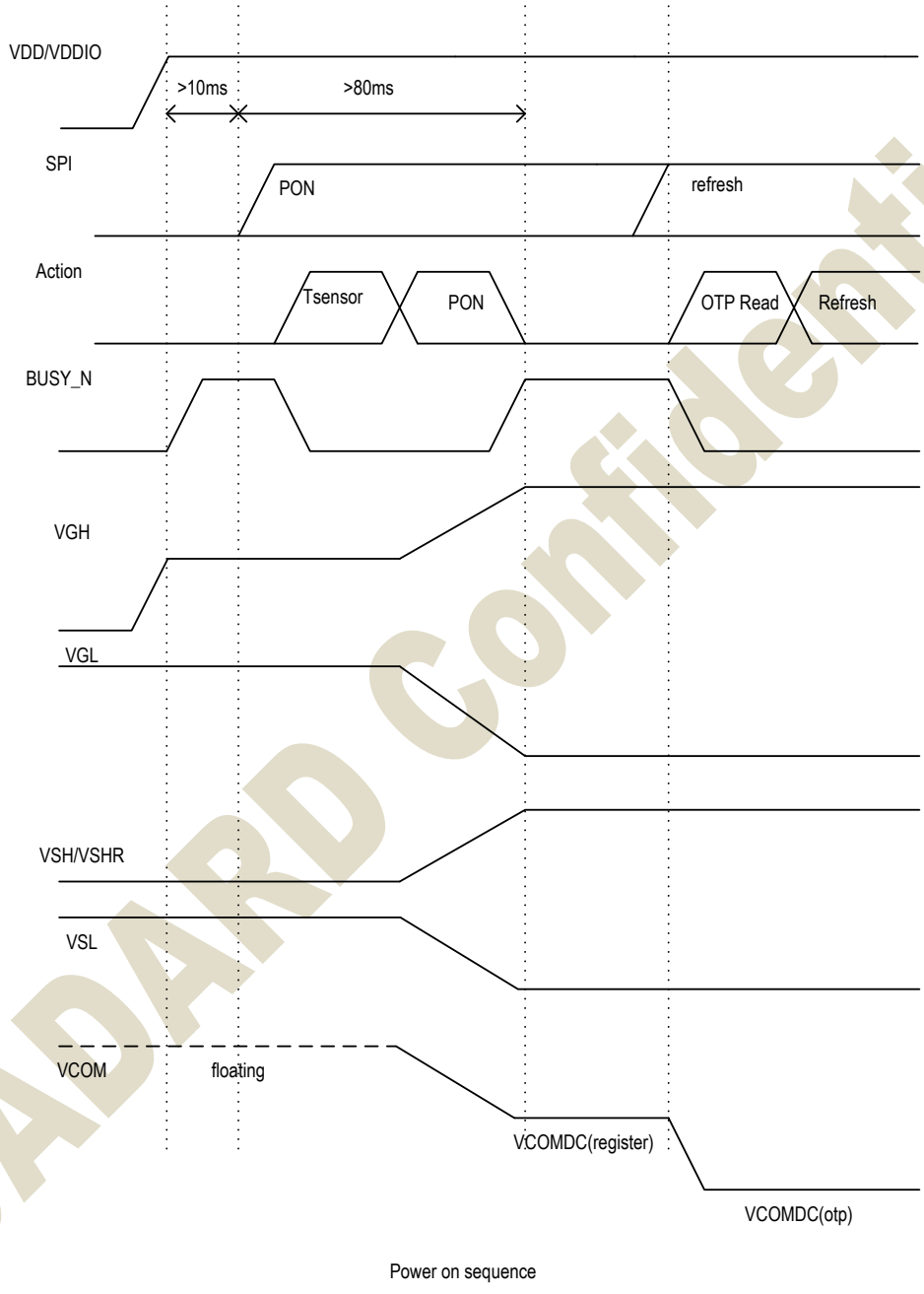


Figure 1: Power on sequence

Power off Sequence

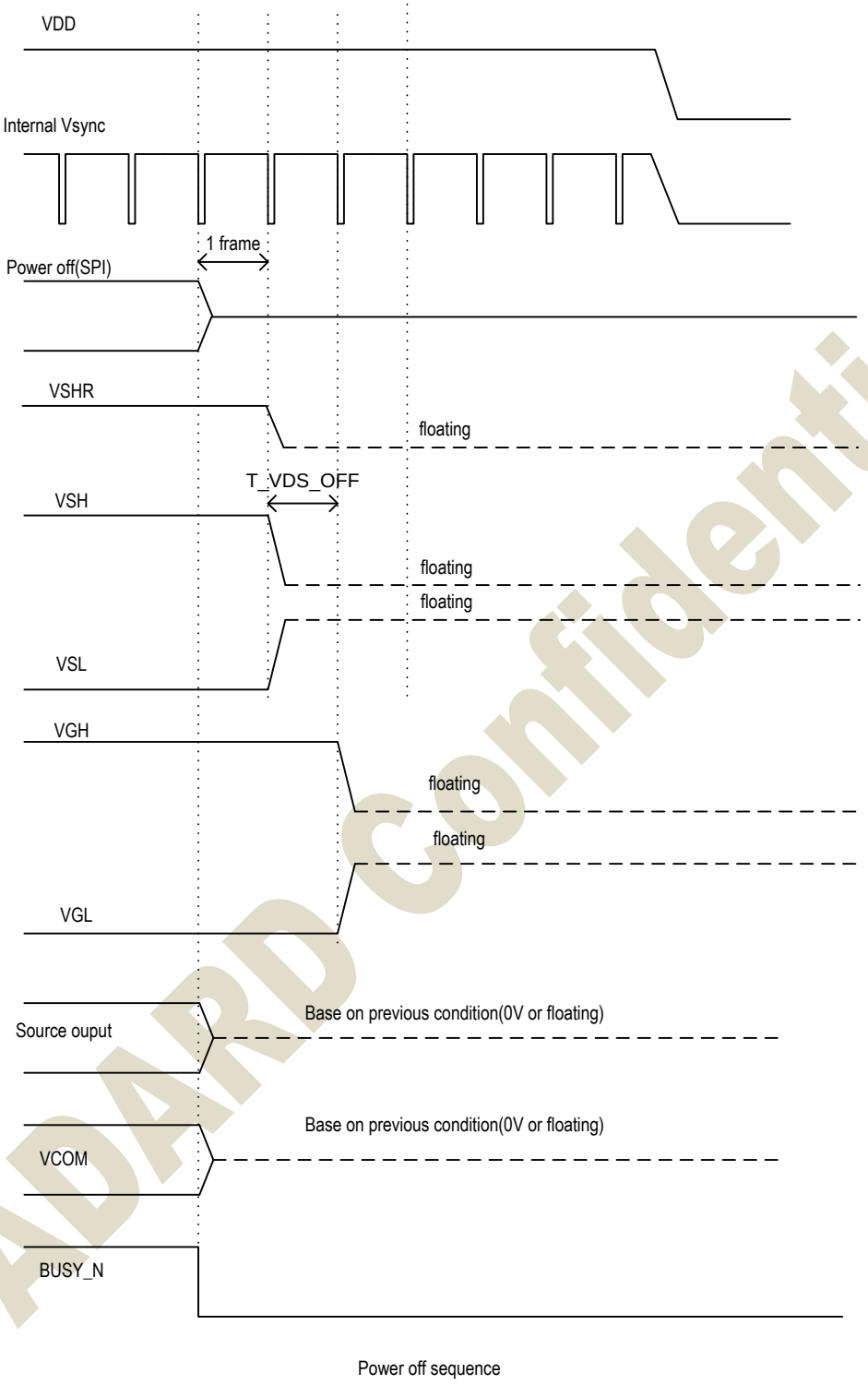


Figure 2: Power off sequence

DSLP sequence

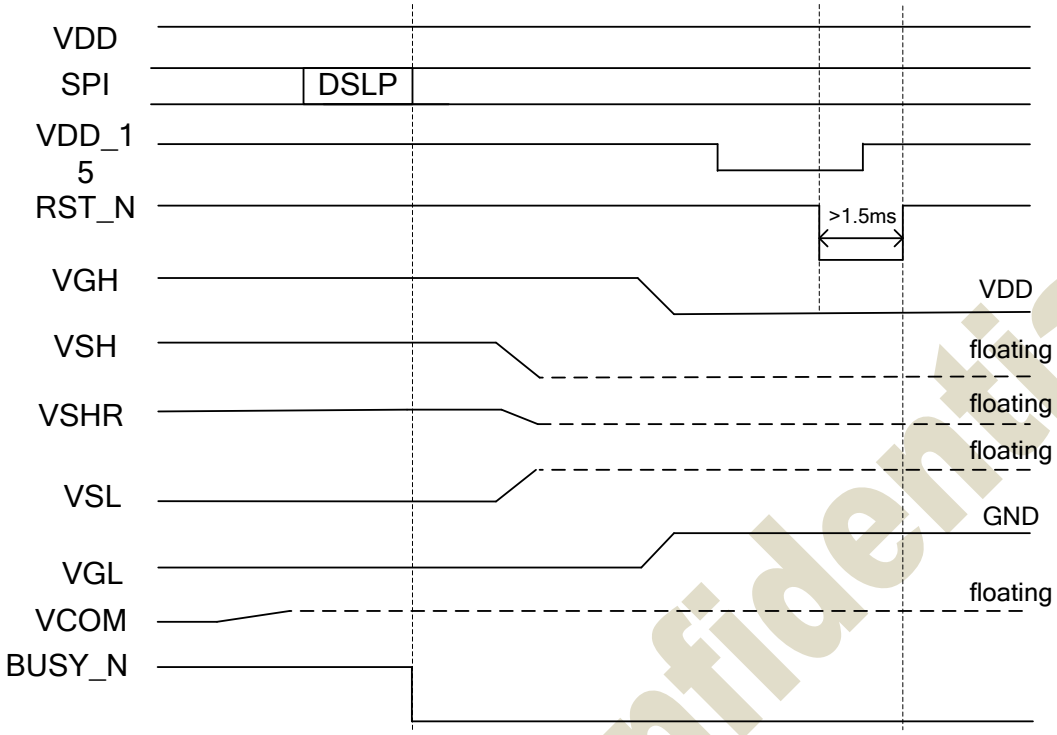


Figure 3: DSLP sequence

9.2 OTP LUT Definition

The OTP size would be 6144 Byte included temperature segment setting and 12 set waveform (maximum).

If TEMP ≦ Boundary0, use TR0 WF

If Boundary0 < TEMP ≦Boundary1, use TR1

If Boundary1 < TEMP ≦ Boundary2, use TR2

……

OTP bank 0 (3K bytes)		OTP bank 1 (3K bytes)	
Address(Hex)	Content	Address(Hex)	Content
000	Check code (0xA5)	C00	Check code (0xA5)
001	Temp. Boundary 0	C01	Temp. Boundary 0
002	Temp. Boundary 1	C02	Temp. Boundary 1
003	Temp. Boundary 2	C03	Temp. Boundary 2
004	Temp. Boundary 3	C04	Temp. Boundary 3
005	Temp. Boundary 4	C05	Temp. Boundary 4
006	Temp. Boundary 5	C06	Temp. Boundary 5
007	Temp. Boundary 6	C07	Temp. Boundary 6
008	Temp. Boundary 7	C08	Temp. Boundary 7
009	Temp. Boundary 8	C09	Temp. Boundary 8
00A	Temp. Boundary 9	C0A	Temp. Boundary 9
00B	Temp. Boundary 10	C0B	Temp. Boundary 10
00C	VCOM DC voltage	C0C	VCOM DC voltage
00D~0F4	TR0 WF	C0D~CF4	TR0 WF
0F5~1DC	TR1 WF	CF5~DDC	TR1 WF
1DD~2C4	TR2 WF	DDD~EC4	TR2 WF
2C5~3AC	TR3 WF	EC5~FAC	TR3 WF
3AD~494	TR4 WF	FAD~1094	TR4 WF
495~57C	TR5 WF	1095~117C	TR5 WF
57D~664	TR6 WF	117D~1264	TR6 WF
665~74C	TR7 WF	1265~134C	TR7 WF
74D~834	TR8 WF	134D~1434	TR8 WF
835~91C	TR9 WF	1435~151C	TR9 WF
91D~A04	TR10 WF	151D~1604	TR10 WF
A05~AEC	TR11 WF	1605~16EC	TR11 WF
AED~AEE	LUT version	16ED~16EE	LUT version
AEF~B1F	Reserved	16EF~171F	Reserved
B20~B5F	Default setting	1720~175F	Default setting
B60~BFF	Reserved	1760~17FF	Reserved

9.2.1 LUT Format in OTP

There are 12 TRs (temperature range) in a bank. Each TR has independent frame rate, voltage, XON settings and LUTs. The format of LUT is different in different mode. In BWR mode, there are only 4 LUTs including LUTC, LUTR, LUTW and LUTB in TRs. All LUT have 8 groups in BWR mode. And the extra options, EOPT is imported to define the end state of source output level. In BW mode, there are 5 LUTs including LUTC, LUTWW, LUTBW, LUTWB and LUTBB in TRs. All LUT have 6 groups in BW mode.

BWR Mode	Description	Addr (Dec)	Addr (Hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note
TR0 WF	Voltage	13	0D	-	-	M[2:0]			N[2:0]			
		14	0E	VGHL_LV[2]	-	-	-	-	-	VGHL_LV[1]	VGHL_LV[0]	
		15	0F	-	-	VSH[5:0]						
		16	10	-	-	VSL[5:0]						
		17	11	OPTEN	VSHR[6:0]							
		18	12	EOPT	-	-	-	-	-	-	-	
		19	13	STATE_XON[7:0]								
		20	14	STATE_XON[15:8]								
	LUTC	21	15	Group Repeat Times[7:0]								Group 1
		22	16	Level Sel.1-1[1:0]	Frame Number1-1[5;0]							
		23	17	Level Sel.1-2[1:0]	Frame Number1-2[5;0]							
		24	18	Level Sel.2-1[1:0]	Frame Number2-1[5;0]							
		25	19	Level Sel.2-2[1:0]	Frame Number2-2[5;0]							
		26	1A	State 1 Repeat Times[7;0]								
		27	1B	State 2 Repeat Times[7;0]								
		28	1C	Group 2 ~ Group 8								
		76	4C									
	LUTR	77	4D	Group Repeat Times[7:0]								Group 1
		78	4E	Level Sel.1-1[1:0]	Frame Number1-1[5;0]							
		79	4F	Level Sel.1-2[1:0]	Frame Number1-2[5;0]							
		80	50	Level Sel.2-1[1:0]	Frame Number2-1[5;0]							
		81	51	Level Sel.2-2[1:0]	Frame Number2-2[5;0]							
		82	52	State 1 Repeat Times[7;0]								
		83	53	State 2 Repeat Times[7;0]								
		84	54	Group 2 ~ Group 8								
		132	84									
	LUTW	133	85	Group Repeat Times[7:0]								Group 1
		134	86	Level Sel.1-1[1:0]	Frame Number1-1[5;0]							
		135	87	Level Sel.1-2[1:0]	Frame Number1-2[5;0]							
		136	88	Level Sel.2-1[1:0]	Frame Number2-1[5;0]							
		137	89	Level Sel.2-2[1:0]	Frame Number2-2[5;0]							
		138	8A	State 1 Repeat Times[7;0]								
		139	8B	State 2 Repeat Times[7;0]								
		140	8C	Group 2 ~ Group 8								
		188	BC									
	LUTB	189	BD	Group Repeat Times[7:0]								Group 1
		190	BE	Level Sel.1-1[1:0]	Frame Number1-1[5;0]							
		191	BF	Level Sel.1-2[1:0]	Frame Number1-2[5;0]							
		192	C0	Level Sel.2-1[1:0]	Frame Number2-1[5;0]							
		193	C1	Level Sel.2-2[1:0]	Frame Number2-2[5;0]							
		194	C2	State 1 Repeat Times[7;0]								
		195	C3	State 2 Repeat Times[7;0]								
		196	C4	Group 2 ~ Group 8								
		244	F4									

BW Mode	Description	Addr (Dec)	Addr (Hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note
TR0 WF	Voltage	13	0D	-	-	M[2:0]			N[2:0]			
		14	0E	VGHL_LV[2]	-	-	-	-	-	VGHL_LV[1]	VGHL_LV[0]	
		15	0F	-	-	VSH[5:0]						
		16	10	-	-	VSL[5:0]						
		17	11	OPTEN	VSHR[6:0]							
		18	12	EOPT	-	-	-	-	-	-	-	
		19	13	STATE_XON[7:0]								
		20	14	STATE_XON[15:8]								
	LUTC	21	15	Group Repeat Times[7:0]								Group 1
		22	16	Level Sel.1-1[1:0]		Frame Number1-1[5;0]						
		23	17	Level Sel.1-2[1:0]		Frame Number1-2[5;0]						
		24	18	Level Sel.2-1[1:0]		Frame Number2-1[5;0]						
		25	19	Level Sel.2-2[1:0]		Frame Number2-2[5;0]						
		26	1A	State 1 Repeat Times[7;0]								
		27	1B	State 2 Repeat Times[7;0]								
		28	1C	Group 2 ~ Group 6								
		62	3E									
	LUTWW	63	3F	Group Repeat Times[7:0]								Group 1
		64	40	Level Sel.1-1[1:0]		Frame Number1-1[5;0]						
		65	41	Level Sel.1-2[1:0]		Frame Number1-2[5;0]						
		66	42	Level Sel.2-1[1:0]		Frame Number2-1[5;0]						
		67	43	Level Sel.2-2[1:0]		Frame Number2-2[5;0]						
		68	44	State 1 Repeat Times[7;0]								
		69	45	State 2 Repeat Times[7;0]								
		70	46	Group 2 ~ Group 6								
		104	68									
	LUTBW	105	69	Group Repeat Times[7:0]								Group 1
		106	6A	Level Sel.1-1[1:0]		Frame Number1-1[5;0]						
		107	6B	Level Sel.1-2[1:0]		Frame Number1-2[5;0]						
		108	6C	Level Sel.2-1[1:0]		Frame Number2-1[5;0]						
		109	6D	Level Sel.2-2[1:0]		Frame Number2-2[5;0]						
		110	6E	State 1 Repeat Times[7;0]								
		111	6F	State 2 Repeat Times[7;0]								
		112	70	Group 2 ~ Group 6								
		146	92									
	LUTWB	147	93	Group Repeat Times[7:0]								Group 1
		148	94	Level Sel.1-1[1:0]		Frame Number1-1[5;0]						
		149	95	Level Sel.1-2[1:0]		Frame Number1-2[5;0]						
		150	96	Level Sel.2-1[1:0]		Frame Number2-1[5;0]						
		151	97	Level Sel.2-2[1:0]		Frame Number2-2[5;0]						
		152	98	State 1 Repeat Times[7;0]								
		153	99	State 2 Repeat Times[7;0]								
		154	9A	Group 2 ~ Group 6								
		188	BC									
	LUTBB	189	BD	Group Repeat Times[7:0]								Group 1
		190	BE	Level Sel.1-1[1:0]		Frame Number1-1[5;0]						
		191	BF	Level Sel.1-2[1:0]		Frame Number1-2[5;0]						
		192	C0	Level Sel.2-1[1:0]		Frame Number2-1[5;0]						
		193	C1	Level Sel.2-2[1:0]		Frame Number2-2[5;0]						
		194	C2	State 1 Repeat Times[7;0]								
		195	C3	State 2 Repeat Times[7;0]								
		196	C4	Group 2 ~ Group 6								
		230	E6									
		231	E7	Reserved								
		244	F4									

9.2.2 Default Setting Format in OTP

	Addr. (Dec)	Addr. (Hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value (Hex)
--	2848	B20	Enable OTP Setting (0xA5)								A5
R00H-1	2849	B21	RES[1:0]		REG_EN	BWR	UD	SHL	SHD_N	RST_N	0F
R01H	2850	B22	-	-	-	-	-	-	VDS_EN	VDG_EN	03
	2851	B23	VGHL_LV[2]	-	-	-	-	VCOM_HV	VGHL_LV[1:0]		00
	2852	B24	-	-	VSH[5:0]						26
	2853	B25	-	-	VSL[5:0]						26
	2854	B26	OPTEN	VSHR[6:0]							06
R03H	2855	B27	-	-	T_VDS_OFF[1:0]		-	-	-	-	00
R06H	2856	B28	BT_PHA[7:0]								17
	2857	B29	BT_PHB[7:0]								17
	2858	B2A	-	-	BT_PHC[5:0]						17
--	2859~2860	B2B~B2C	Reserved								FF
RE4H	2861	B2D	-	-	-	-	-	-	LVD_SEL[1:0]		03
RE3H	2862	B2E	VCOM_W[3:0]				SD_W[3:0]				00
--	2863	B2F	Reserved								FF
R00H-2	2864	B30	-	-	-	VCMZ	TS_AUTO	VGLTIEG	NORG	VC_LUTZ	09
--	2865	B31	Reserved								FF
R26H	2866	B32	-	-	-	-	-	-	GROUP_SEL[1:0]		00
R30H	2867	B33	-	-	M[2:0]			N[2:0]			3C
R41H	2868	B34	TSE	-	TO[5:0]						00
R42H	2869	B35	WATTR[7:0]								00
	2870	B36	WMSB[7:0]								00
	2871	B37	WLSB[7:0]								00
R50H	2872	B38	VBD[1:0]		DDX[1:0]		CDI[3:0]				D7
R60H	2873	B39	S2G[3:0]				G2S[3:0]				22
--	2874	B3A	Reserved								FF
R61H	2875	B3B	HRES[7:3]					-	-	-	00
	2876	B3C	-	-	-	-	-	-	-	VRES[8]	00
	2877	B3D	VRES[7:0]								00
R80H	2878	B3E	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE	10
--	2879	B3F	Reserved								FF
RE0H	2880	B40	-	-	-	-	-	-	TSFIX	CCEIN	00
RE5H	2881	B41	TS_SET[7:0]								00
--	2882	B42	Reserved								FF
R65H	2883	B43	S_Start[7:3]					-	-	-	00
	2884	B44	-	-	-	G_Scan	-	-	-	G_Start[8]	00
	2885	B45	G_Start[7:0]								00
--	2886~2887	B46~B47	Reserved								FF
RE1H	2888	B48	-	-	-	-	-	-	LUT_Bank0	REG_Bank0	03
Slave Setting											
R00H	2889	B49	slv_res[1:0]		slv_reg_en	slv_bwr	slv_ud	slv_shl	slv_shd_n	slv_rst_n	FF
	2890	B4A	-	-	-	slv_vcmz	slv_ts_auto	slv_vgltieg	slv_norg	slv_vc_lutz	FF
R62H	2891	B4B	slv_sstart[7:3]					-	-	-	FF
	2892	B4C	-	-	-	slv_gscan	-	-	-	slv_gstart[8]	FF
	2893	B4D	slv_gstart[7:0]								FF
--	2894~2911	B4E~B5F	Reserved								FF

9.3 Data transmission waveform

Example1: LUT all states complete or phase number=0, the driver will send 2 frame VCOM and data to 0 v.

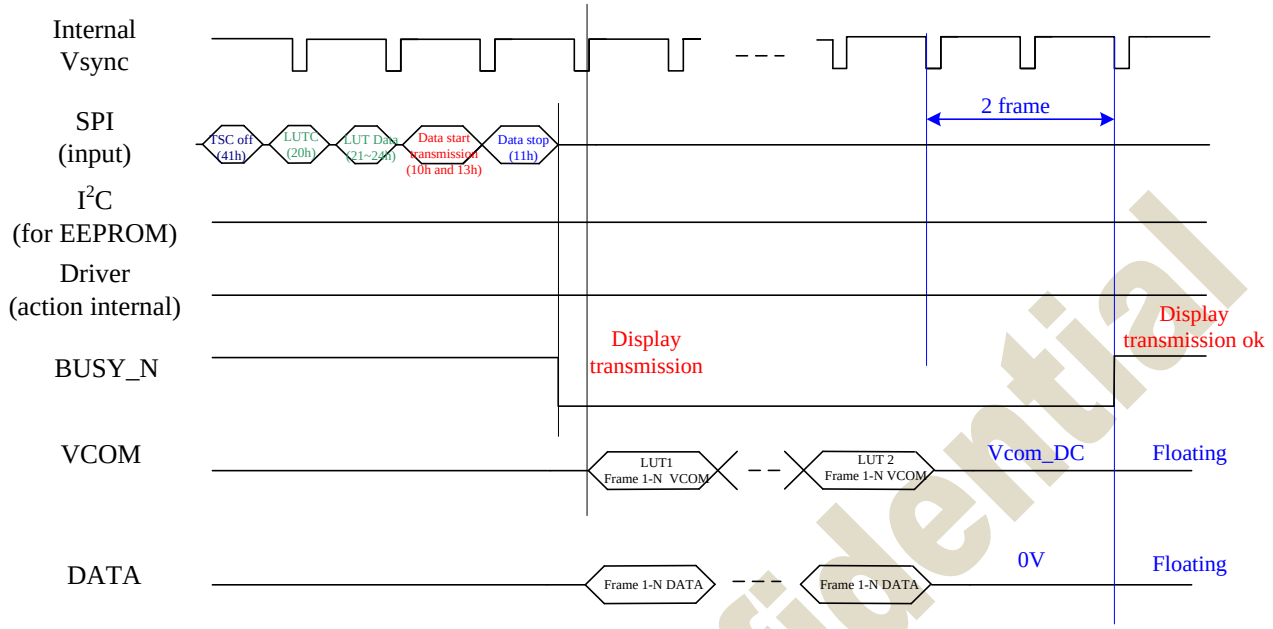


Figure 3: Data transmission example1 waveform

Example2: While level selection in LUT is “11”, the driver will float VCOM and data. (EOPT=0)

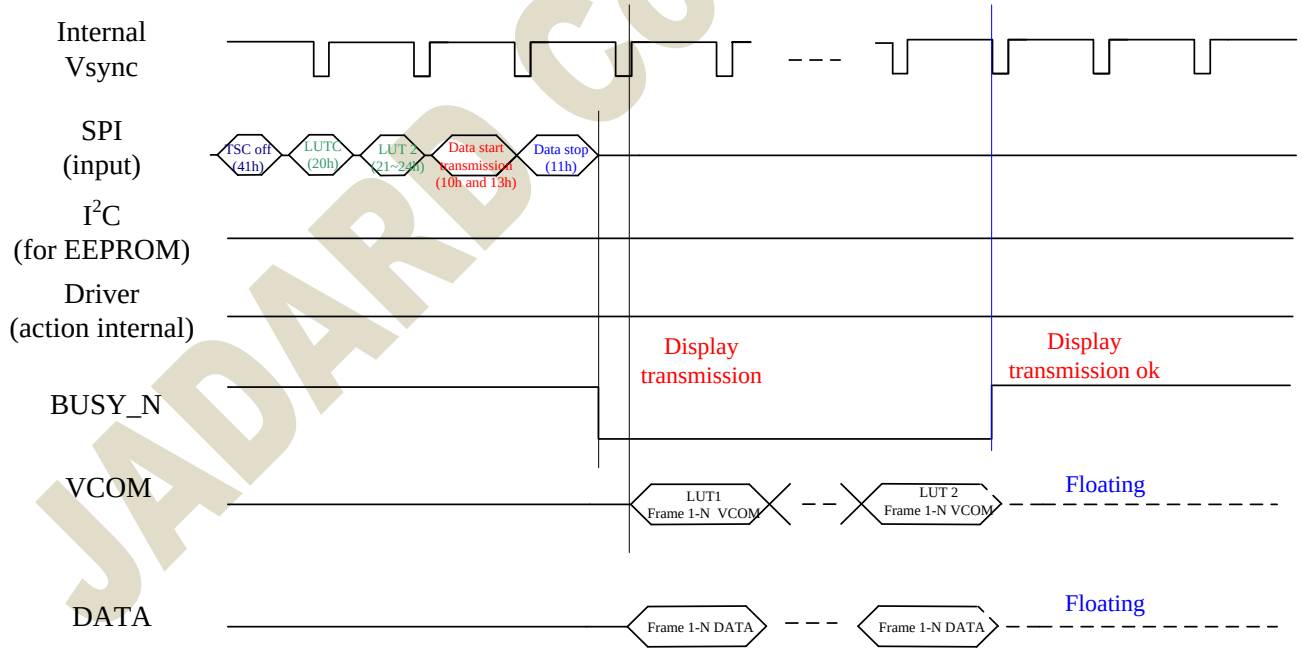


Figure 4: Data transmission example2 waveform

Example3: While level selection in LUT is “11”, the driver will float VCOM and keep last frame data. (EOPT=1)

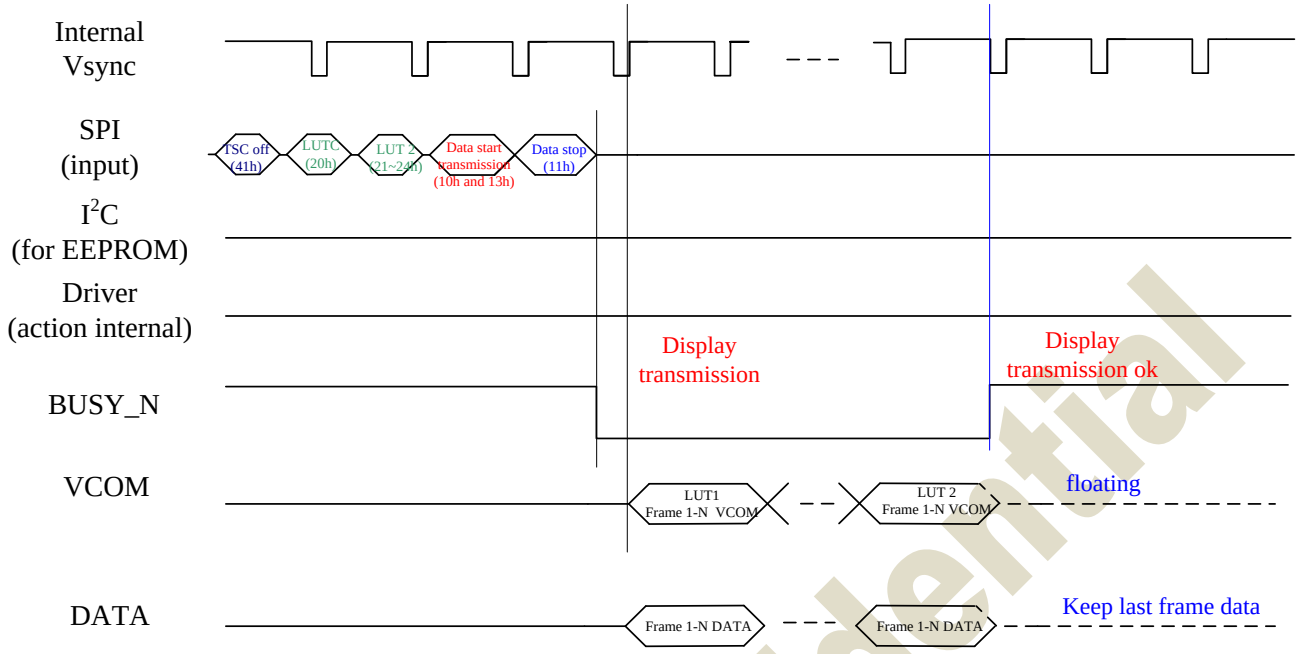


Figure 5: Data transmission example3 waveform

9.5 Display refresh waveform

Example1: LUT all states complete or phase number=0, the driver will send 2 frame VCOM and data to 0 v.

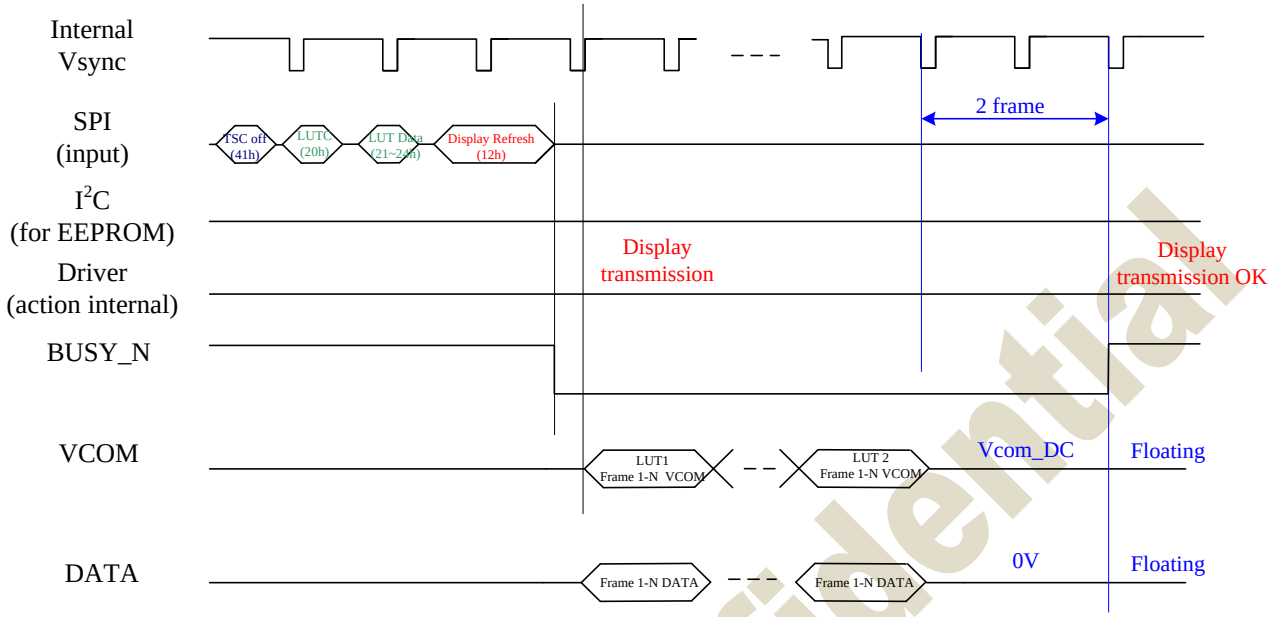


Figure 6: Display refresh example1 waveform

Example2: While level selection in LUT is “11”, the driver will float VCOM and data. (EOPT=0)

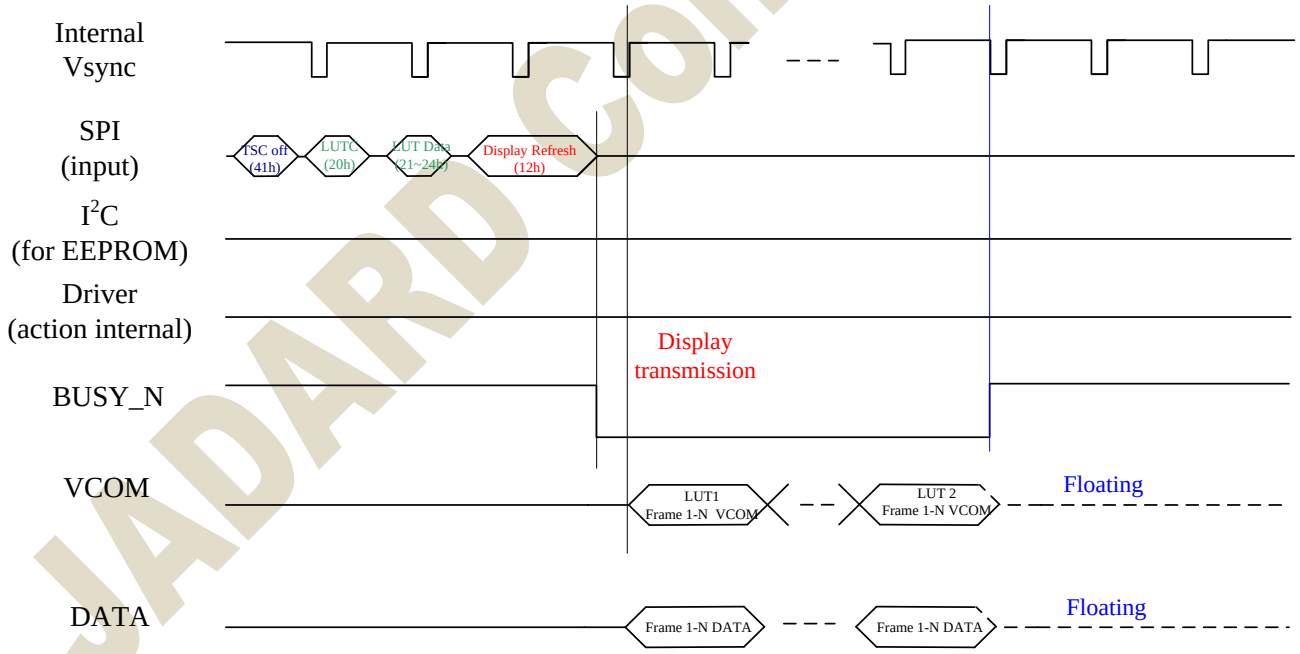


Figure 7: Display refresh example2 waveform

Example3: While level selection in LUT is “11”, the driver will float VCOM and keep last frame data. (EOPT=1)

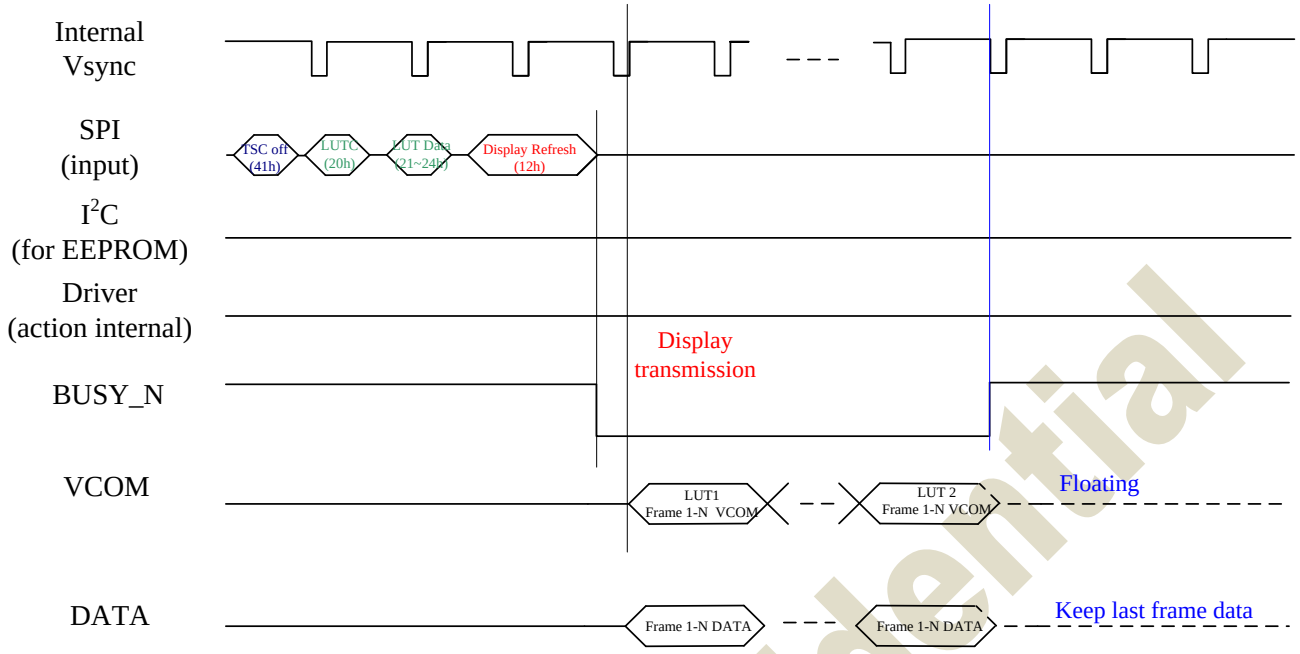


Figure 8: Display refresh example3 waveform

10. ELECTRICAL SPECIFICATIONS

10.1 Absolute Maximum Rating

Parameter	Symbol	Min.	Max.	Unit
Logic supply voltage	VDD, AVDD,VDDIO, VDD1,VPP	-0.3	+6.0	V
Digital input voltage	VI	-0.3	VDDIO+0.3	V
Supply range	VGH-VGL	VGL-0.3	VGH+0.3	V
Analog supply	VSH	+6.4	+15	V
Analog supply	VSL	-15	-6.4	V
Analog supply	VSHR	2.4	+15	
Supply voltage	VGH	+15	+20	V
Supply voltage	VGL	-20	-15	V
Storage temperature	T_{STG}	-55	125	℃

Note:
Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied.
Exposing device to the absolute maximum ratings in a long period of time may degrade the device and affect its reliability.

10.2 Digital DC Characteristic

DC electrical characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
IO Supply Voltage	VDDIO	2.3	3.3	3.6	V	
Digital/Analog supply voltage	VDD	2.3	3.3	3.6	V	
DCDC power input voltage	AVDD	2.3	3.3	3.6	V	
1.5V output voltage	VDD_15	1.35	1.5	1.65		
1.5V input voltage	VDD_15	1.35	1.5	1.65		
OTP program power	VOTP	8.0	8.25	8.5		
Digital ground	VSS		0			
DCDC ground	VSSP		0			
Low Level Input Voltage	Vil	GND	-	0.3xVDD	V	Digital input pins
High Level Input Voltage	Vih	0.7xVIO	-	VIO	V	Digital input pins
High Level Output Voltage	Voh	VIO-0.4	-	-	V	Digital output pins; IOH = 400μA
High Level Output Voltage	Vohd	VDD1-0.4	-	-	V	Digital output pins; IOH = 400μA DRVD, DRVU
Low Level Output Voltage	Vol	GND	-	GND+0.4	V	Digital output pins; IOL = -400μA
Input Leakage Current	Iin	-1.0	-	+1.0	uA	Digital input pins, except pull-up, pull-down pin
Pull-up/down impedance	Rin	-	200K		ohm	
Digital Stand-by Current (power off mode)	IstVDD*	-	0	1	uA	All stopped
Digital Operating Current	IVDD*	-	0.5	2.0	mA	
IO Stand-by Current (power off mode)	IstVDDIO*	-	0.4	1.0	uA	All stopped
IO Operating Current	IVDDIO*	-	-	0.2	mA	No load
Operating Current	IVDD1*	-	-	TBD	mA	
Operating temperature	T_{op}	-30	-	85	℃	

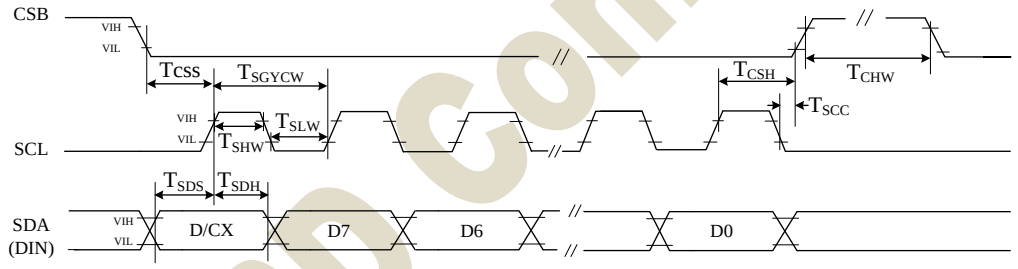
NOTE: typ. and max. values to be confirmed by design

10.3 Analog DC Characteristics

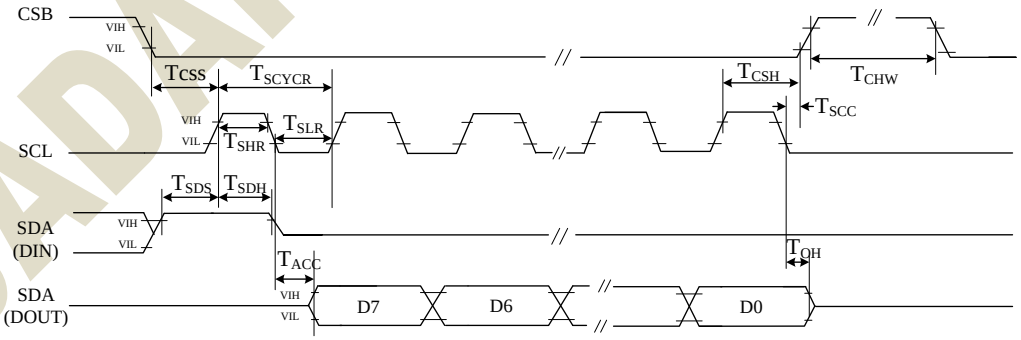
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Positive Source voltage	VSH		15		V	For source driver/VCOM
Positive Source voltage dev	dVSH	-200	0	+200	mV	
Negative Source voltage	VSL		-15		V	For source driver/VCOM
Negative Source voltage dev	dVSL	-200	-	+200	mV	
Positive Source voltage for Red dev.	dVSHR	-200	-	+200	mV	
VCOM voltage dev.	dVCOM	-200	-	+200	mV	
Dynamic Range of Output	Vdr	0.1	-	VSH-0.1	V	
Voltage Range of VGH - VGL	VGH-VGL	-	-	40	V	
Negative Gate voltage	VGL	-15	-	-20	V	For gate driver
Positive Gate voltage	VGH	15		20	V	For gate driver
Positive HV Stand-by Current (power off mode)	IstVGH*	-	0	0.2	uA	Include VSH power With load
Positive HV Operating Current	IVGH*	-	0.7	1.1	mA	Include VSH power With load all SD=L VCOM external resistor divider not included
Positive HV Operating Current	IVGH*	-	0.8	1.2	mA	Include VSH power With load all SD=H VCOM external resistor divider not included
Negative HV Stand-by Current (power off mode)	IstVGL*	-	0	0.2	μA	Include VSH power With load
Negative HV Operating Current	IVGL*	-	0.8	1.2	mA	Include VSL power With load all SD=L
Negative HV Operating Current	IVGL*	-	0.9-	1.3	mA	Include VSL power With load all SD=H
VINT1 Stand-by Current (power off mode)	IstVINT1*		0	0.01	μA	
VINT1 Operating Current	IVINT1*			0.3	mA	
Voltage	IVINT1*			0.3	mA	

10.4 AC Characteristics

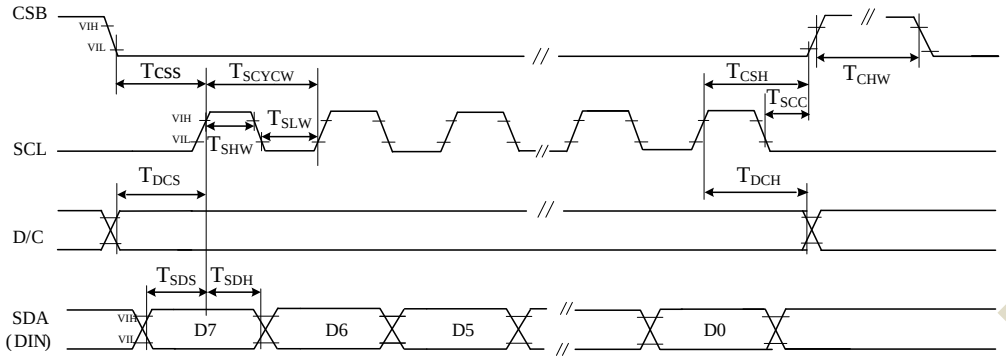
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SERIAL COMMUNICATION						
CSB	T_{CSS}	60			ns	Chip select setup time
	T_{CSH}	65			ns	Chip select hold time
	T_{SCC}	20			ns	Chip select CSB setup time
	T_{CHW}	40			ns	Chip select setup time
SCL	T_{SCYCW}	100			ns	Serial clock cycle (Write)
	T_{SHW}	35			ns	SCL “H” pulse width (Write)
	T_{SLW}	35			ns	SCL “L” pulse width (Write)
	T_{SCYCR}	150			ns	Serial clock cycle (Read)
	T_{SHR}	60			ns	SCL “H” pulse width (Read)
	T_{SLR}	60			ns	SCL “L” pulse width (Read)
SDA (DIN) (DOUT)	T_{SDS}	30			ns	Data setup time
	T_{SDH}	30			ns	Data hold time
	T_{ACC}			50	ns	Access time
	T_{OH}	15			ns	Output disable time
D/C	T_{DCS}	20			ns	DC setup time
	T_{DCH}	20			ns	DC hold time



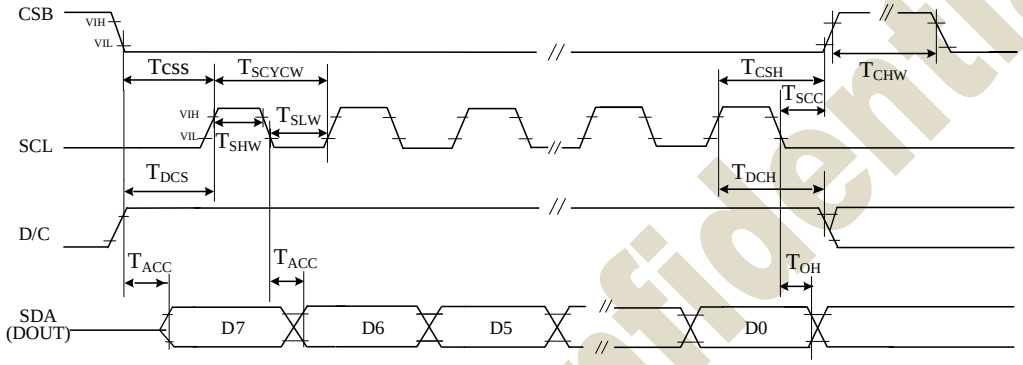
3 pin serial interface characteristics (write mode)



3 pin serial interface characteristics (read mode)



4 pin serial interface characteristics(write mode)

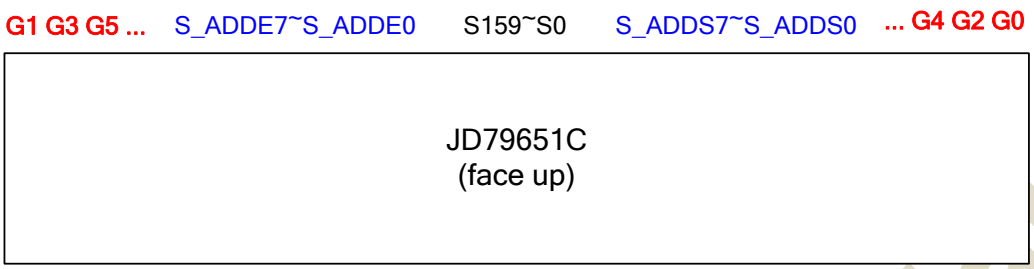


4 pin serial interface characteristics(read mode)

Figure 8: SPI interface timing

11. CHIP OUTLINE DIMENSIONS

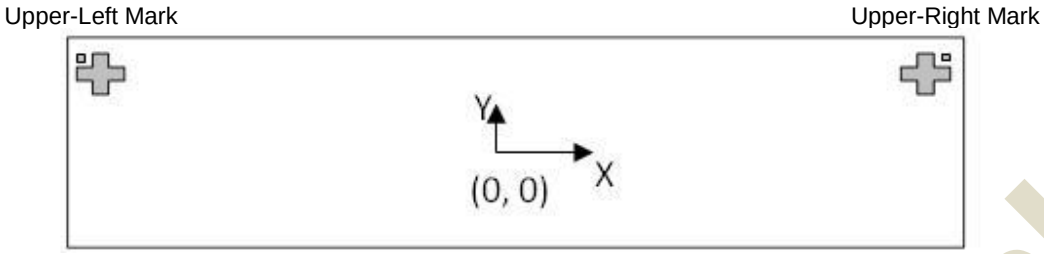
11.1 Circuit/Bump View



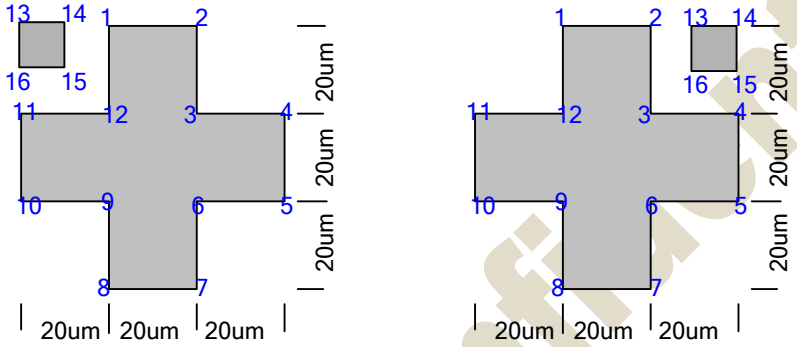
Die Size:	9531um*981um
Die Thickness:	230 μm ± 20μm (Polish)
Die TTV:	(D_{MAX} – D_{MIN}) within die ≤ 2μm
Bump Height:	12 μm ± 2μm
	(H_{MAX} – H_{MIN}) within die ≤ 2μm
Hardness:	75 Hv ±25Hv
Coordinate origin:	Chip center

12. ALIGNMENT MARK INFORMATION

12.1 Location:



Shapes and Points:



Point Coordinates:

Point	Upper-Left Mark		Upper-Right Mark	
	X	Y	X	Y
Center	-4665	390	4665	390
1	-4675	420	4655	420
2	-4655	420	4675	420
3	-4655	400	4675	400
4	-4635	400	4695	400
5	-4635	380	4695	380
6	-4655	380	4675	380
7	-4655	360	4675	360
8	-4675	360	4655	360
9	-4675	380	4655	380
10	-4695	380	4635	380
11	-4695	400	4635	400
12	-4675	400	4655	400
13	-4695	420	4685	420
14	-4685	420	4695	420
15	-4685	410	4695	410
16	-4695	410	4685	410

12.2 Pad coordinates

No.	Name	X-axis	Y-axis	W	H
1	DUMMY	-4646	-398	28	70
2	VCOM	-4600	-398	28	70
3	VCOM	-4554	-398	28	70
4	VCOM	-4508	-398	28	70
5	VCOM	-4462	-398	28	70
6	VCOM	-4416	-398	28	70
7	VCOM	-4370	-398	28	70
8	VCOM	-4324	-398	28	70
9	VCOM	-4278	-398	28	70
10	VSSA	-4232	-398	28	70
11	VGL	-4186	-398	28	70
12	VGL	-4140	-398	28	70
13	VGL	-4094	-398	28	70
14	VGL	-4048	-398	28	70
15	VGL	-4002	-398	28	70
16	VGL	-3956	-398	28	70
17	VGL	-3910	-398	28	70
18	VGL	-3864	-398	28	70
19	VGL	-3818	-398	28	70
20	VGL	-3772	-398	28	70
21	VGL	-3726	-398	28	70
22	VGL	-3680	-398	28	70
23	VGL	-3634	-398	28	70
24	VGL	-3588	-398	28	70
25	VGL	-3542	-398	28	70
26	VGL	-3496	-398	28	70
27	VSSA	-3450	-398	28	70
28	VSL	-3404	-398	28	70
29	VSL	-3358	-398	28	70
30	VSL	-3312	-398	28	70
31	VSL	-3266	-398	28	70
32	VSL	-3220	-398	28	70
33	VSL	-3174	-398	28	70
34	VSL	-3128	-398	28	70
35	VSL	-3082	-398	28	70
36	VSL	-3036	-398	28	70
37	VSL	-2990	-398	28	70
38	VSSA	-2944	-398	28	70
39	VGH	-2898	-398	28	70
40	VGH	-2852	-398	28	70
41	VGH	-2806	-398	28	70
42	VGH	-2760	-398	28	70
43	VGH	-2714	-398	28	70
44	VGH	-2668	-398	28	70
45	VGH	-2622	-398	28	70
46	VGH	-2576	-398	28	70
47	VGH	-2530	-398	28	70
48	VGH	-2484	-398	28	70
49	VGH	-2438	-398	28	70
50	VGH	-2392	-398	28	70
51	VSSA	-2346	-398	28	70
52	VSH	-2300	-398	28	70
53	VSH	-2254	-398	28	70
54	VSH	-2208	-398	28	70
55	VSH	-2162	-398	28	70
56	VSH	-2116	-398	28	70
57	VSH	-2070	-398	28	70
58	VSH	-2024	-398	28	70

No.	Name	X-axis	Y-axis	W	H
59	VSH	-1978	-398	28	70
60	VSH	-1932	-398	28	70
61	VSH	-1886	-398	28	70
62	VSSA	-1840	-398	28	70
63	VOTP	-1794	-398	28	70
64	VOTP	-1748	-398	28	70
65	VOTP	-1702	-398	28	70
66	VOTP	-1656	-398	28	70
67	VOTP	-1610	-398	28	70
68	VOTP	-1564	-398	28	70
69	VDD_15V	-1518	-398	28	70
70	VDD_15V	-1472	-398	28	70
71	VDD_15V	-1426	-398	28	70
72	VDD_15V	-1380	-398	28	70
73	VDD_15V	-1334	-398	28	70
74	VDD_15V	-1288	-398	28	70
75	VDD_15V	-1242	-398	28	70
76	VDD_15V	-1196	-398	28	70
77	VSSA	-1150	-398	28	70
78	VSSA	-1104	-398	28	70
79	VSSA	-1058	-398	28	70
80	VSSA	-1012	-398	28	70
81	VSSA	-966	-398	28	70
82	VSSA	-920	-398	28	70
83	VSSA	-874	-398	28	70
84	VSSA	-828	-398	28	70
85	VSSA	-782	-398	28	70
86	VSSA	-736	-398	28	70
87	VSSA	-690	-398	28	70
88	VSSA	-644	-398	28	70
89	VSS	-598	-398	28	70
90	VSS	-552	-398	28	70
91	VSS	-506	-398	28	70
92	VSS	-460	-398	28	70
93	VSS	-414	-398	28	70
94	VSS	-368	-398	28	70
95	VSS	-322	-398	28	70
96	VSS	-276	-398	28	70
97	VSS	-230	-398	28	70
98	VSS	-184	-398	28	70
99	T_IN[1]	-138	-398	28	70
100	T_IN[0]	-92	-398	28	70
101	VDD	-46	-398	28	70
102	VDD	0	-398	28	70
103	VDD	46	-398	28	70
104	VDD	92	-398	28	70
105	VDD	138	-398	28	70
106	VDD	184	-398	28	70
107	VDD	230	-398	28	70
108	VDD	276	-398	28	70
109	VDD	322	-398	28	70
110	VDD	368	-398	28	70
111	VDDIO	414	-398	28	70
112	VDDIO	460	-398	28	70
113	VDDIO	506	-398	28	70
114	VDDIO	552	-398	28	70
115	VDDIO	598	-398	28	70
116	VDDIO	644	-398	28	70

No.	Name	X-axis	Y-axis	W	H
117	VDDIO	690	-398	28	70
118	T_DEBUG[7]	736	-398	28	70
119	T_DEBUG[6]	782	-398	28	70
120	VDDP	828	-398	28	70
121	VDDP	874	-398	28	70
122	VDDP	920	-398	28	70
123	VDDP	966	-398	28	70
124	T_DEBUG[5]	1012	-398	28	70
125	T_DEBUG[4]	1058	-398	28	70
126	T_DEBUG[4]	1104	-398	28	70
127	T_DEBUG[3]	1150	-398	28	70
128	T_DEBUG[3]	1196	-398	28	70
129	DUMMY[1]	1242	-398	28	70
130	SDA	1288	-398	28	70
131	SCL	1334	-398	28	70
132	VSS	1380	-398	28	70
133	CSB	1426	-398	28	70
134	VDDIO	1472	-398	28	70
135	T_DEBUG[2]	1518	-398	28	70
136	VSS	1564	-398	28	70
137	DC	1610	-398	28	70
138	VDDIO	1656	-398	28	70
139	T_DEBUG[1]	1702	-398	28	70
140	VSS	1748	-398	28	70
141	RST_N	1794	-398	28	70
142	BUSY_N	1840	-398	28	70
143	SYNCC	1886	-398	28	70
144	VDDIO	1932	-398	28	70
145	T_DEBUG[8]	1978	-398	28	70
146	VSS	2024	-398	28	70
147	T_DEBUG[0]	2070	-398	28	70
148	VDDIO	2116	-398	28	70
149	BS	2162	-398	28	70
150	VSS	2208	-398	28	70
151	T_EN_DIG	2254	-398	28	70
152	VDDIO	2300	-398	28	70
153	PCKI	2346	-398	28	70
154	VSS	2392	-398	28	70
155	MS	2438	-398	28	70
156	VDDIO	2484	-398	28	70
157	TSDA	2530	-398	28	70
158	TSDA	2576	-398	28	70
159	TSCL	2622	-398	28	70
160	TSCL	2668	-398	28	70
161	PCKO	2714	-398	28	70
162	SYNCD	2760	-398	28	70
163	T_EX_SYSCLK	2806	-398	28	70
164	T_EX_REFCLK	2852	-398	28	70
165	VSHR	2898	-398	28	70
166	VSHR	2944	-398	28	70
167	VSHR	2990	-398	28	70
168	VSHR	3036	-398	28	70
169	VSHR	3082	-398	28	70
170	VSHR	3128	-398	28	70
171	VSHR	3174	-398	28	70
172	VSHR	3220	-398	28	70
173	DUMMY[2]	3266	-398	28	70
174	DUMMY[3]	3312	-398	28	70
175	DUMMY[4]	3358	-398	28	70
176	DUMMY[5]	3404	-398	28	70

No.	Name	X-axis	Y-axis	W	H
177	DUMMY[6]	3450	-398	28	70
178	DUMMY[7]	3496	-398	28	70
179	VSSA	3542	-398	28	70
180	FB	3588	-398	28	70
181	FB	3634	-398	28	70
182	VSSA	3680	-398	28	70
183	RESE	3726	-398	28	70
184	RESE	3772	-398	28	70
185	VSSA	3818	-398	28	70
186	GDR	3864	-398	28	70
187	GDR	3910	-398	28	70
188	GDR	3956	-398	28	70
189	GDR	4002	-398	28	70
190	GDR	4048	-398	28	70
191	GDR	4094	-398	28	70
192	GDR	4140	-398	28	70
193	GDR	4186	-398	28	70
194	VSSA	4232	-398	28	70
195	VCOM	4278	-398	28	70
196	VCOM	4324	-398	28	70
197	VCOM	4370	-398	28	70
198	VCOM	4416	-398	28	70
199	VCOM	4462	-398	28	70
200	VCOM	4508	-398	28	70
201	VCOM	4554	-398	28	70
202	VCOM	4600	-398	28	70
203	DUMMY[8]	4646	-398	28	70
204	T_EN_LSH	4540	313.5	18	75
205	T_VREF	4519	413.5	18	75
206	T_VTSEN	4498	313.5	18	75
207	T_IBIAS	4477	413.5	18	75
208	T_SAR_REF	4456	313.5	18	75
209	DUMMY[9]	4435	413.5	18	75
210	G[0]	4414	313.5	18	75
211	G[2]	4393	413.5	18	75
212	G[4]	4372	313.5	18	75
213	G[6]	4351	413.5	18	75
214	G[8]	4330	313.5	18	75
215	G[10]	4309	413.5	18	75
216	G[12]	4288	313.5	18	75
217	G[14]	4267	413.5	18	75
218	G[16]	4246	313.5	18	75
219	G[18]	4225	413.5	18	75
220	G[20]	4204	313.5	18	75
221	G[22]	4183	413.5	18	75
222	G[24]	4162	313.5	18	75
223	G[26]	4141	413.5	18	75
224	G[28]	4120	313.5	18	75
225	G[30]	4099	413.5	18	75
226	G[32]	4078	313.5	18	75
227	G[34]	4057	413.5	18	75
228	G[36]	4036	313.5	18	75
229	G[38]	4015	413.5	18	75
230	G[40]	3994	313.5	18	75
231	G[42]	3973	413.5	18	75
232	G[44]	3952	313.5	18	75
233	G[46]	3931	413.5	18	75
234	G[48]	3910	313.5	18	75
235	G[50]	3889	413.5	18	75
236	G[52]	3868	313.5	18	75

No.	Name	X-axis	Y-axis	W	H
237	G[54]	3847	413.5	18	75
238	G[56]	3826	313.5	18	75
239	G[58]	3805	413.5	18	75
240	G[60]	3784	313.5	18	75
241	G[62]	3763	413.5	18	75
242	G[64]	3742	313.5	18	75
243	G[66]	3721	413.5	18	75
244	G[68]	3700	313.5	18	75
245	G[70]	3679	413.5	18	75
246	G[72]	3658	313.5	18	75
247	G[74]	3637	413.5	18	75
248	G[76]	3616	313.5	18	75
249	G[78]	3595	413.5	18	75
250	G[80]	3574	313.5	18	75
251	G[82]	3553	413.5	18	75
252	G[84]	3532	313.5	18	75
253	G[86]	3511	413.5	18	75
254	G[88]	3490	313.5	18	75
255	G[90]	3469	413.5	18	75
256	G[92]	3448	313.5	18	75
257	G[94]	3427	413.5	18	75
258	G[96]	3406	313.5	18	75
259	G[98]	3385	413.5	18	75
260	G[100]	3364	313.5	18	75
261	G[102]	3343	413.5	18	75
262	G[104]	3322	313.5	18	75
263	G[106]	3301	413.5	18	75
264	G[108]	3280	313.5	18	75
265	G[110]	3259	413.5	18	75
266	G[112]	3238	313.5	18	75
267	G[114]	3217	413.5	18	75
268	G[116]	3196	313.5	18	75
269	G[118]	3175	413.5	18	75
270	G[120]	3154	313.5	18	75
271	G[122]	3133	413.5	18	75
272	G[124]	3112	313.5	18	75
273	G[126]	3091	413.5	18	75
274	G[128]	3070	313.5	18	75
275	G[130]	3049	413.5	18	75
276	G[132]	3028	313.5	18	75
277	G[134]	3007	413.5	18	75
278	G[136]	2986	313.5	18	75
279	G[138]	2965	413.5	18	75
280	G[140]	2944	313.5	18	75
281	G[142]	2923	413.5	18	75
282	G[144]	2902	313.5	18	75
283	G[146]	2881	413.5	18	75
284	G[148]	2860	313.5	18	75
285	G[150]	2839	413.5	18	75
286	G[152]	2818	313.5	18	75
287	G[154]	2797	413.5	18	75
288	G[156]	2776	313.5	18	75
289	G[158]	2755	413.5	18	75
290	G[160]	2734	313.5	18	75
291	G[162]	2713	413.5	18	75
292	G[164]	2692	313.5	18	75
293	G[166]	2671	413.5	18	75
294	G[168]	2650	313.5	18	75
295	G[170]	2629	413.5	18	75
296	G[172]	2608	313.5	18	75

No.	Name	X-axis	Y-axis	W	H
297	G[174]	2587	413.5	18	75
298	G[176]	2566	313.5	18	75
299	G[178]	2545	413.5	18	75
300	G[180]	2524	313.5	18	75
301	G[182]	2503	413.5	18	75
302	G[184]	2482	313.5	18	75
303	G[186]	2461	413.5	18	75
304	G[188]	2440	313.5	18	75
305	G[190]	2419	413.5	18	75
306	G[192]	2398	313.5	18	75
307	G[194]	2377	413.5	18	75
308	G[196]	2356	313.5	18	75
309	G[198]	2335	413.5	18	75
310	G[200]	2314	313.5	18	75
311	G[202]	2293	413.5	18	75
312	G[204]	2272	313.5	18	75
313	G[206]	2251	413.5	18	75
314	G[208]	2230	313.5	18	75
315	G[210]	2209	413.5	18	75
316	G[212]	2188	313.5	18	75
317	G[214]	2167	413.5	18	75
318	G[216]	2146	313.5	18	75
319	G[218]	2125	413.5	18	75
320	G[220]	2104	313.5	18	75
321	G[222]	2083	413.5	18	75
322	G[224]	2062	313.5	18	75
323	G[226]	2041	413.5	18	75
324	G[228]	2020	313.5	18	75
325	G[230]	1999	413.5	18	75
326	G[232]	1978	313.5	18	75
327	G[234]	1957	413.5	18	75
328	G[236]	1936	313.5	18	75
329	G[238]	1915	413.5	18	75
330	G[240]	1894	313.5	18	75
331	G[242]	1873	413.5	18	75
332	G[244]	1852	313.5	18	75
333	G[246]	1831	413.5	18	75
334	G[248]	1810	313.5	18	75
335	G[250]	1789	413.5	18	75
336	G[252]	1768	313.5	18	75
337	G[254]	1747	413.5	18	75
338	G[256]	1726	313.5	18	75
339	G[258]	1705	413.5	18	75
340	G[260]	1684	313.5	18	75
341	G[262]	1663	413.5	18	75
342	G[264]	1642	313.5	18	75
343	G[266]	1621	413.5	18	75
344	G[268]	1600	313.5	18	75
345	G[270]	1579	413.5	18	75
346	G[272]	1558	313.5	18	75
347	G[274]	1537	413.5	18	75
348	G[276]	1516	313.5	18	75
349	G[278]	1495	413.5	18	75
350	G[280]	1474	313.5	18	75
351	G[282]	1453	413.5	18	75
352	G[284]	1432	313.5	18	75
353	G[286]	1411	413.5	18	75
354	G[288]	1390	313.5	18	75
355	G[290]	1369	413.5	18	75
356	G[292]	1348	313.5	18	75

No.	Name	X-axis	Y-axis	W	H
357	G[294]	1327	413.5	18	75
358	DUMMY[11]	1306	313.5	18	75
359	DUMMY[10]	1285	413.5	18	75
360	VBD[3]	1176.5	420	12	100
361	S_ADDS[0]	1150.5	420	12	100
362	S_ADDS[1]	1137.5	301	12	100
363	S_ADDS[2]	1124.5	420	12	100
364	S_ADDS[3]	1111.5	301	12	100
365	S_ADDS[4]	1098.5	420	12	100
366	S_ADDS[5]	1085.5	301	12	100
367	S_ADDS[6]	1072.5	420	12	100
368	S_ADDS[7]	1059.5	301	12	100
369	VBD[1]	1046.5	420	12	100
370	S[0]	1033.5	301	12	100
371	S[1]	1020.5	420	12	100
372	S[2]	1007.5	301	12	100
373	S[3]	994.5	420	12	100
374	S[4]	981.5	301	12	100
375	S[5]	968.5	420	12	100
376	S[6]	955.5	301	12	100
377	S[7]	942.5	420	12	100
378	S[8]	929.5	301	12	100
379	S[9]	916.5	420	12	100
380	S[10]	903.5	301	12	100
381	S[11]	890.5	420	12	100
382	S[12]	877.5	301	12	100
383	S[13]	864.5	420	12	100
384	S[14]	851.5	301	12	100
385	S[15]	838.5	420	12	100
386	S[16]	825.5	301	12	100
387	S[17]	812.5	420	12	100
388	S[18]	799.5	301	12	100
389	S[19]	786.5	420	12	100
390	S[20]	773.5	301	12	100
391	S[21]	760.5	420	12	100
392	S[22]	747.5	301	12	100
393	S[23]	734.5	420	12	100
394	S[24]	721.5	301	12	100
395	S[25]	708.5	420	12	100
396	S[26]	695.5	301	12	100
397	S[27]	682.5	420	12	100
398	S[28]	669.5	301	12	100
399	S[29]	656.5	420	12	100
400	S[30]	643.5	301	12	100
401	S[31]	630.5	420	12	100
402	S[32]	617.5	301	12	100
403	S[33]	604.5	420	12	100
404	S[34]	591.5	301	12	100
405	S[35]	578.5	420	12	100
406	S[36]	565.5	301	12	100
407	S[37]	552.5	420	12	100
408	S[38]	539.5	301	12	100
409	S[39]	526.5	420	12	100
410	S[40]	513.5	301	12	100
411	S[41]	500.5	420	12	100
412	S[42]	487.5	301	12	100
413	S[43]	474.5	420	12	100
414	S[44]	461.5	301	12	100
415	S[45]	448.5	420	12	100
416	S[46]	435.5	301	12	100
417	S[47]	422.5	420	12	100
418	S[48]	409.5	301	12	100
419	S[49]	396.5	420	12	100
420	S[50]	383.5	301	12	100
421	S[51]	370.5	420	12	100
422	S[52]	357.5	301	12	100
423	S[53]	344.5	420	12	100
424	S[54]	331.5	301	12	100
425	S[55]	318.5	420	12	100
426	S[56]	305.5	301	12	100
427	S[57]	292.5	420	12	100
428	S[58]	279.5	301	12	100
429	S[59]	266.5	420	12	100
430	S[60]	253.5	301	12	100
431	S[61]	240.5	420	12	100
432	S[62]	227.5	301	12	100
433	S[63]	214.5	420	12	100
434	S[64]	201.5	301	12	100
435	S[65]	188.5	420	12	100
436	S[66]	175.5	301	12	100
437	S[67]	162.5	420	12	100
438	S[68]	149.5	301	12	100
439	S[69]	136.5	420	12	100
440	S[70]	123.5	301	12	100
441	S[71]	110.5	420	12	100
442	S[72]	97.5	301	12	100
443	S[73]	84.5	420	12	100
444	S[74]	71.5	301	12	100
445	S[75]	58.5	420	12	100
446	S[76]	45.5	301	12	100
447	S[77]	32.5	420	12	100
448	S[78]	19.5	301	12	100
449	S[79]	6.5	420	12	100
450	S[80]	-6.5	301	12	100
451	S[81]	-19.5	420	12	100
452	S[82]	-32.5	301	12	100
453	S[83]	-45.5	420	12	100
454	S[84]	-58.5	301	12	100
455	S[85]	-71.5	420	12	100
456	S[86]	-84.5	301	12	100
457	S[87]	-97.5	420	12	100
458	S[88]	-110.5	301	12	100
459	S[89]	-123.5	420	12	100
460	S[90]	-136.5	301	12	100
461	S[91]	-149.5	420	12	100
462	S[92]	-162.5	301	12	100
463	S[93]	-175.5	420	12	100
464	S[94]	-188.5	301	12	100
465	S[95]	-201.5	420	12	100
466	S[96]	-214.5	301	12	100
467	S[97]	-227.5	420	12	100
468	S[98]	-240.5	301	12	100
469	S[99]	-253.5	420	12	100
470	S[100]	-266.5	301	12	100
471	S[101]	-279.5	420	12	100
472	S[102]	-292.5	301	12	100
473	S[103]	-305.5	420	12	100
474	S[104]	-318.5	301	12	100
475	S[105]	-331.5	420	12	100
476	S[106]	-344.5	301	12	100

No.	Name	X-axis	Y-axis	W	H
477	S[107]	-357.5	420	12	100
478	S[108]	-370.5	301	12	100
479	S[109]	-383.5	420	12	100
480	S[110]	-396.5	301	12	100
481	S[111]	-409.5	420	12	100
482	S[112]	-422.5	301	12	100
483	S[113]	-435.5	420	12	100
484	S[114]	-448.5	301	12	100
485	S[115]	-461.5	420	12	100
486	S[116]	-474.5	301	12	100
487	S[117]	-487.5	420	12	100
488	S[118]	-500.5	301	12	100
489	S[119]	-513.5	420	12	100
490	S[120]	-526.5	301	12	100
491	S[121]	-539.5	420	12	100
492	S[122]	-552.5	301	12	100
493	S[123]	-565.5	420	12	100
494	S[124]	-578.5	301	12	100
495	S[125]	-591.5	420	12	100
496	S[126]	-604.5	301	12	100
497	S[127]	-617.5	420	12	100
498	S[128]	-630.5	301	12	100
499	S[129]	-643.5	420	12	100
500	S[130]	-656.5	301	12	100
501	S[131]	-669.5	420	12	100
502	S[132]	-682.5	301	12	100
503	S[133]	-695.5	420	12	100
504	S[134]	-708.5	301	12	100
505	S[135]	-721.5	420	12	100
506	S[136]	-734.5	301	12	100
507	S[137]	-747.5	420	12	100
508	S[138]	-760.5	301	12	100
509	S[139]	-773.5	420	12	100
510	S[140]	-786.5	301	12	100
511	S[141]	-799.5	420	12	100
512	S[142]	-812.5	301	12	100
513	S[143]	-825.5	420	12	100
514	S[144]	-838.5	301	12	100
515	S[145]	-851.5	420	12	100
516	S[146]	-864.5	301	12	100
517	S[147]	-877.5	420	12	100
518	S[148]	-890.5	301	12	100
519	S[149]	-903.5	420	12	100
520	S[150]	-916.5	301	12	100
521	S[151]	-929.5	420	12	100
522	S[152]	-942.5	301	12	100
523	S[153]	-955.5	420	12	100
524	S[154]	-968.5	301	12	100
525	S[155]	-981.5	420	12	100
526	S[156]	-994.5	301	12	100
527	S[157]	-1007.5	420	12	100
528	S[158]	-1020.5	301	12	100
529	S[159]	-1033.5	420	12	100
530	VBD[2]	-1046.5	301	12	100
531	S_ADDE[0]	-1059.5	420	12	100
532	S_ADDE[1]	-1072.5	301	12	100
533	S_ADDE[2]	-1085.5	420	12	100
534	S_ADDE[3]	-1098.5	301	12	100
535	S_ADDE[4]	-1111.5	420	12	100
536	S_ADDE[5]	-1124.5	301	12	100

No.	Name	X-axis	Y-axis	W	H
537	S_ADDE[6]	-1137.5	420	12	100
538	S_ADDE[7]	-1150.5	301	12	100
539	VBD[4]	-1176.5	301	12	100
540	DUMMY[12]	-1285	313.5	18	75
541	DUMMY[13]	-1306	413.5	18	75
542	G[295]	-1327	313.5	18	75
543	G[293]	-1348	413.5	18	75
544	G[291]	-1369	313.5	18	75
545	G[289]	-1390	413.5	18	75
546	G[287]	-1411	313.5	18	75
547	G[285]	-1432	413.5	18	75
548	G[283]	-1453	313.5	18	75
549	G[281]	-1474	413.5	18	75
550	G[279]	-1495	313.5	18	75
551	G[277]	-1516	413.5	18	75
552	G[275]	-1537	313.5	18	75
553	G[273]	-1558	413.5	18	75
554	G[271]	-1579	313.5	18	75
555	G[269]	-1600	413.5	18	75
556	G[267]	-1621	313.5	18	75
557	G[265]	-1642	413.5	18	75
558	G[263]	-1663	313.5	18	75
559	G[261]	-1684	413.5	18	75
560	G[259]	-1705	313.5	18	75
561	G[257]	-1726	413.5	18	75
562	G[255]	-1747	313.5	18	75
563	G[253]	-1768	413.5	18	75
564	G[251]	-1789	313.5	18	75
565	G[249]	-1810	413.5	18	75
566	G[247]	-1831	313.5	18	75
567	G[245]	-1852	413.5	18	75
568	G[243]	-1873	313.5	18	75
569	G[241]	-1894	413.5	18	75
570	G[239]	-1915	313.5	18	75
571	G[237]	-1936	413.5	18	75
572	G[235]	-1957	313.5	18	75
573	G[233]	-1978	413.5	18	75
574	G[231]	-1999	313.5	18	75
575	G[229]	-2020	413.5	18	75
576	G[227]	-2041	313.5	18	75
577	G[225]	-2062	413.5	18	75
578	G[223]	-2083	313.5	18	75
579	G[221]	-2104	413.5	18	75
580	G[219]	-2125	313.5	18	75
581	G[217]	-2146	413.5	18	75
582	G[215]	-2167	313.5	18	75
583	G[213]	-2188	413.5	18	75
584	G[211]	-2209	313.5	18	75
585	G[209]	-2230	413.5	18	75
586	G[207]	-2251	313.5	18	75
587	G[205]	-2272	413.5	18	75
588	G[203]	-2293	313.5	18	75
589	G[201]	-2314	413.5	18	75
590	G[199]	-2335	313.5	18	75
591	G[197]	-2356	413.5	18	75
592	G[195]	-2377	313.5	18	75
593	G[193]	-2398	413.5	18	75
594	G[191]	-2419	313.5	18	75
595	G[189]	-2440	413.5	18	75
596	G[187]	-2461	313.5	18	75

No.	Name	X-axis	Y-axis	W	H
597	G[185]	-2482	413.5	18	75
598	G[183]	-2503	313.5	18	75
599	G[181]	-2524	413.5	18	75
600	G[179]	-2545	313.5	18	75
601	G[177]	-2566	413.5	18	75
602	G[175]	-2587	313.5	18	75
603	G[173]	-2608	413.5	18	75
604	G[171]	-2629	313.5	18	75
605	G[169]	-2650	413.5	18	75
606	G[167]	-2671	313.5	18	75
607	G[165]	-2692	413.5	18	75
608	G[163]	-2713	313.5	18	75
609	G[161]	-2734	413.5	18	75
610	G[159]	-2755	313.5	18	75
611	G[157]	-2776	413.5	18	75
612	G[155]	-2797	313.5	18	75
613	G[153]	-2818	413.5	18	75
614	G[151]	-2839	313.5	18	75
615	G[149]	-2860	413.5	18	75
616	G[147]	-2881	313.5	18	75
617	G[145]	-2902	413.5	18	75
618	G[143]	-2923	313.5	18	75
619	G[141]	-2944	413.5	18	75
620	G[139]	-2965	313.5	18	75
621	G[137]	-2986	413.5	18	75
622	G[135]	-3007	313.5	18	75
623	G[133]	-3028	413.5	18	75
624	G[131]	-3049	313.5	18	75
625	G[129]	-3070	413.5	18	75
626	G[127]	-3091	313.5	18	75
627	G[125]	-3112	413.5	18	75
628	G[123]	-3133	313.5	18	75
629	G[121]	-3154	413.5	18	75
630	G[119]	-3175	313.5	18	75
631	G[117]	-3196	413.5	18	75
632	G[115]	-3217	313.5	18	75
633	G[113]	-3238	413.5	18	75
634	G[111]	-3259	313.5	18	75
635	G[109]	-3280	413.5	18	75
636	G[107]	-3301	313.5	18	75
637	G[105]	-3322	413.5	18	75
638	G[103]	-3343	313.5	18	75
639	G[101]	-3364	413.5	18	75
640	G[99]	-3385	313.5	18	75
641	G[97]	-3406	413.5	18	75
642	G[95]	-3427	313.5	18	75
643	G[93]	-3448	413.5	18	75
644	G[91]	-3469	313.5	18	75
645	G[89]	-3490	413.5	18	75
646	G[87]	-3511	313.5	18	75

No.	Name	X-axis	Y-axis	W	H
647	G[85]	-3532	413.5	18	75
648	G[83]	-3553	313.5	18	75
649	G[81]	-3574	413.5	18	75
650	G[79]	-3595	313.5	18	75
651	G[77]	-3616	413.5	18	75
652	G[75]	-3637	313.5	18	75
653	G[73]	-3658	413.5	18	75
654	G[71]	-3679	313.5	18	75
655	G[69]	-3700	413.5	18	75
656	G[67]	-3721	313.5	18	75
657	G[65]	-3742	413.5	18	75
658	G[63]	-3763	313.5	18	75
659	G[61]	-3784	413.5	18	75
660	G[59]	-3805	313.5	18	75
661	G[57]	-3826	413.5	18	75
662	G[55]	-3847	313.5	18	75
663	G[53]	-3868	413.5	18	75
664	G[51]	-3889	313.5	18	75
665	G[49]	-3910	413.5	18	75
666	G[47]	-3931	313.5	18	75
667	G[45]	-3952	413.5	18	75
668	G[43]	-3973	313.5	18	75
669	G[41]	-3994	413.5	18	75
670	G[39]	-4015	313.5	18	75
671	G[37]	-4036	413.5	18	75
672	G[35]	-4057	313.5	18	75
673	G[33]	-4078	413.5	18	75
674	G[31]	-4099	313.5	18	75
675	G[29]	-4120	413.5	18	75
676	G[27]	-4141	313.5	18	75
677	G[25]	-4162	413.5	18	75
678	G[23]	-4183	313.5	18	75
679	G[21]	-4204	413.5	18	75
680	G[19]	-4225	313.5	18	75
681	G[17]	-4246	413.5	18	75
682	G[15]	-4267	313.5	18	75
683	G[13]	-4288	413.5	18	75
684	G[11]	-4309	313.5	18	75
685	G[9]	-4330	413.5	18	75
686	G[7]	-4351	313.5	18	75
687	G[5]	-4372	413.5	18	75
688	G[3]	-4393	313.5	18	75
689	G[1]	-4414	413.5	18	75
690	T_LDON5V	-4435	313.5	18	75
691	T_LDON5V	-4456	413.5	18	75
692	T_VCOM	-4477	313.5	18	75
693	T_VCOM	-4498	413.5	18	75
694	T_N18V	-4519	313.5	18	75
695	T_N18V	-4540	413.5	18	75

13. REVISION HISTORY

Revision	Content	Page	Date
1.0.0	new issue	-	2020/09/11
1.0.1	Update VDD15 & VOTP	87	2021/04/09