ANALYSE DE PERFORMANCES BASSE CONSOMMATION DE CONTROLEURS AUTOMOBILES

END OF INTERNSHIP PRESENTATION
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Advanced Masters in Embedded Systems (2015-2016)

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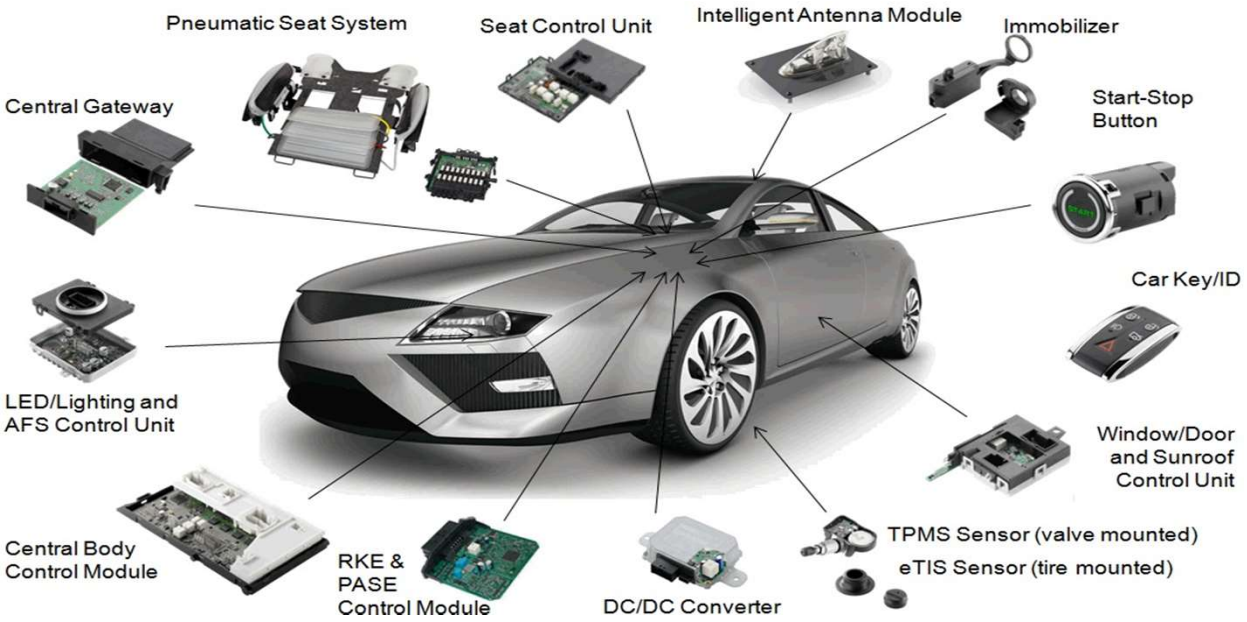
AGENDA

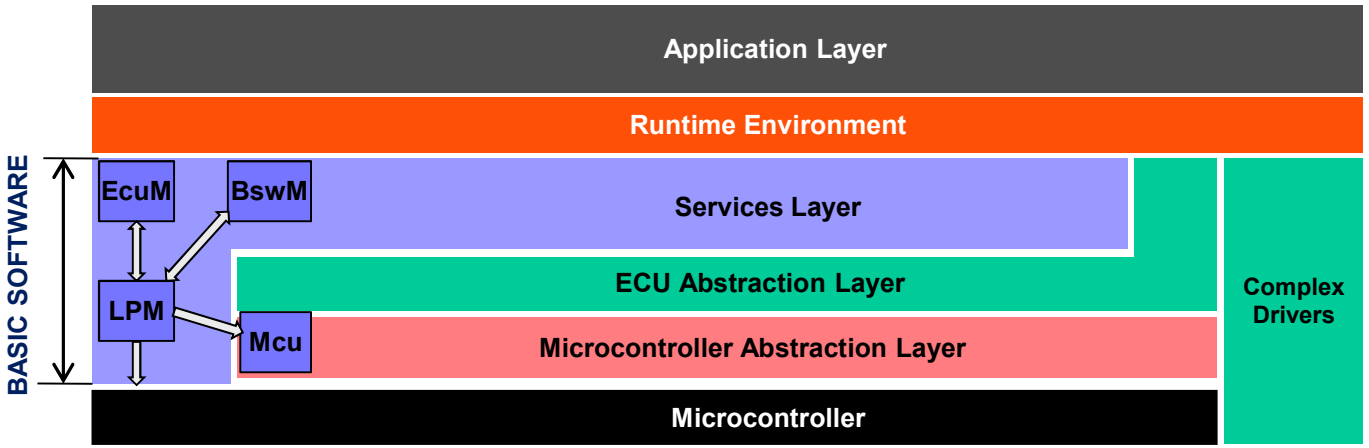
1. Project Context
2. Objective Of Internship
3. Debug Feature In Low Power
4. Dual Core Prototype Development
5. Deliverables
6. Improvements
7. Merits Obtained
8. Conclusion

TEAM ORGANIZATION



- AUTOSAR Layered Architecture

- Mode Management Team



PROJECT CONTEXT

POWER MODES - I

~150 mA

All components fully functional

(FULL) **HIGH** POWER MODE

ECU State changed

ENGINE SWITCHED OFF

ENGINE POWERED ON

Periodic LP task to be performed

~10 mA

Un-used components switched off

LOGICAL LOW POWER

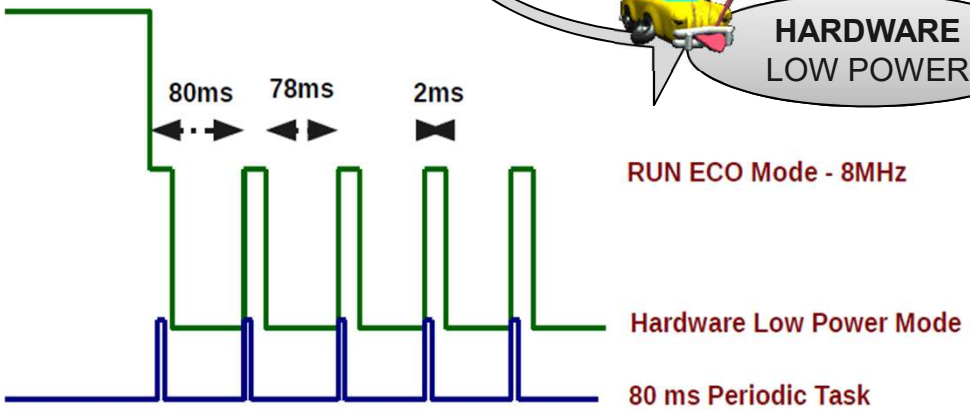
Periodic LP task to be performed or Hardware wake-up event received

LP task Completed

~600 – 100 µA

HARDWARE LOW POWER

The complete unit is stopped
(except for very few components)



OBJECTIVE OF INTERNSHIP

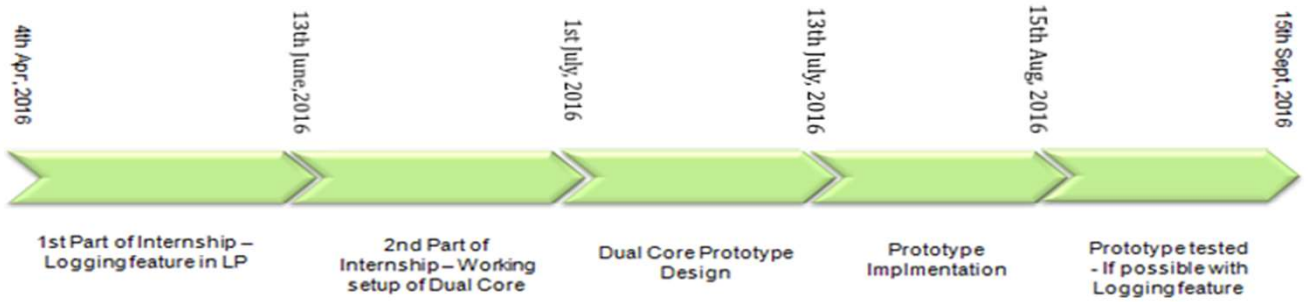
Profiling and Debugging in LPM

In a Representative Environment

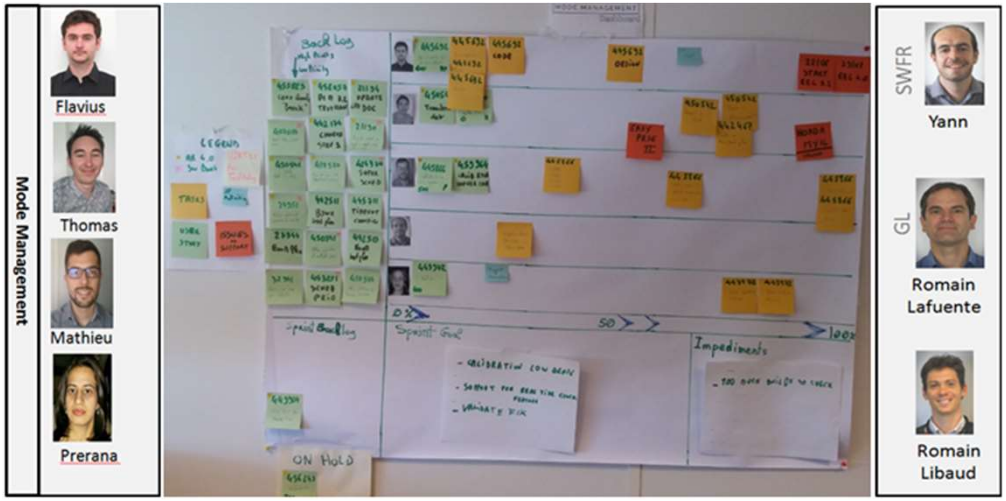
Implementation of Debug Feature in LPM

Dual Core Prototype Development

Implementation of Synchronization between two cores for entering and exiting the LPM



Process Followed - Agile Process



- Small deliverables with evolving requirements
- Features to be delivered → User Story
- Team determine the complexity and time required to deliver a user story
- User Story are broken down into task
- Frequent small stand-up meetings are conducted to be inline with the goals

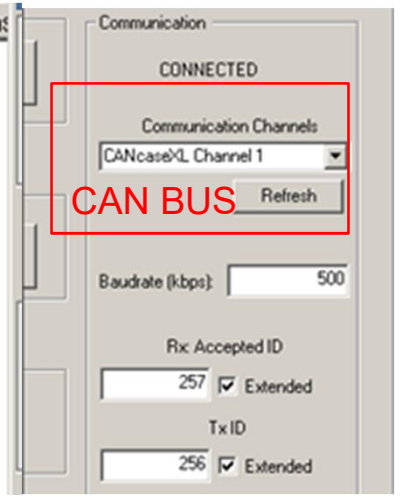
Delivered User Stories

DEBUG FEATURE IN LOW POWER

Before Implementation of this feature Logs were obtained only in High Power

Task	Activation	Interrupt	Activation	Execution Point	Activations
Task_SWP_FG2_IoHwAb_...	462			DbgF_ExecPoint_Test1	116
Task_SWP_FG1_5ms	463				
Task_SWP_FG1_IoHwAb_...	463				
Task_ASW_FG1_5ms	463				
Task_SWP_FG1_10ms	232				
Task_SWP_FG1_20ms	116				
Task_ASW_FG1_10ms	231				
Task_ASW_FG1_20ms	116				
Task_SWP_System_Idle	1379				
Task_SWP_FG1_100ms	23				
Task_ASW_FG1_100ms	23				
Task_SWP_FG1_1s	2				
Task_ASW_FG1_1s	2				

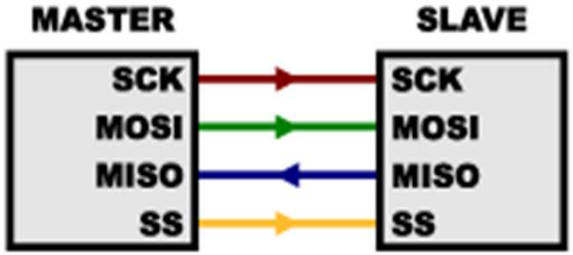
HIGH POWER TASK

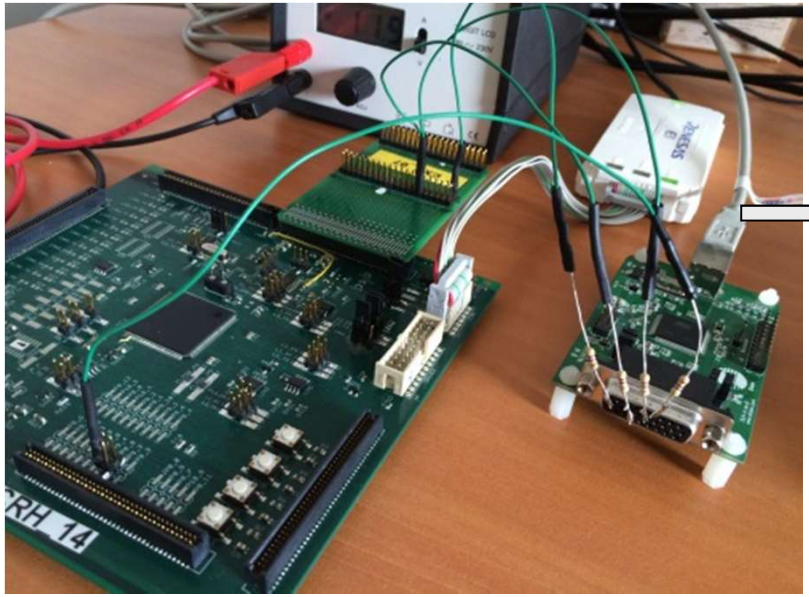


- Unavailability of this feature in LPM
  - OS is Paused → APIs used in HP can not be used in LP
  - Unavailability of communication buses in LP
  - Consumes more power

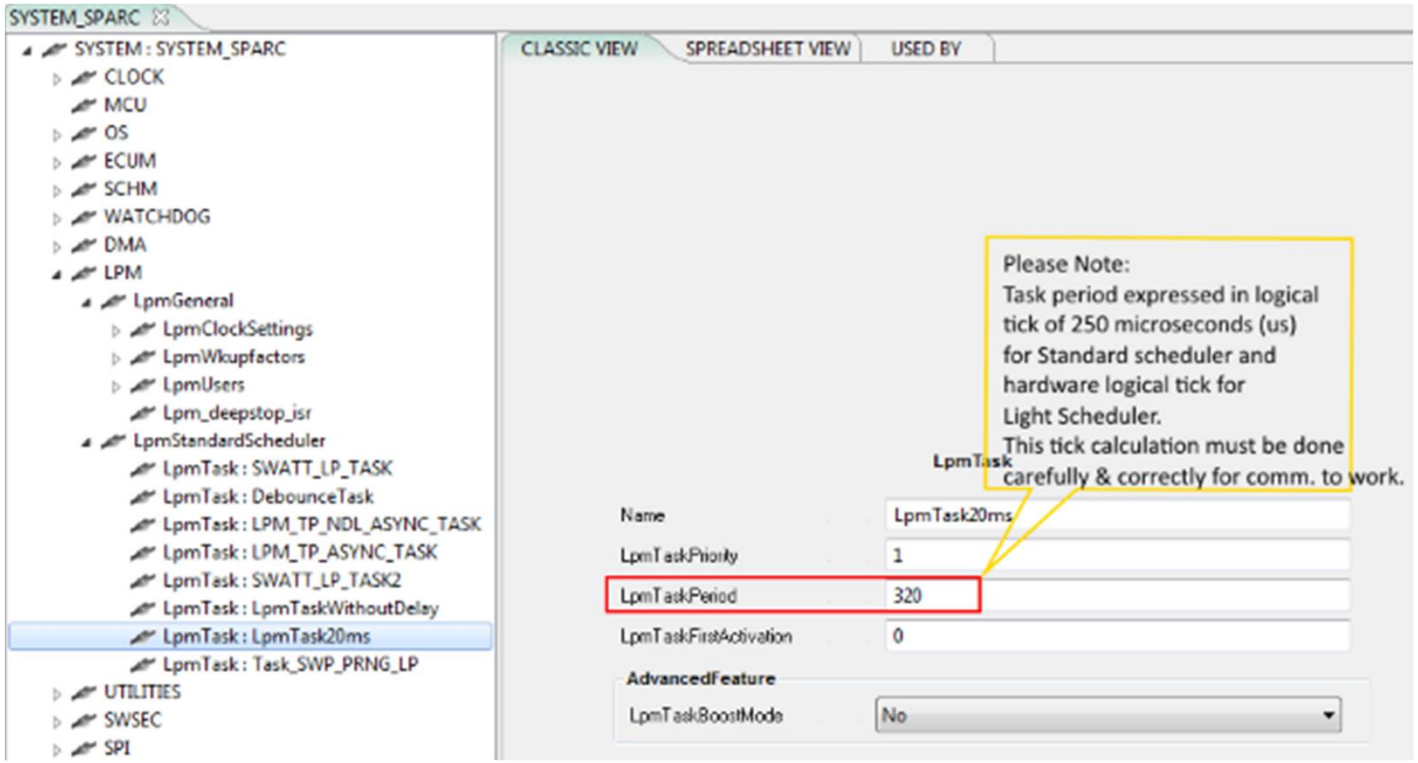
HARDWARE SETUP

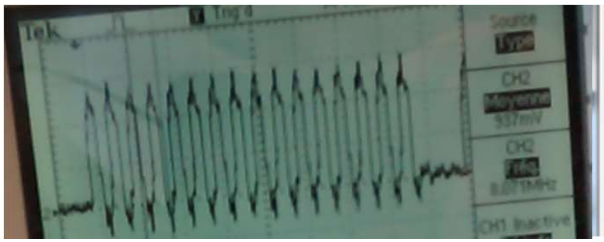
- Set-up [Master – Slave]
  - Renesas F1L: Microcontroller → Master
  - DioLAN board → Slave
  - E1 → Emulator used to flash
  - SPI communication → Light weight bus





Configuration Tools and Initial Trials





00E0 0505 0505 0517 00E0 0505 0505 0517
00E0 0505 0505 0517 00E0 0505 0505 0517
00E0 0505 0505 0517 00E0 0505 0505 0517
00E0 0505 0505 0517 00E0 0505 0505 0517
00E0 0505 0505 0517 00E0 0505 0505 0517
00E0 0505 0505 0517 00E0 0505 0505 0517
00E0 0505 0505 0517 00E0 0505 0505 0517
00E0 0505 0505 0517 00E0 0505 0505 0517
00E0 0505 0505 0517 00E0 0505 0505 0517

IMPLEMENTATION AND RESULTS

- There were 3 APIs Introduced:
  - Interrupts received
  - Resource activation and de-activation
  - Execution duration of LP Task

LOGS OBTAINED

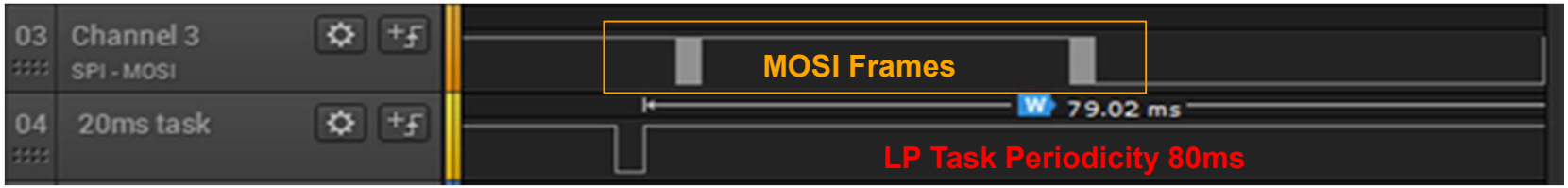
Time (in CPU Ticks)	Event Occurred (Task / ISR)	Event Details
4609	SPI_CSIH3_TIC_CAT2_ISR	START
5112	SPI_CSIH3_TIC_CAT2_ISR	STOP
35195	DBGF_EXECPOINT_TEST_32B	START
35233	LpmTask_LpmTask20ms	START
37706	DBGF_EXECPOINT_TEST_32B	STOP
37738	LpmTask_LpmTask20ms	STOP

LP TASK

Task	Avg T...	Max ...	Min Ti...	AvgP...
LpmTask20ms	2186	2740	1737	80725
LpmTaskWithoutDelay	197	545	158	80724

INT	Avg T...	Ma
Fts_IT	302	12
SPI_CSIH3_TIC_C...	562	56
Lpm_Api_Notification	61	62

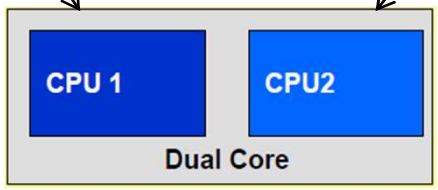
ExecP	Avg T...	Max ...	Min Ti...
DBGF_EXECPOI...	2217	2248	2162
DBGF_EXECPOI...	3019	5081	2395



DUAL CORE PROTOTYPE

BCM –
Body Control Module

PASE –
Passive Entry and Start



Renesas F1H
Microcontroller

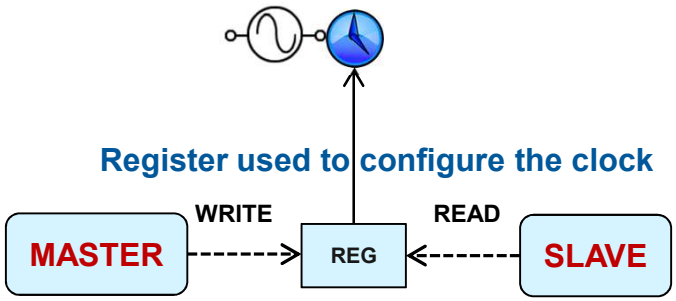
- Optimized power consumption
- Cost Effective
- To reduce the space used

Challenge: To achieve Effective Communication
To obtain synchronization for entering and exiting LPM

DESIGN GUIDELINES – MASTER SLAVE MODEL

HARDWARE CONSTRAINT

- Microcontroller has **[1]** Source Clock →
  - Master Slave Model [If Master is Off, Slave is Off]



DESIGN CONSTRAINT

- **HIGH POWER** Task executed Independently on both Cores → Idle task is executed Independently

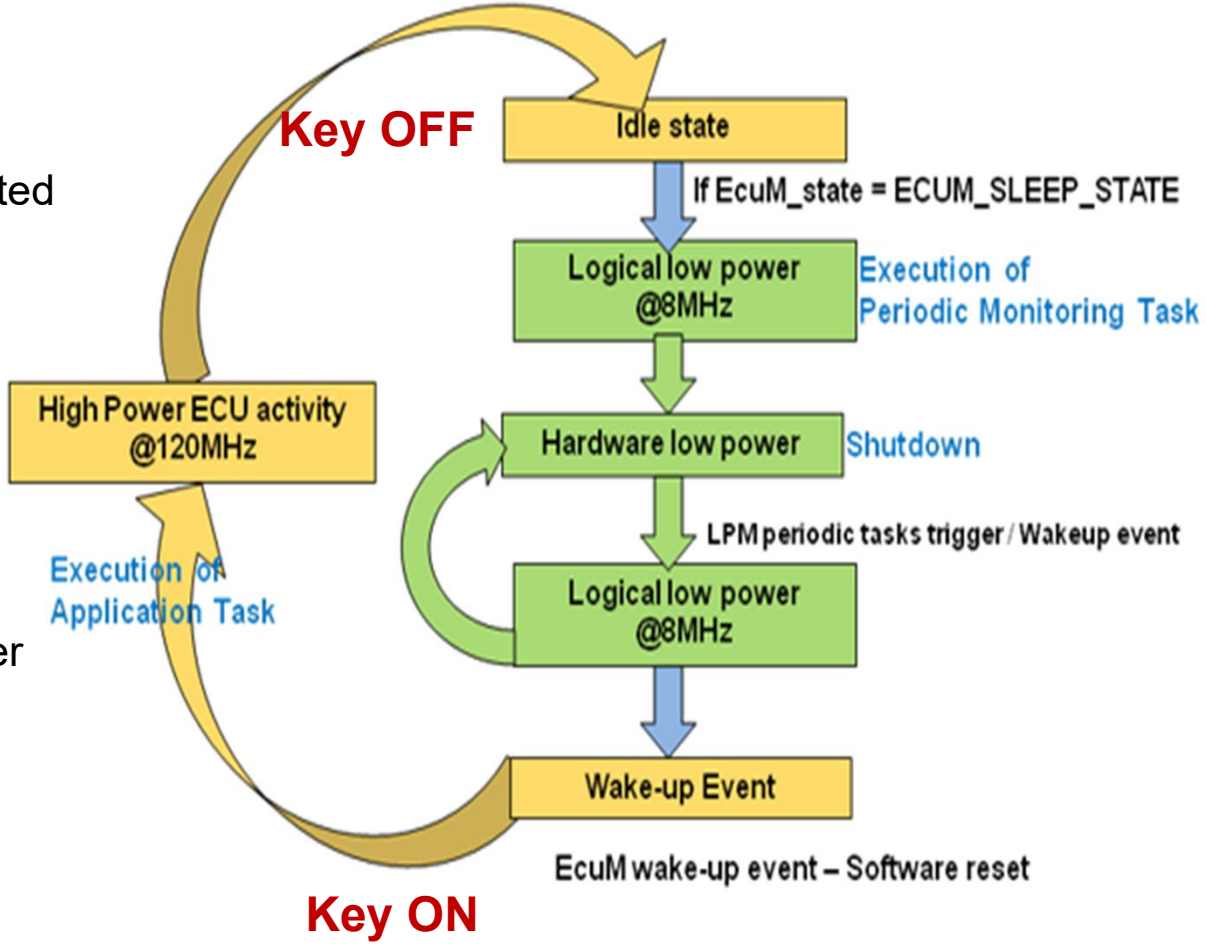
ARCHITECTURAL CONSTRAINT FROM AUTOSAR

- **[1]** Basic software module → all BSW activities are done by Master
  - **[1]** LP Module → Slave Core has no activity in LP
- **[1]** OS Counter is available → All task triggered by Master Core

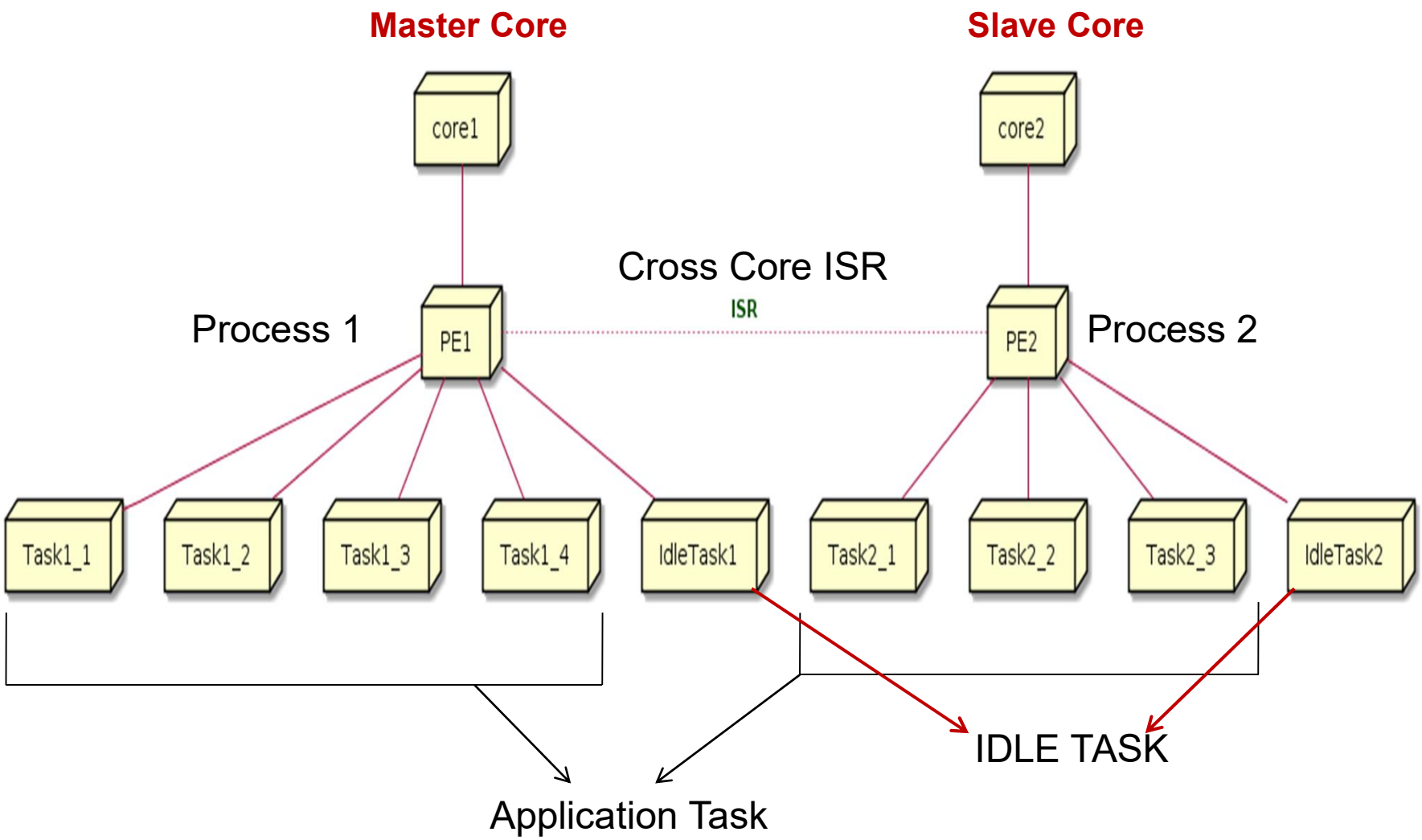
PROJECT CONTEXT

POWER MODES - II

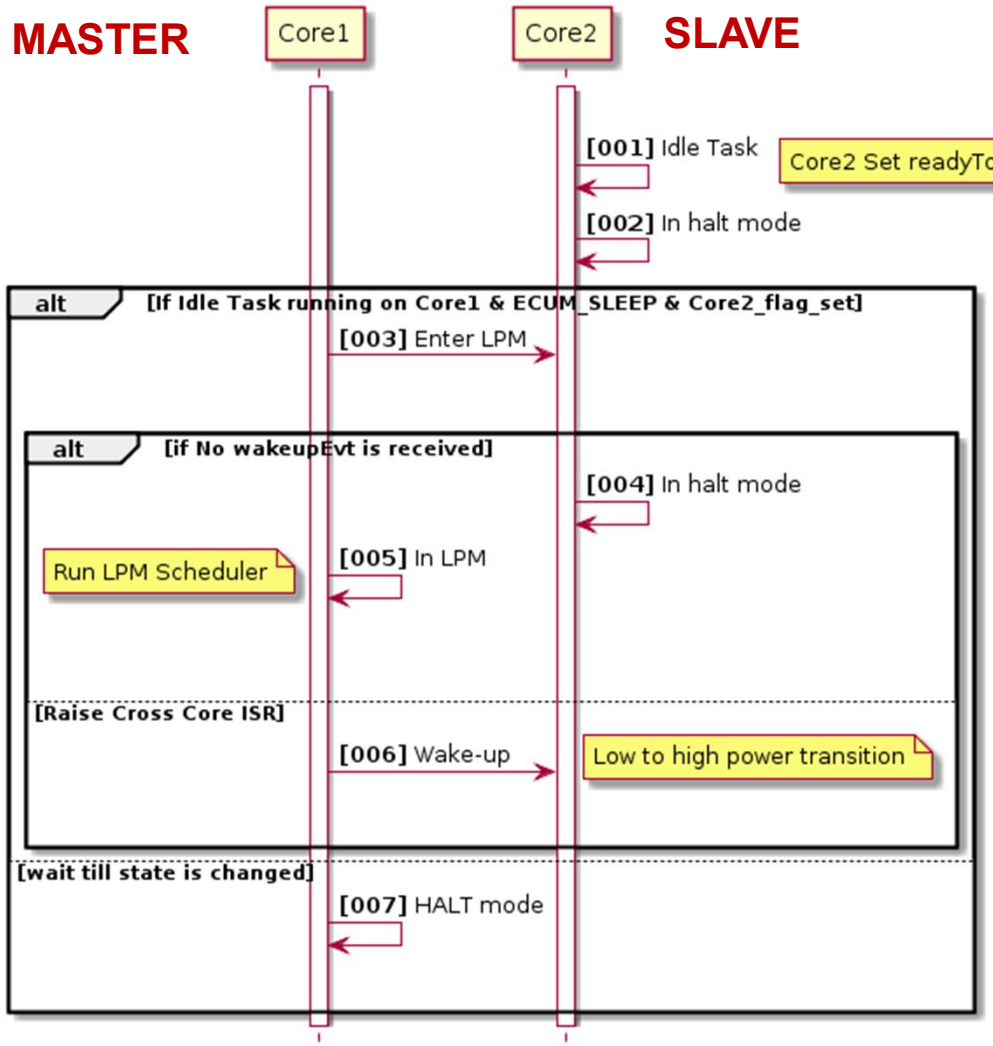
- Application Task Execute in HP
- On Key Off - Idle Task is executed
- When Ecu State = SLEEP
- Enter LP
- In LP:
- Pause OS, Start LPM Scheduler
- Start Periodic Activity in LP
- Enter Hardware Low Power
- On Key On – Enter HP



PROTOYPE HIGH LEVEL DESIGN



DETAIL DESIGN [Synchronization Mechanism]– I



❖**General Idea:**

❖Master & Slave should be in Idle Loop to enter LP

❖If Wake-up = TRUE → Master sends CrossCoreISR to Slave

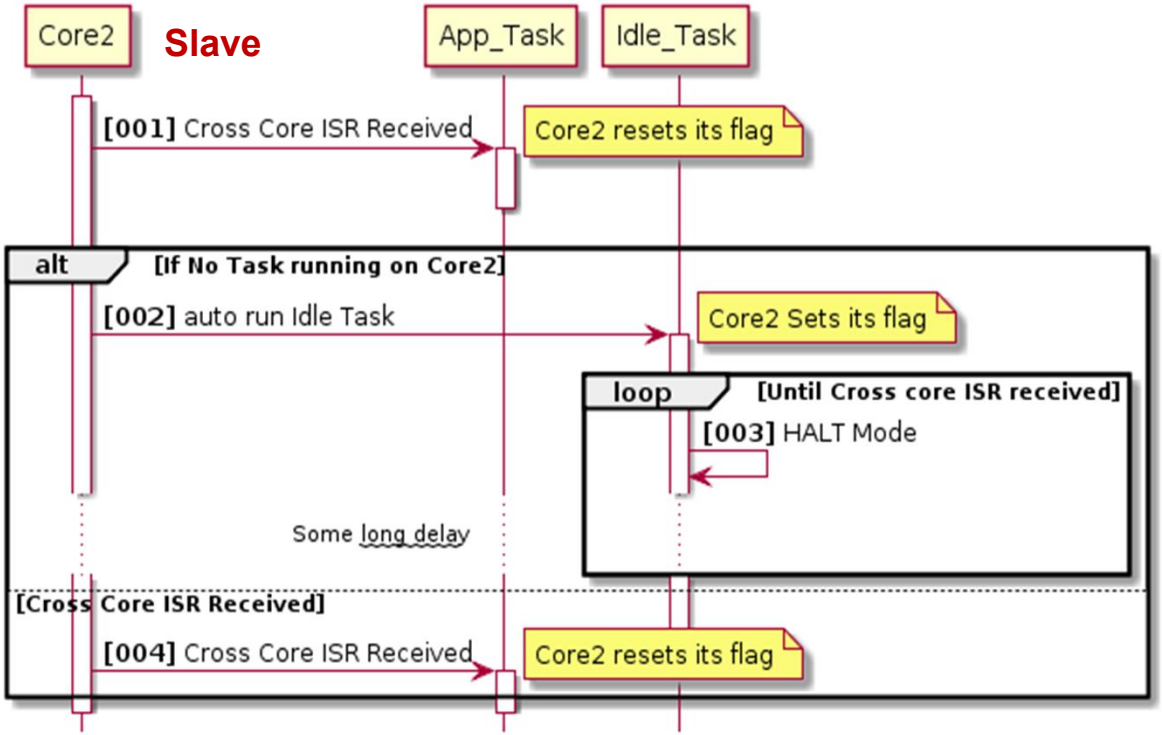
❖**Flagging Mechanism**

- In Idle Task, Slave will set a **readyToEnterIntoLowPower** flag
- Slave Core remains in HALT mode

DETAIL DESIGN [Synchronization Mechanism]– II

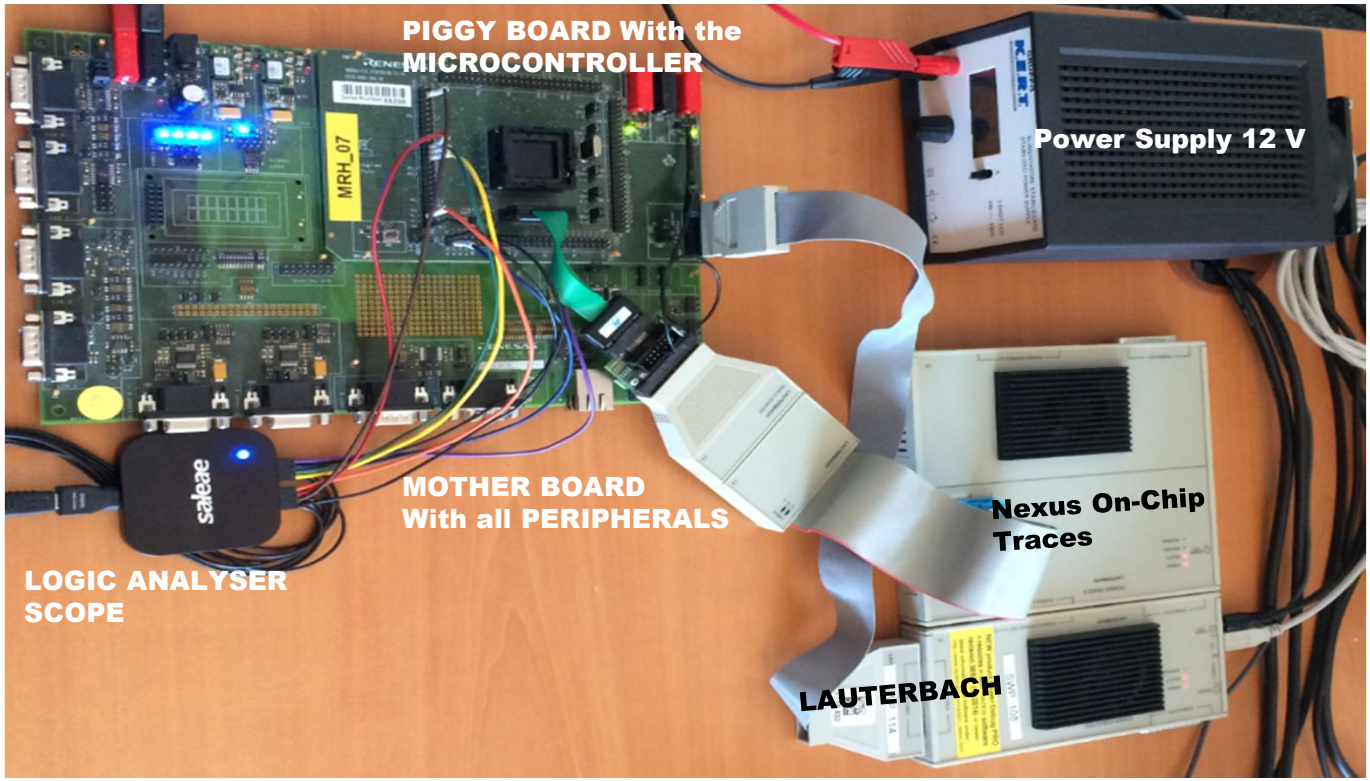
If Slave is Busy

- Reset the **readyToEnterIntoLowPower** flag in CrossCoreISR Call Back
- Execute the Application task

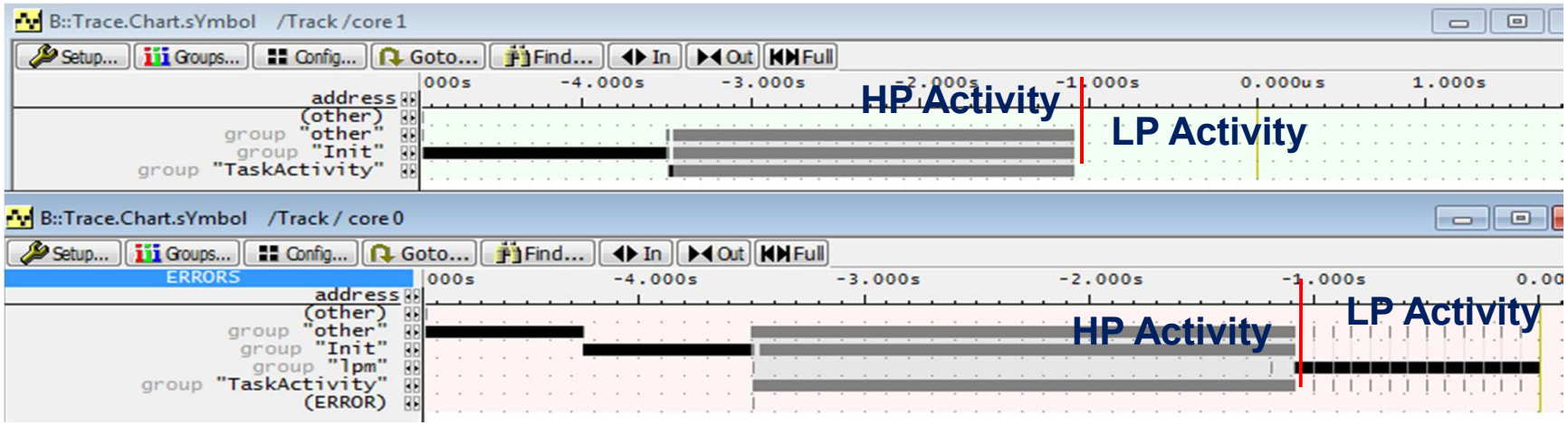


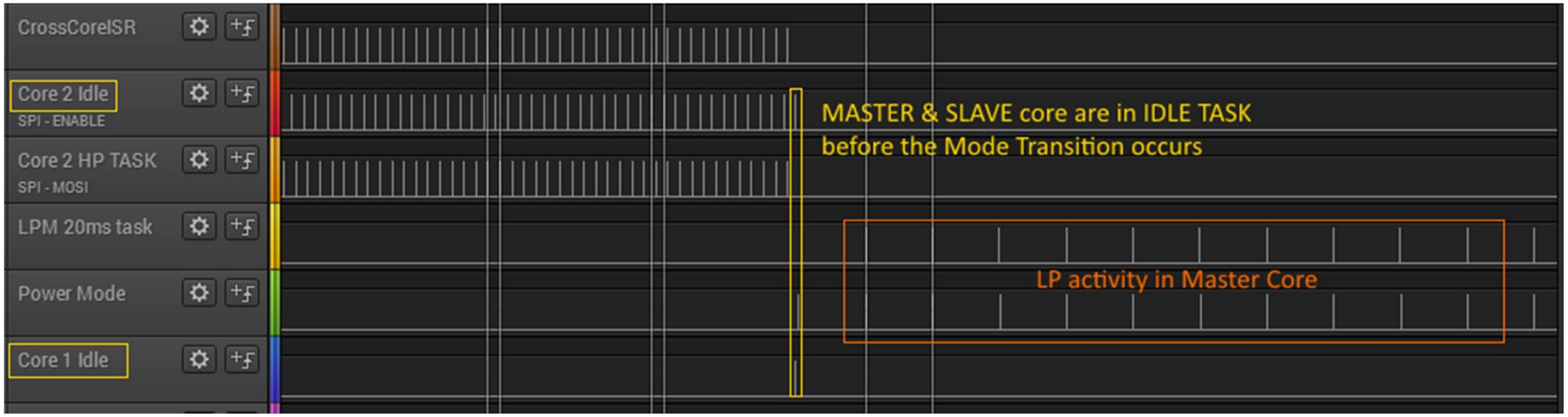
HARDWARE SET-UP & IMPLEMENTATION

- Renesas F1H Dual Microcontroller
- Lauterbach as the Emulator and Nexus debugger
- Saleae Logic Analyzer as the Scope

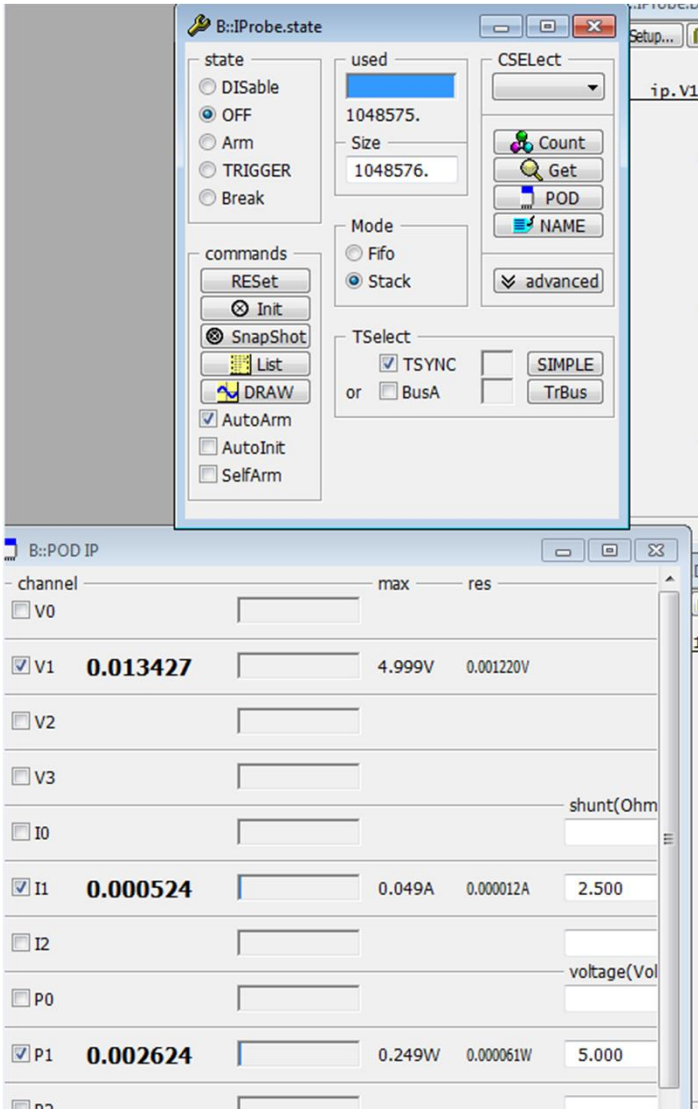


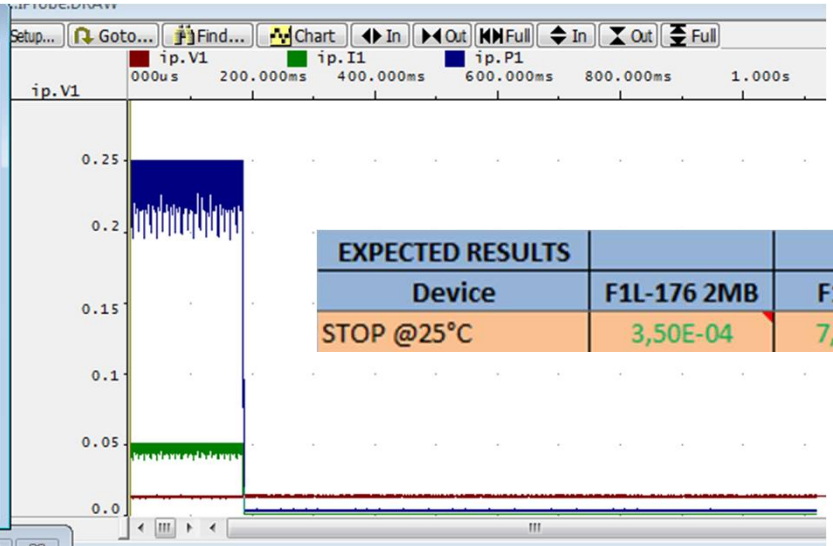
RESULTS


B::Trace.Chart.sYmbol /Track /core 1
Setup... Groups... Config... Goto... Find... In Out Full
000s -4.000s -3.000s -2.000s -1.000s 0.000us 1.000s
address
(other)
group "other"
group "Init"
group "TaskActivity"
HP Activity
LP Activity
B::Trace.Chart.sYmbol /Track / core 0
Setup... Groups... Config... Goto... Find... In Out Full
ERRORS
000s -4.000s -3.000s -2.000s -1.000s 0.00
address
(other)
group "other"
group "Init"
group "lpm"
group "TaskActivity"
(ERROR)
HP Activity
LP Activity

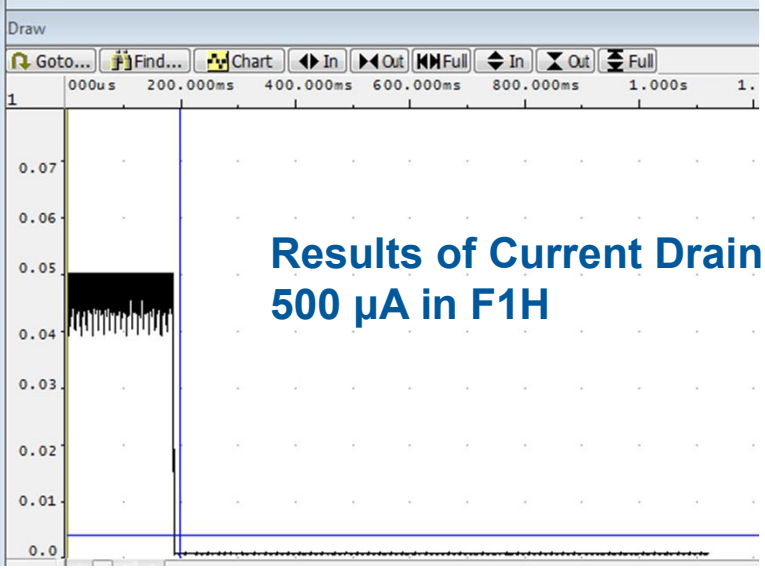

CrossCoreISR
Core 2 Idle
SPI - ENABLE
Core 2 HP TASK
SPI - MOSI
LPM 20ms task
Power Mode
Core 1 Idle
MASTER & SLAVE core are in IDLE TASK
before the Mode Transition occurs
LP activity in Master Core

Current Drain – STOP Mode



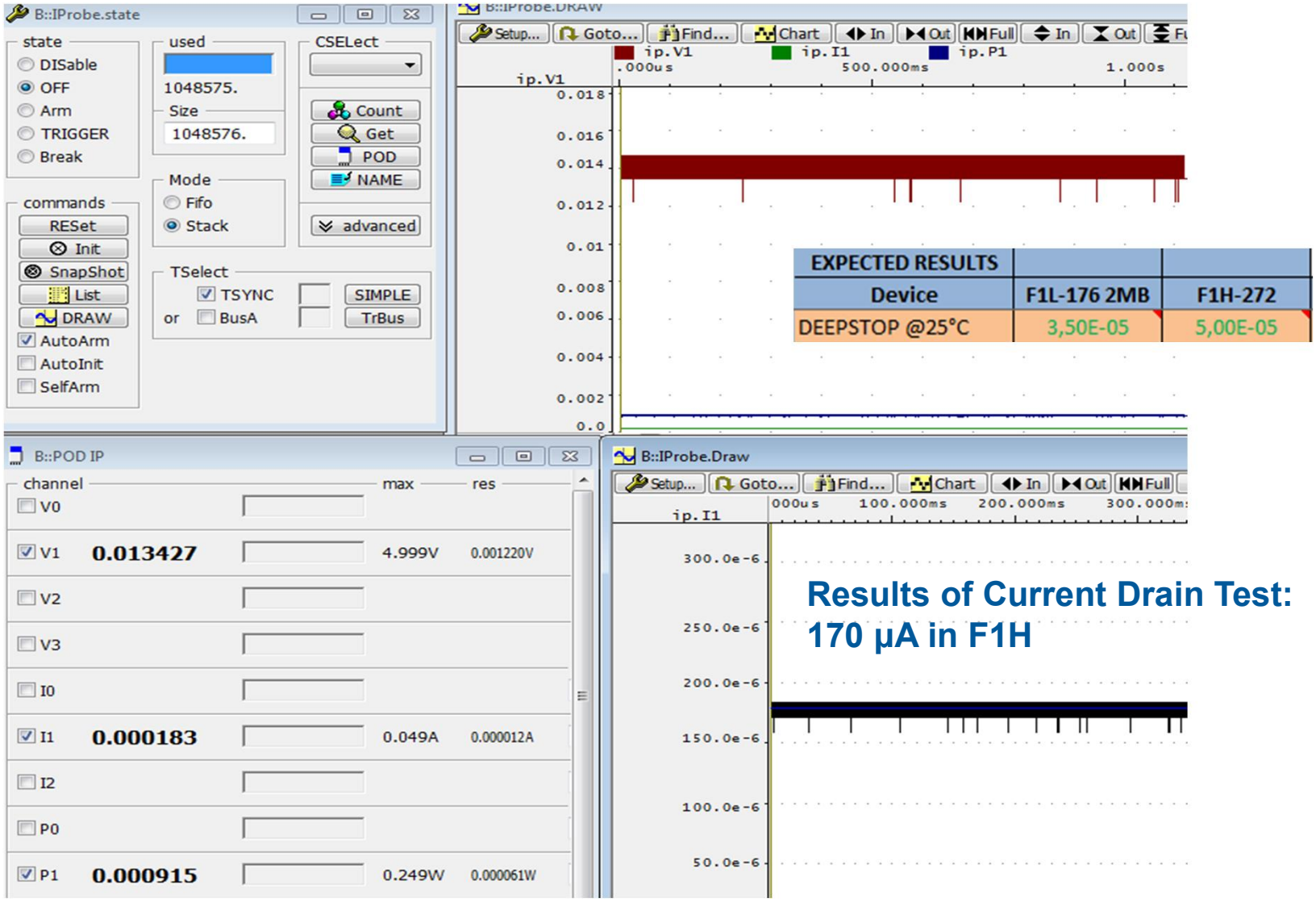


EXPECTED RESULTS		
Device	F1L-176 2MB	F1H-272
STOP @25°C	3,50E-04	7,50E-04



Results of Current Drain Test: 500 µA in F1H

Current Drain – DEEPSTOP Mode



EXPECTED RESULTS		
Device	F1L-176 2MB	F1H-272
DEEPSTOP @25°C	3,50E-05	5,00E-05

Results of Current Drain Test: 170 µA in F1H

DELIVERABLES

DEBUGGING FEATURE TO BE INTRODUCED IN LOW POWER MODE

- Implemented the code
- Tested in various Power modes
- Documented in a User Manual
- Currently the feature is being utilized by the Software Platform Team

DUAL CORE PROTOTYPE DEVELOPMENT (SYNCHRONIZATION TO BE DONE TO ENTER AND EXIT LPM)

- Implemented the code
- Tested with various design scenarios
- Documented in a Design Document and User Guide
- The feature will form the base for future implementations on customer demand

IMPROVEMENTS

- Debug Feature in LPM:
  - Calibration of the Timers
  - Test with smallest LPM Period
  - Test in different Power modes on other variants

- Dual Core Prototype Development:
  - Simulation for different possible scenarios
  - Test in different Power modes
  - To test the performance of the Dual Core system

MERITS OBTAINED

- Concept of AUTOSAR
- POWER MODES in an ECU
- Programming of Microcontrollers
- Usage of debug tools - 

LAUTERBACH DEVELOPMENT TOOLS
- Usage of Configuration tools – IMS, CESSAR-CT, SPARC
- Designing using UMLs
- Dual Core Technology
- Development process 

vs 

- Other module concepts like Bootloaders and their working

CONCLUSION

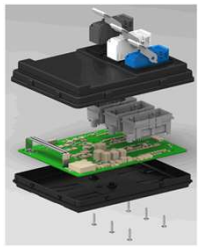
- Interesting Topics
- Proposed solution was satisfactory
- Implementation of my courses
- Confirmation of my interest in Embedded Systems
- Opportunity to work on Hardware
- To understand and work in different cultural environment

Questions

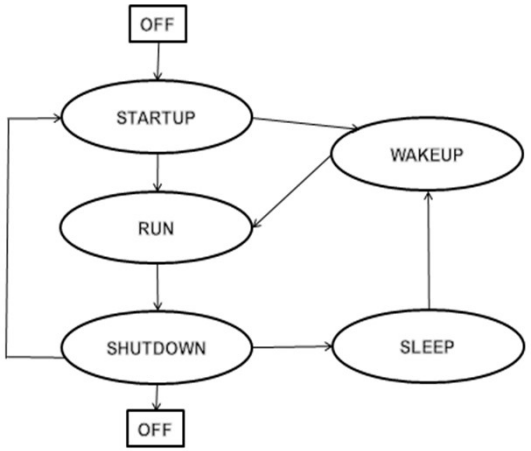
THANK YOU

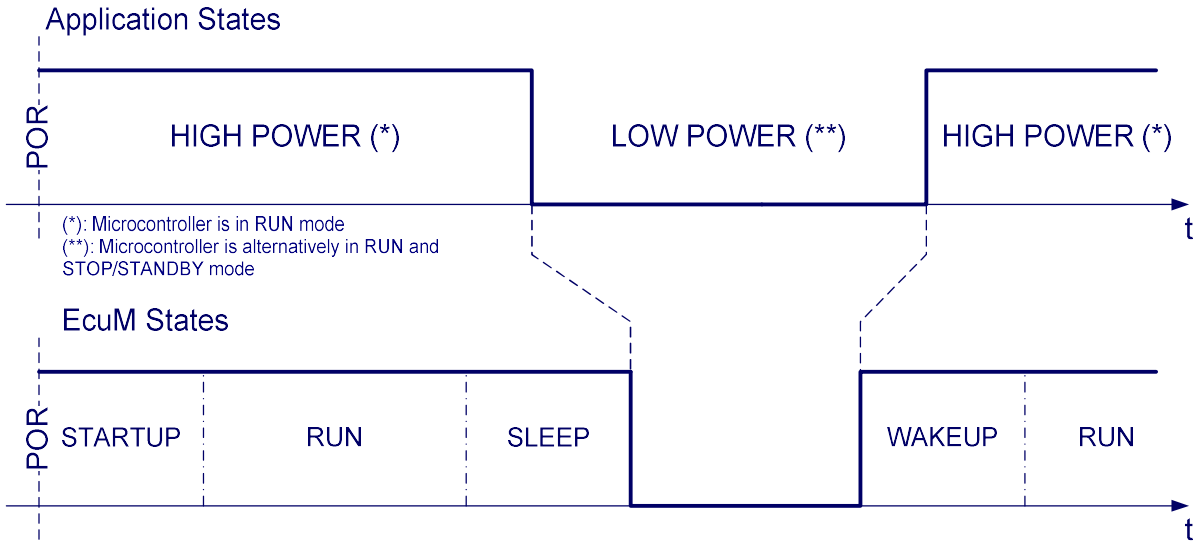
Modes of Operation

BCM

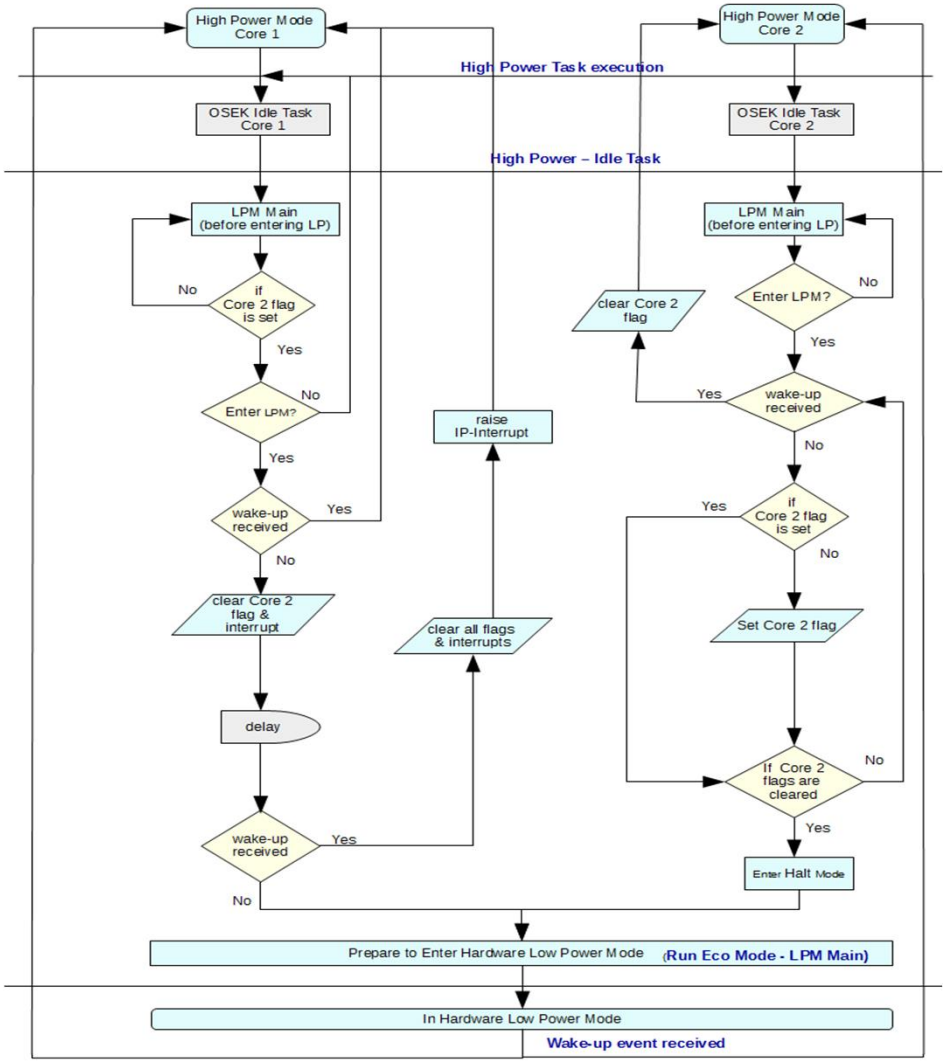


MODES OF OPERATION





DESIGN


High Power Mode Core 1
High Power Mode Core 2
High Power Task execution
OSEK Idle Task Core 1
OSEK Idle Task Core 2
High Power – Idle Task
LPM Main (before entering LP)
LPM Main (before entering LP)
No
if Core 2 flag is set
Yes
Enter LPM?
No
Yes
raise IP-Interrupt
clear Core 2 flag
Enter LPM?
No
Yes
wake-up received
Yes
wake-up received
No
clear Core 2 flag & interrupt
clear all flags & interrupts
Yes
if Core 2 flag is set
No
Set Core 2 flag
delay
If Core 2 flags are cleared
No
wake-up received
Yes
Yes
Enter Halt Mode
No
Prepare to Enter Hardware Low Power Mode (Run Eco Mode - LPM Main)
In Hardware Low Power Mode
Wake-up event received

- Master Core wakes up Slave Core in case a wake event is received
- Master Core & Slave Core should be in Idle Loop to enter LP
- If Wake-up = TRUE → Master Core sends CrossCoreISR to Slave Core