DESIGN OF THE CHRONOMETER

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Executive Summary

The Main Aim of this project is to develop a digital chronometer which can display time from 00.00 to 59.99s onto Digilent Basys2 Board.

The four LEDs present onto the board are used to display the timer value. Once the timer value reaches 59.99s the chronometer is stopped automatically.

In our design we use a 50MHz Input clock to synchronize all the components used in the chronometer.

The user is facilitated with a start_stop toggle button that they can use to start the timer or to pause it at any given point of time.

The clock can also be reset but this can be possible only when it is in a paused state or it is stopped (due to reaching its limit i.e. 59.99).

Finally, the chronometer should be implemented is such a manner that it works efficiently without any errors / delays with the simplest, fast working design.

1 Model Description

Design Description:

The Main Aim was to develop a design for a Digital Chronometer that counters from 0-5999. This design is based on the customer specifications provided as given below:

Inputs:

Clock signal CK_50M which is 50MHz from the board

BP_START_STOP signal from a push button to start and stop the chronometer;

BP_RAZ signal from a push button to reset the chronometer only when it stops.

Output:

The LED can display time from 00.00s to 59.99s. At 59.99s, the chronometer should stop automatically.

TABLE 1: CUSTOMER REQUIREMENTS

No.	Requirements
1	The Input clock runs at 50 MHz cycle
2	The chronometer LED display from 00.00s to 59.99s. The chronometer shall stop automatically when it reaches 59.99s.
3	The chronometer output shall be displayed on to four 7-segment displays available on the board
4	The counter will be initiated when the Start_Stop button is pressed
5	The start button shall act as an toggle button that starts / pause the counter on alternative button press events
6	Using the reset button the user can reset the counter. The reset can be done only if the counter is either paused or the has reached its maximum limit (59'99'')

The developed Modelhas been segregated into three main sections:

1. Top moduleof the Chronometer
2. Clock Logic sub module
3. Display Selection sub module

The top module is only for port map. The main design is in the two sub modules.

'Clock Logic sub-module' has been designed and it is as shown below.

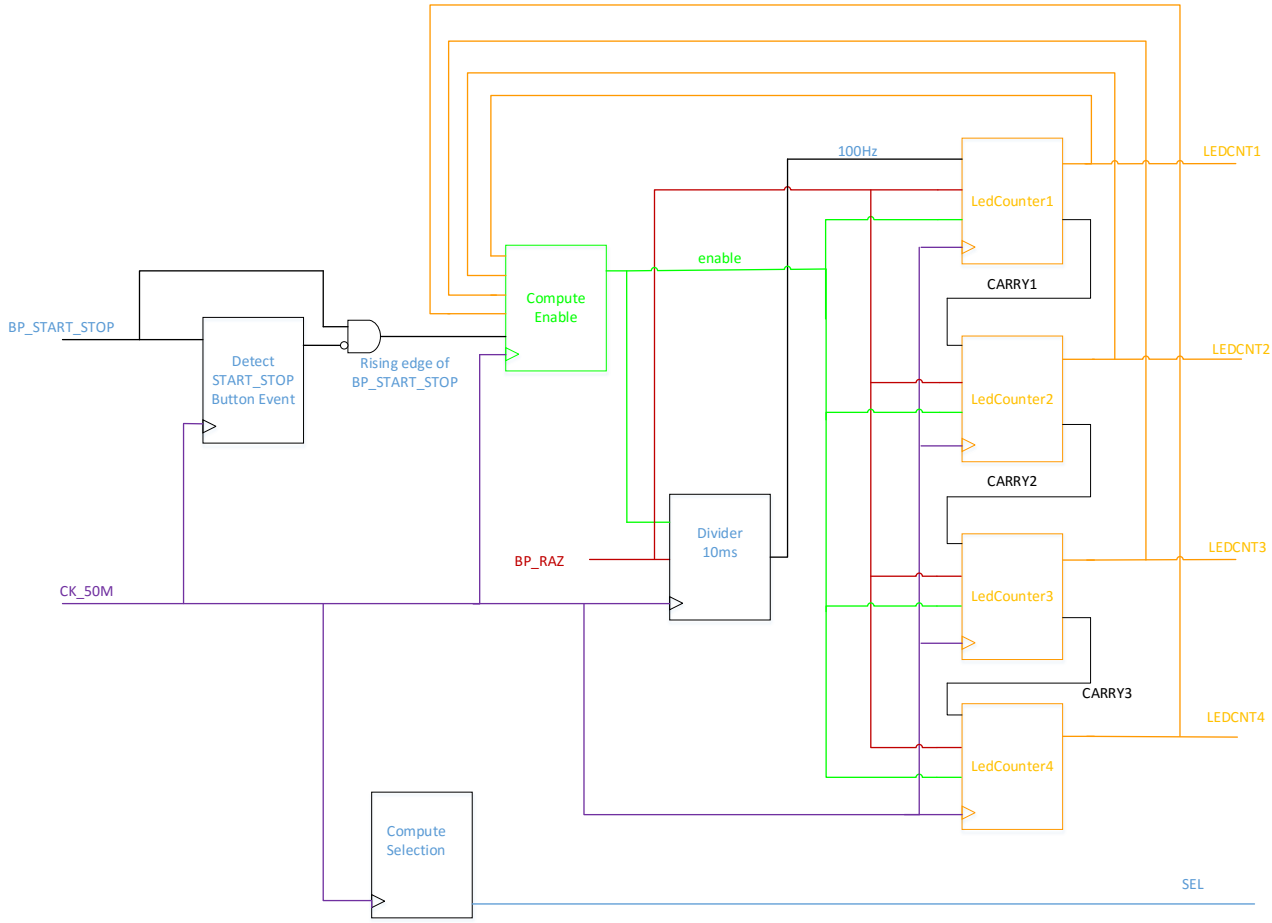

FIGURE 1: DESIGN FOR CLOCKLOGIC

Clock logic sub module design description

- ➔ The 50MHz clock is used to synchronize all the components in the chronometer
- ➔ As is shown in the Fig 1, a process is used to detect the rising edge of the BP_START_STOP signal so as to control the chronometer counter. And this rising edge signal along with the four led counter signals (LEDCNT1, LEDCNT2, LEDCNT3, LEDCNT4) are used to compute the state of enable signal. When the start_stop button is pushed or the chronometer reaches the maximum value, the enable signal should change. This signal is used to control the other components of the chronometer logic.
- ➔ The Input clock is divided to generate another signal with a frequency of 100Hz. This new signal is as an input of the LedCoutner1 process. So the chronometer can be incrementedeach 10ms.
- ➔ LedCoutner1 process has two outputs: LEDCNT1 and CARRY1. Once LEDCNT1 reaches 9, the CARRY1 value will be 1.
- ➔ This CARRY acts as one of the enablers to the next counter (tens place)
- ➔ Similar design is done for counter_3 (hundreds place) and counter_4 (thousands place).
- ➔ The enable and BP_RAZ signal are used to control the four LedCounter processes.
- ➔ A new signal named SEL ranged from 0 to 3 is created from 50MHz clock to control the LED display selection.

'Display selection sub-module' has been designed and it is as shown below.

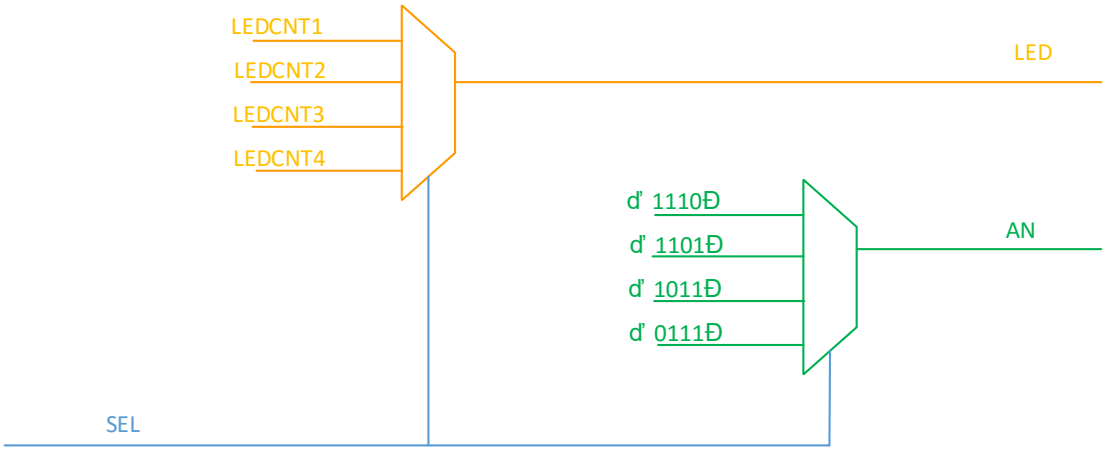

FIGURE 2: DESIGN FOR THE DISPLAY SELECTION

Display selection sub module design description.

The BASYS2 board has 4 LEDs but each LED can be written onto one at a time hence the each LED is refreshed sequentially in order to have the latest data. So the SEL signal created from the clock logic sub module is used to select which LEDCNT to be displayed and which LED is used to display the LEDCNT.

2 Simulate Behavioral Model

To reduce the simulation running time, the counter's limitused in the 10ms clock divider and the display selection clock divider are reduced to 5 and 2 respectively. So the simulation time has been reduced to 2ms.

The below simulation screenshot has been taken by setting BP_START_STOP to 1 only once, so the chronometer will keep on increasinguntil 59.99s.

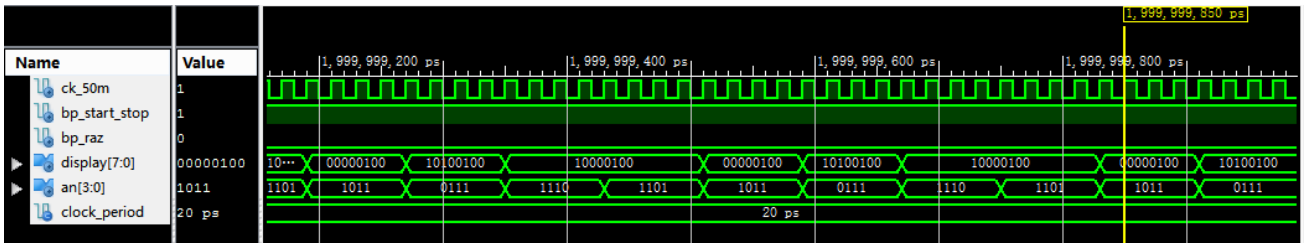

FIGURE3 SIMULATION FOR CHECKING 5999 LIMIT

In this simulation the clock will reach the 59.99 limit at about 0.6ms as we have reduced the period of the new clock. As is shown above, at about 2ms, the chronometer display does not change. For instance, if AN equals to "0111", which means that the highest bit would be displayed. And the LED display signal for the last counter remains constant with a value "10100100"in the next cycles, it will be displayed as 5. The display remains with a value 59.99 around the yellow line.

In the below simulation the BP_START_STOP is selected twice and hence the counter is paused after the yellow line.

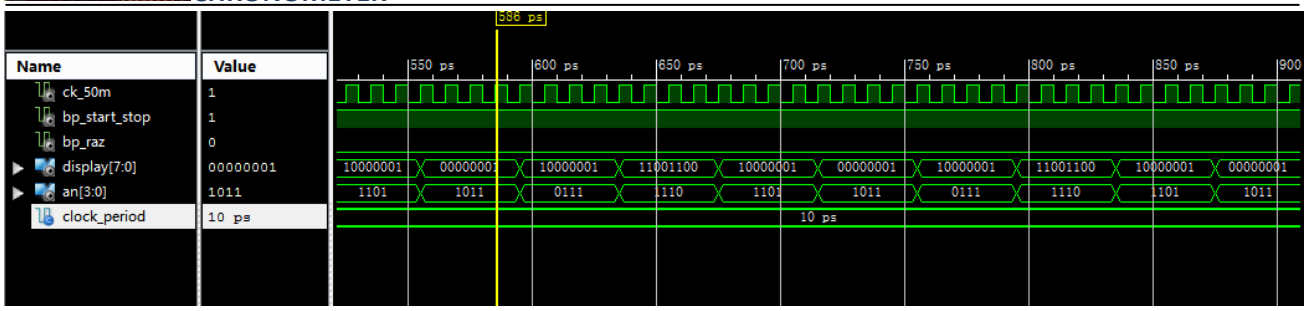

FIGURE 4 SIMULATION FOR CHECKING STOP STATE OF THE CHRONOMETER

3 Conclusion

The designed Chronometer meets the requirements.

The development of Chronometer Model gave us the opportunity to learn and design in VHDL.

Additionally, as a team we could share our view points and understand each other's ideas and come up with a common solution.

Nevertheless, in the end we were able to develop a good chronometer code, which has beensimulated and tested on BASYS2. And the chronometer works perfectly as below.