GAURAV KUMAR DEWANGAN

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OBJECTIVE:

- Seeking full-time opportunities in Semiconductor Industry for enhancing my skills and acquire profound knowledge in VLSI related fields.

Qualifications:

Education	University	Year	% / CGPA
M.Tech (ECE)	IIIT-NR, Raipur	2021	7.5
B.E (ETC)	CSVTU, Bhilai	2017	71.16

VOCATIONAL TRAINING:

- Entuple Technologies (4th June to 24th July 2020)

  Training on Floor planning, Placement, Routing, Power Planning and Hands-on experience in Cadence Innovus.

ACADEMIC PROJECTS:

- **Design and implementation of low power and high speed MIPS based RISC processor. (**M.Tech Thesis, August 2020 - May 2021**)**

  FPGA Design of MIPS based RISC processor with the help of Verilog hardware description language. In this project I tried to rectify data hazard problem present in the processor in such a way that total consumed power and total foot print area was optimized.

- **Physical Design of DMA Controller using Cadence Innovus. (Feb - May 2021)**

  Followed a generic physical design flow to understand Floor planning, Placement, Routing and Power Planning in gpdk90nm.

SKILLS:

- Languages: TCL, Verilog.
- Software Packages: Xilinx Vivado, Cadence Innovus.

AREA OF INTEREST:

- Physical Design
- Digital logic Design.

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DECLARATION:

I hereby declare that the information provided above is correct and unaltered as per my knowledge.

Place: Naya Raipur
Date : 09/06/2021