KALKOTE MAYUR TIPPANNA

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OBJECTIVE

To seek challenging responsibility in VLSI sector, with an opportunity for growth of the sector and career advancement in terms of knowledge as well as position.

TECHNICAL SKILLS

Operating System	Linux, Windows Family Networking
Programming Languages/ Scripting Languages	VHDL, Verilog, Basic C Basic Perl, TCL
Physical Design Tools / Layout Tools	Modelsim, Cadence Encounter, Mentor Graphics Cadence (Virtuoso, Assura, Spectra), RTL compiler
Programming Languages Tool	Xilinx ISE, ModelSim
Knowledge & Experience	Good Knowledge about Basic Electronics, Digital Design Experience with the **Cadence Virtuoso Tool** for **Physical design** and **Analog circuit design** Working experience on Xilinx ISE Good knowledge about **custom layout design**
Area of Interest	Physical design, Digital design and Layout design, Component design

EDUCATIONAL QUALIFICATION

Degree	Institute	Board / University	Year of passing	Percentage/ CGPA
M.Tech VLSI Design	Vellore Institute of technology University, Chennai Campus, TN	VIT University	2016	7.99
B.E. Electronics &Telecommunication	SSBT COET Bambhori Jalgaon, MH	North Maharashtra University, Jalgaon	2013	66.13%

H.S.C	Basveshwaar Junior college Latur, MH	Latur	2009	77.50%
S.S.C.	SantVinobaBhave school Khudawadi, MH	Latur	2007	84.15%

PROJECT EXPERIENCE

POST GRADUATION:

Title: Design of High Performance and Enhancement of Transconductance of Folded Cascode Amplifier Using Multi-Recycling Structure (**Layout Design and Analysis**)
Guide Name: Dr. Ananiah Durai S, Asst. Professor, VIT University, Chennai
Description: The project work deals with design of high performance recycle folded cascode amplifier which enhance its Gain and GBW (Gain bandwidth frequency). To achieve this new structure is design known as QRFC (Quadruple Recycle Folded Cascode) which is boost the gain up to 95dB and 185MHz GBW frequency with greater stability. Its overall performance is good as compare with other all OTA's. Along with working on Layout Design. Work with all analysis of amplifier such as pole- zero and noise.
Tool Used: Cadence Virtuoso (0.18um cmos tech.)

Title: Verilog Implementation Low power and Hardware Efficient FIR Filter
Guide Name: Dr. Berlin Hency, Asst. Professor, VIT University, Chennai
Duration: July 2014-December 2014
Description: The project work is concerned with the design of the FIR filter which is implemented with reduction of multipliers to reduce the area and power consumption and increase the speed of the operation.
Tools Used: Xilinx ISE, Cadence RC-64, Encounter

Title: A Verilog Implementation Of Reconfigurable High speed FFT processor
Guide Name: Prof.Shaktivel, Asst Professor, VIT University, Chennai
Duration: January 2015- May 2015
Description: The project work deals with the design of FFT processor which is used for converting the signal from time domain signal to frequency domain signal by deploying less computation technique to increase its speed and performance.
Tools Used: Xilinx ISE, Cadence RC-64, Encounter

UNDER GRADUATION PROJECT

Title: Tire pressure monitoring system and break failure indication system embedded based
Duration : 1 Year 2012-13
Guide Name: Prof. A.S.Wani, Asst. Professor , SSBT COET Jalgaon Maharashtra
Description: The project work was concerned with the design embedded based system which gives the indication about the pressure of the tire and if any case the break failure to avoid the accident on road.

PUBLICATION:

I recently published one paper "Enhancement of Transconductance using Multi- recycle Folded Cascode amplifier" in IJST 2016.

VOCATIONAL INDUSTRAL TRAINING:

I completed the training in All India Radio Osmanabad to Communication purpose for 2 month duration. This is the Government Radio Station they explain about how to FM communication takes place and explain the each and every section working in that stations related to broadcasting. Learn about how modulation takes place and actually working which is very helpful

WORKSHOPS:

- Attended workshop on "Android Apps development" conducted by PCCOE college, Pune.
- Completed workshop on "Robotics" conducted by CAMPUS COMPONENT in PVG college, Pune.
- Attended the workshop on "Automation in Industries" In SSBT COET,Jalgaon.

POSITION OF RESPONSIBILITY

- Event organizer for MEC FEST Competition in SSBT COET Jalgaon MH
- Active Member of ETECA Committee

DECLARATION

I do hereby declare that the particulars of information and facts stated here in above are true, correct and complete to the best of my knowledge and belief.

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