Curriculum Vitae

JUHI

Master of Technology
Inderprastha Engineering College, *Gzb(U.P.)*

Achievement

Paper Published– Design, implementation and analysis low power pulse decoder for SRAM in 45nm CMOS technology

IJARECE (2016)

Areas of Interest

- Digital Electronics
- Networking
- VLSI

Research Interest

- VLSI Technology
- Power Minimization in SRAM.

Objective

Seeking a challenging, entry level position to utilize my skills and abilities in the industry that will allow me to expand my knowledge being resourceful, innovative and flexible.

Experience

PCB Design engineer at megha circuits, GZB(Jan-17 to April 17)

Designer at R D Pack Oct 2018- present.

Education

Academic Qualifications:

M.Tech. (VLSI Design)

- Institute: Inderprastha Engineering College, Ghaziabad
  (Affiliated to Dr. A.P.J. Abdul Kalam University, Lucknow)
- Percentage: 77 %

Session: 2013-2016

B. Tech. (Electronics & Communication)

- College : Krishna Engineering College, Ghaziabad
  (Affiliated to Uttar Pradesh Technology University(UPTU))
- Percentage: 65%
- Session : 2008-2012

12th Shree Thakur Dwara Balika Vidyalaya, Ghaziabad

- Board: CBSE
- Percentage: 68 %.
- Session : 2008

10th Shree Thakur Dwara Balika Vidyalaya, Ghaziabad

- Board: CBSE
- Percentage: 77.4 %.
- Year: 2006

Training & Workshop

- Organized and participated advance workshop on cadence virtuoso tool.
- **Organization:** BEL(Sahibabad, Ghaziabad)
  Duration: Six weeks training (July 2011 to August 2011)
  Project: Study of "IFF Radar"

- Attended one day seminar of Microsoft.
- Attend one day workshop on embedded system.
- One Months (June 2009- July 2009) Course on **C Language** from **SGIT**(Ghaziabad)

Personal Data

Date of Birth: 14/01/1992
Sex : Female
Father : Late. Sh. R.B.Singh

Permanent Address

III-H 44/1, Nehru Nagar,
Rakesh Marg.
Ghaziabad-201001
Contact**:** +91-9319334681

E-Mail:

juhiece@yahoo.com

Academic Projects

*Thesis:*Design, implementation and analysis low powerpulse decoder for SRAMin45nm CMOS technology.

CMOS circuits are designed to minimize power dissipation and low area consumption. Pulse decoder is design to reduce the total power consumptionand analysis the leakage power, total power consumption.

Projects:

- Analysis various SRAM structure for calculating the SNM
- Automatic room light and temperature controller with visitor counter

Hands on Experience

Designing Tools:

- Cadence Virtuoso
- Protel 99 se
- Mentor Graphics IC Station
- Coral draw

IT Skills:

- Application Package :Microsoft Office 2007/2010/2013
- Operating System : Windows 7 & Windows 8, Linux

HDL & Programming Language Proficiency:

- VHDL
- C

I hereby declare that the above mentioned information is true to my knowledge and belief.

Date 2019

Place: Ghaziabad **JUHI**