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HW 2

2.5
a) Suppose offsets can be 0, 8, 16, or 24 bits (including the sign bit); what is the average length of an executed instruction?

Load 26%
Store 10%
Branch 12% + Jump 1% + Call 1%

How often (frequencies)

0: (36% * 30.4% + 14% * 0.1%) * 16 = 1.773440
8: (36% * 41.2% + 14% * 90.4%) * 24 = 6.597120
16: (36% * 28.4% + 14% * 9%) * 32 = 3.674880
24: (36% * 0% + 14% * 0%) * 40 = 0
Other: (50%) * 16 = 8.00

Sum for the average: 20.05
Approximately 20 bits on average.

b) Suppose we want a fixed length instruction, we chose 24 bits. For every offset >8 bits, additional instructions are required. Determine the instruction bytes fetched this machine in the 2 scenarios (fixed and variable length).

Variable Length: 2.51 bytes per instruction. (See math from a).

Fixed length > 8 bits require an additional arithmetic operation which is another 24 bits (because all operations are).

(11.0840% + 27.4880% + 50%) * 3 bytes = 2.65716
(11.484%) * 6 bytes = 0.68904
Total: 3.3462 bytes on average.

The fixed length is 3.34 bytes versus 2.51 bytes

c) Suppose we use a fixed offset length of 24 bits, so no additional instruction is ever required.

So others are 16 bits, load/store/branch are 40 bits.

(36% + 10% + 14%) * 40 = 24
(50%) * 16 = 8
32 bits, 4 bytes

This scenario produces worse results than with my method with part b. It appears variable length has the lowest average bytes per instruction.

2.12

Consider adding a new addressing mode to MIPS. The mode adds 2 registers and an 11-bit signed offset.

2 instructions are replaced by 1 (that handles the offsets for 10% of displacement load/stores).

a) Assume that the addressing mode can be used for 10% of the displacement load/stores. What is the ratio of instruction count on the enhanced MIPS compared to the original?

New addressing mode can be used for 10% of displacement addressing instructions.
This is an improvement of 10% of the 36% of instructions. (3.6% improved)

This means 10% went from requiring 2 instructions to 1. That is ½ the instructions for 10% of 36% of the total. 3.6% was improved by 100% → 1.8% less instructions.

(100-1.8)/100 = .982

.982 of the instructions.

b) The total execution time will reveal if this system is faster if the clock cycle is lengthened by 5%.

execution time = instructions * CPI * clock cycle time

original = 100 * CPI * clocktime
new = 98.2 * CPI * 1.05clocktime

(100 * 100) / (98.2 * 105) = 0.9698

= 10000/10311 → original was faster by 1.031x.