KYUNGPOOK NATIONAL UNIVERSITY

COMP311-1 Logic Circuit Design (Syllabus)

Instructor: Taigon Song (송대건)

2019 Fall

Last update: 2019.9.1

COMP311-1 Logic Circuit Design

- Class hours/room: Mon 9am–12pm (IT2-206)
- Credit: 3
- Textbook
  - Verilog HDL, 2nd, Samir Palnitkar/장훈 역
  - Students are encouraged to choose either one

- Instructor: Prof. Taigon Song(송대건)
- Contact: (T) 053-950-5535, (email) tsong@knu.ac.kr
- Office: IT2-241
- Office hours:
  - Per request (by email)
  - TBD

Grading Policy

- Attendance - 10% (Absence: -1, Late class: -0.5)
  - Late: +10 min from the beginning of the class
  - Absence exceeding 2 times will be accounted for negative credit
  - **1% of participation credit**
- Homework - 25%
  - Projects included
- Mid-term - 20%
- Final exam - 25%
- Quiz - 20% (5%, 15%)
  - 9/30, 11/25 (during class, 1hr)

Participation Credit

- Students are encouraged to ask many questions that are related/non-related to the class
  - ***English/Korean both encouraged***
- By just asking one question, ***you get 1% of the total credit*** of this class
  - i.e.) 1% is 20 points in your first quiz (20/100 of 5%)
  - So don't miss it

- Conditions
  - For any "non-related to the class" questions, these questions cannot overlap
  - For any "class-related" questions, you may ask any
  - No obvious statements

Attendance

- This class requires each student to **place their name tag in front of their desk by the start of the class.** Failing to do so will result as an absence or late in class.

Policy for Impaired Students

- This class ***fully supports*** students with impairments.
  - Please let the instructor know if you have trouble in studying this course.

No Cheating!!!

- This class will follow the policy of the school of EE for academic dishonesty when noticed.
  - **In other words, “F”.** Thus, this class strongly encourages its students to be honest for their work.

Email Etiquette

- This class will ask students to use the email title of **[COMP311-1]** when contacting the instructor for questions. The instructor will not respond when this policy is not followed.

- E.g.)
  - [COMP311-1] 수업관련 문의 드립니다.
  - [COMP311-1] A question in chap. 2
  - [COMP311-1] Request to …
  - [COMP311-1] Regarding the final term project

Experienced Student Penalty

- Penalty to the 'experienced' students that are taking this course more than once.
  - '**A-**' will be the upper limit to the final grades that those experienced students can achieve.

Course Schedule (Tentative)

Week	Dates	Topics	Note
1	9/2	Ch. 1-2. and Tool tutorial	
2	9/9	Ch. 3. Basic Concepts	
3	9/16	Ch. 4 Modules and Ports	
4	9/23	Ch. 5. Gate lv Modeling	
5	9/30	Ch. 6. Dataflow Modeling	Quiz 1 (9/30)
6	10/7	Ch. 7. Behavioral Modeling	
7	10/14	Ch. 8. Tasks and Functions	
8	10/21-10/25	Mid-term exam	

Course Schedule (Tentative)

Week	Dates	Topics	Note
9	10/28	Ch. 9. Useful Modeling Techniques	
10	11/4	Ch. 11. Timing and Delays	
11	11/11	Ch. 12. User-def Primitives	
12	11/18	Ch. 14. Logic Synthesis w/ Verilog HDL	
13	11/25	Final Project (1)	Quiz 2 (11/25)
14	12/2	Final Project (2)	
15	12/9-13	Make-up classes	
16	12/13–19	Final Exam	

Others (but very important)

- LMS System
  - Course materials and notices will be uploaded in the KNU LMS system
  - http://lms.knu.ac.kr