



COMP311-1 Logic Circuit Design Chap. 1

Instructor: Taigon Song (송대건)
2019 Fall

Evolution of Computer-aided Digital Design

- Early digital circuits with vacuum tubes
- IC: Integrated circuits in
 - SSI: Small Scale Integration
 - MSI: Medium Scale Integration (hundreds of gates)
 - LSI: Large Scale Integration (> 1000 gates)
 - VLSI: Very-large Scale Integration (> 100,000 transistors)
 - Measurement and verification were impossible to perform by hand
 - Design automation?...
- EDA: Electronic Design Automation
 - Before the era of EDA, everything was done by hand
 - Designing, testing...etc.

Processing Information

Mechanical? Electronical?

- Mechanical
 - <https://www.youtube.com/watch?v=OFJUYFISYsM>
- Electronical



vs.



https://www.amazon.com/Calculator-Helect-Standard-Function-Desktop/dp/B01B5MU6JG/ref=sr_1_4?keywords=calculator&qid=1551576516&s=gateway&sr=8-4

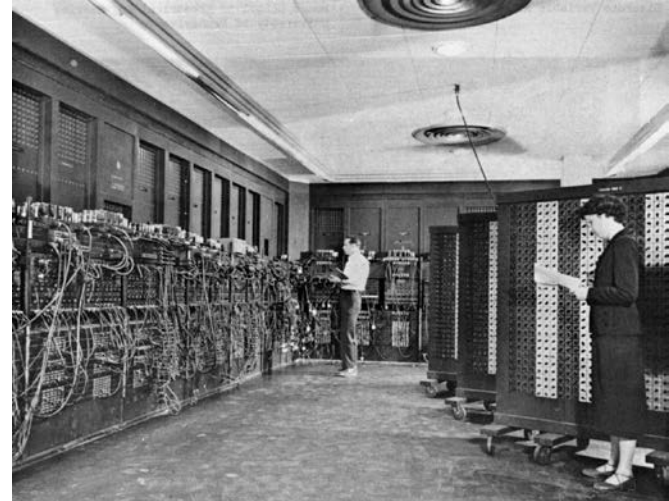
<https://www.google.com/url?sa=i&source=images&cd=&ved=2ahUKEwi7kfHogJvkAhVIQN4KHR9hAR0QjRx6BAGBEAQ&url=https%3A%2F%2Fwww.youtube.com%2Fwatch%3Fv%3D5utHg7tG10c&psig=AOvVaw3wggw0SEP0Jw9tWzt7NCs2&ust=1566718877232446>

Note. This lecture is not connected to the product by any means and is describing this product solely for educational purpose.

ENIAC – The First Computer

- **Specs**

- **Width** : 1m
- **Height**: 2.5m
- **Length** : 25m
- **Weight** : ~ 30t
- **# of Vacuum tubes** : ~18,000
- **Power** : 1,500kWh



- LG Gram 14Z990-GA5IK

- **Size**: 323x212x16.5mm
- **Weight**: ~995g
- **Power**: 10.7kWh

Sources:

<https://ko.wikipedia.org/wiki/%EC%97%90%EB%8B%88%EC%95%85>

<http://prod.danawa.com/info/?pcode=7971001&cate=112758>

How Expensive is Electricity?

- Note: ENIAC's power consumption: **1500kWh**
 - At least 300k won per hour

계약종별 전기요금 계산 | 전기요금계산기 사용방법

1. 계약종별선택

주택용(저압)
주택용(고압)
일반용(갑) I
일반용(갑) II
일반용(을)
1주택 수 가구
교육용(갑)
교육용(을)
산업용(갑) I
산업용(갑) II
산업용(을)
임시(갑)
임시(을) 300kW▼
임시(을) 300kW▲
임시(을) 300kW▼
시간대별 요금사용
가토등(을)
심야전력(갑)
농사용(갑)
농사용(을)

2. 조건선택

대가족요금/생명유지장치요금
☐ 5인 이상 가구
☐ 출산가구
☐ 3자녀 이상 가구
☐ 생명유지장치
☒ 해당없음

복합할면요금

사용기간
2018.01.01 ~ 2018.01.31

사용량 700 kWh

요금계산

3. 계산된결과

계산된 금액은
167,950원 입니다.

4. 상세계산내역

■ 월간 700kWh 사용시 전기요금 계산(주거용)

기본요금(원미만 결사) : 7,300원

전력량요금(원미만 결사) : 140,420원

전기요금계(기본요금 + 전력량요금)
: 7,300원 + 140,420원 = 147,720원

부가가치세(원미만 4사 5입) : 147,720원 × 0.1 = 14,772원

전력산업기반기금(10원미만 결사) : 147,720원 × 0.037 = 5,460원

청구금액(전기요금계 + 부가가치세 + 전력산업기반기금)
: 147,720원 + 14,772원 + 5,460원 = 167,950원(10원미만 결사)

ddengle.com by %nick_name% on 2018-11-01

Source:
<https://www.ddengle.com/mining/6285565>

CPU Design in the Early Days

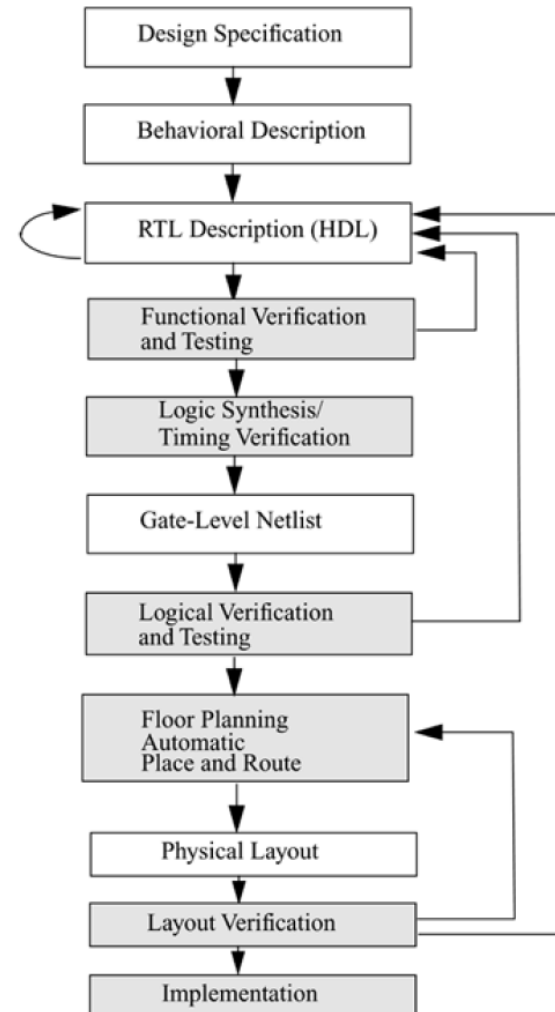
- An Intel 4004 processor example
 - http://www.intel4004.com/4004_original_schematics.htm

Emergence of HDLs

- Sequential languages to describe computer programs
- Hardware Description Languages (HDL) for concurrent hardware designs
 - Verilog HDL from Gateway Design Automation (1983)
 - Acquired by Cadence Design Systems (www.cadence.com)
- Concept of logic synthesis invented (1980s)
 - Design Compiler by Synopsys Inc. (www.synopsys.com)
 - Era of **RTLs** (**register transfer level**)
 - Source code for hardware design
- HDL now used for system-level design
 - FPGA (Field Programmable Gate Arrays), PAL (Programmable Array Logic) becomes useful for various purposes
- Current Verilog HDL standard
 - IEEE1364-2001

Typical Design Flow

- For what?
 - Think what makes “\$\$\$” in the semiconductor business



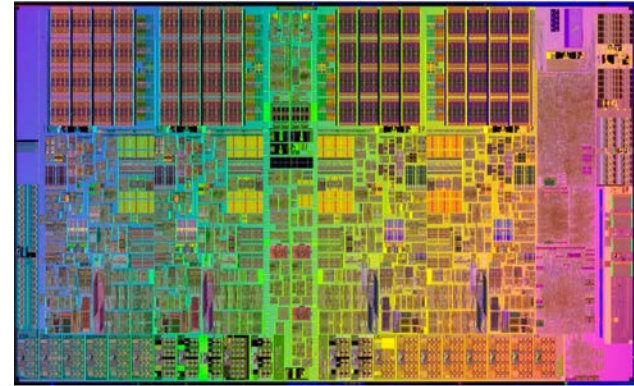
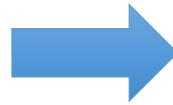
Silicon Design and Verification

How IC designs are done

- An RTL-to-GDSII flow

```
Module intel_i7 (clk, input_a, input_b, ... output_z);  
  input clk, input_a;  
  output output_a, output_b;  
  ...  
endmodule
```

RTL



GDSII

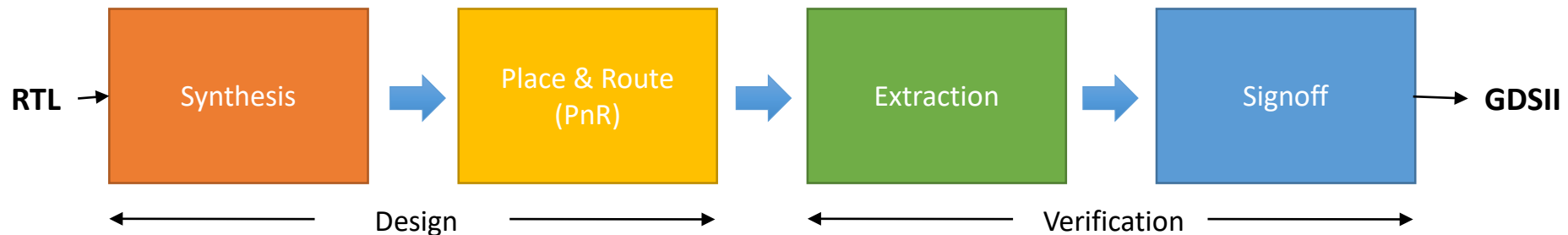
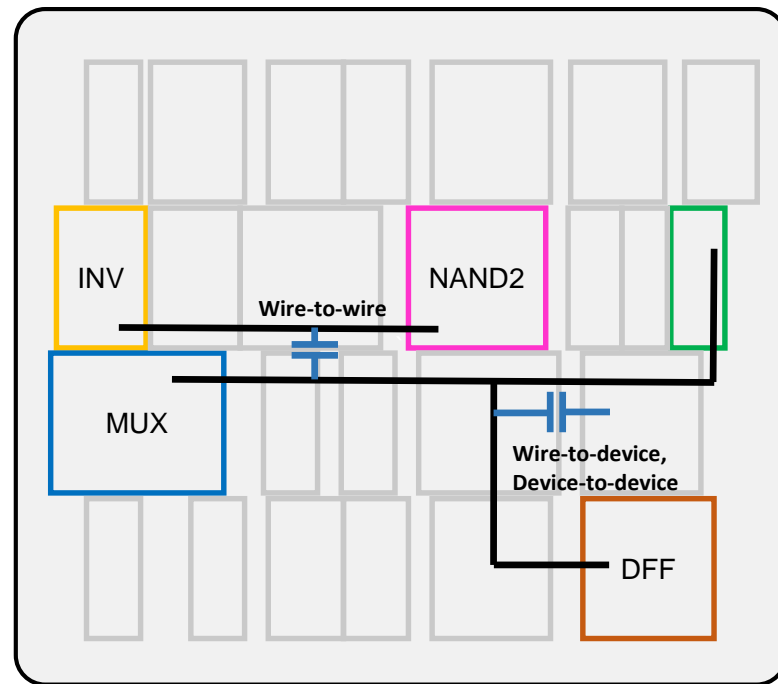
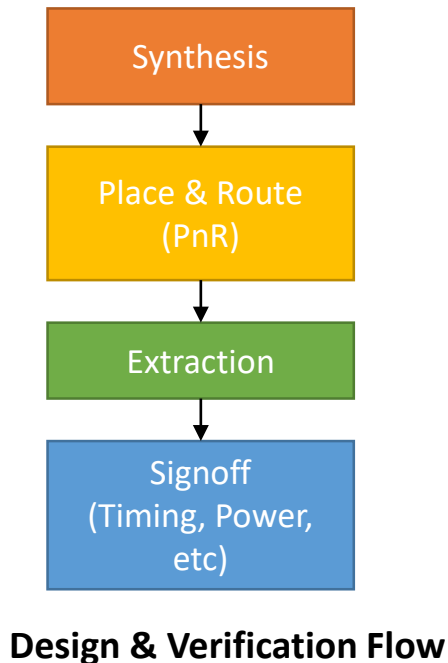


Image source : Intel

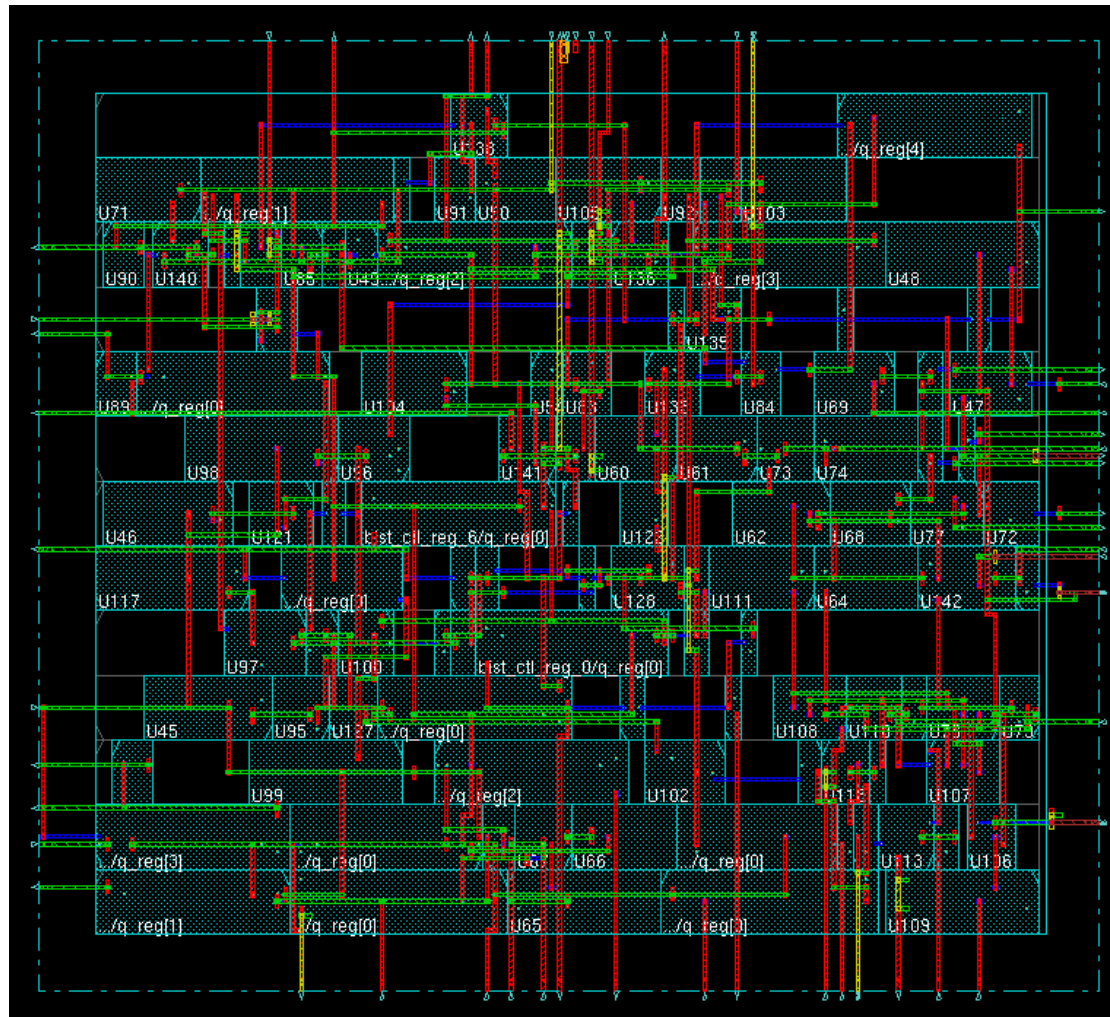
Silicon Design and Verification

Details of IC design and verification



Actual Layout

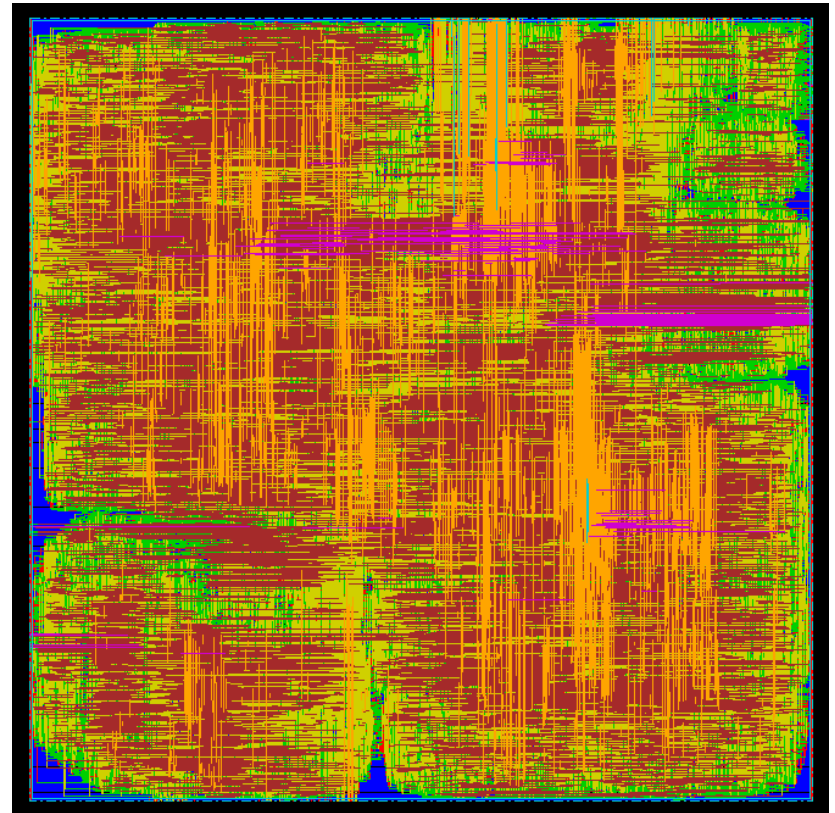
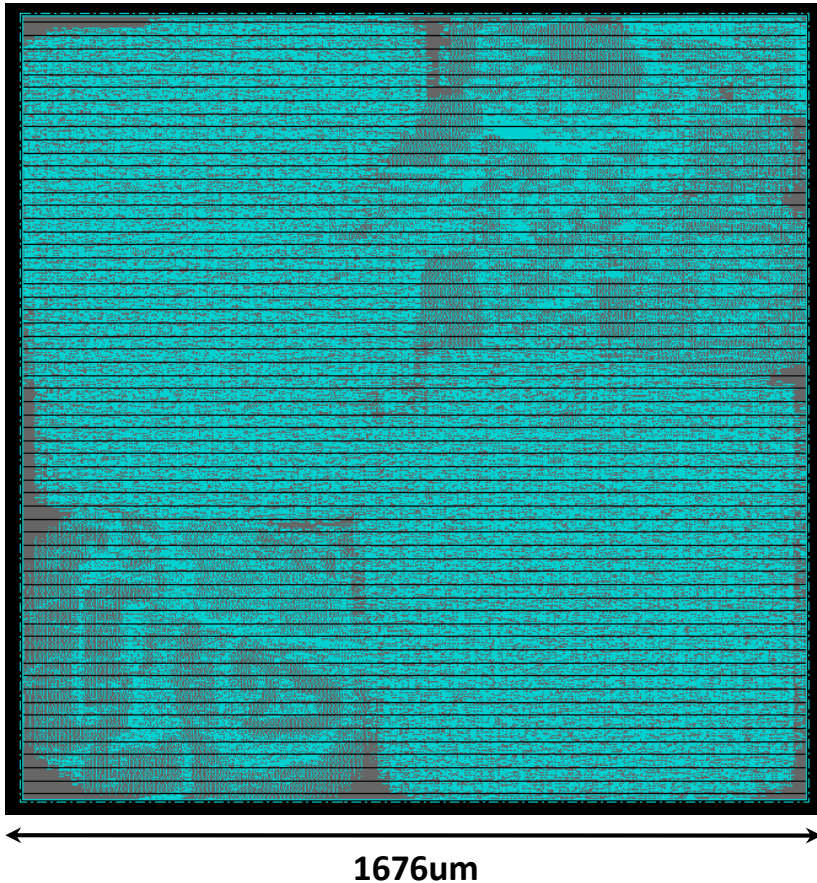
test_stub_bist (in OpenSPARC T1)



Layout of FGU

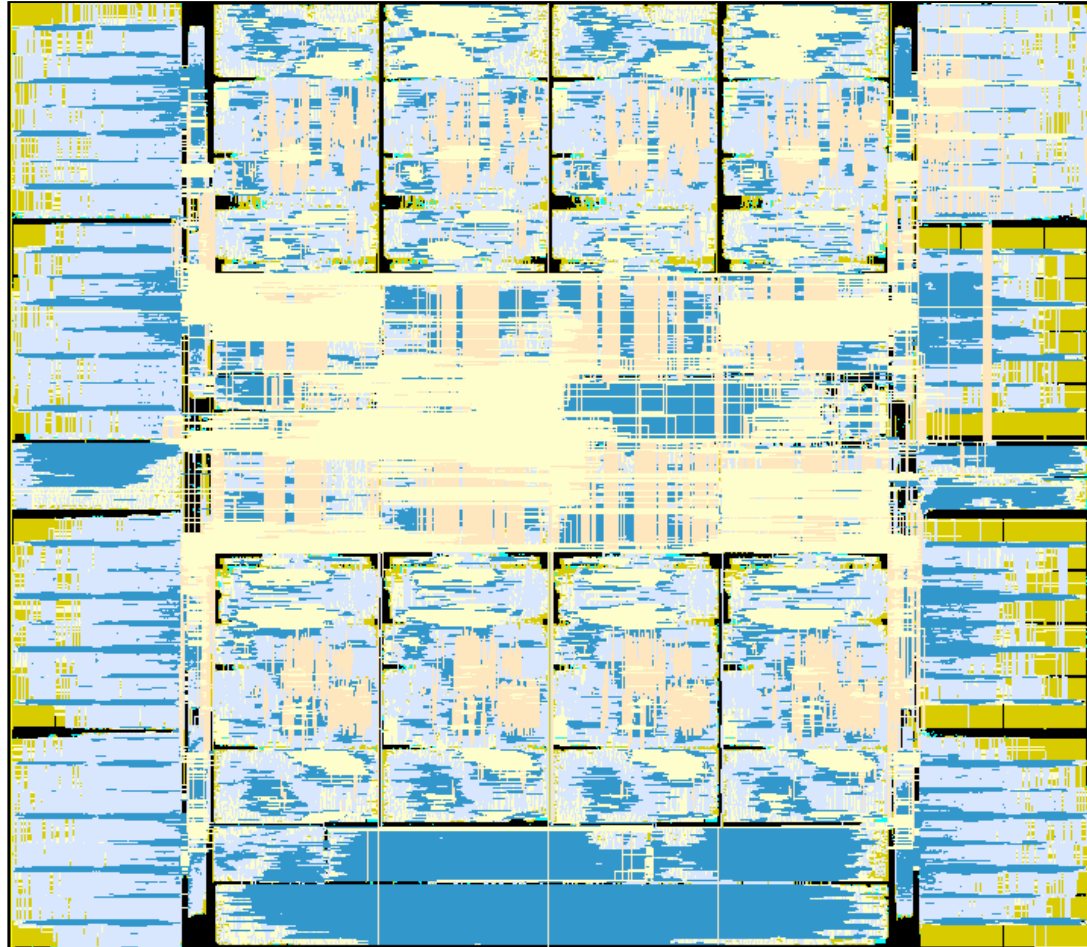
A module in OpenSPARC T1

- In 90nm Technology
 - Cell count: 111k



GDSII Layout of a Commercial CPU

- OpenSPARC T2 in 28nm Technology
 - 9mm x 8mm
 - 7.41M cells

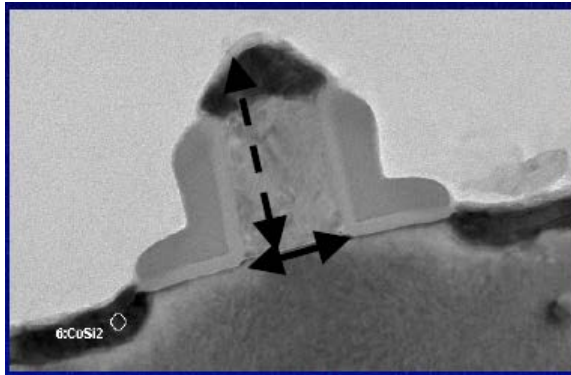


Importance of HDLs

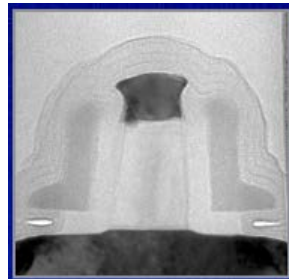
- A very abstract level design is possible by HDLs
 - Immune to fabrication technology
 - By Synthesis magic!
- Functional verification can be done early in the design cycle
 - Reducing \$\$\$
- Easier to develop and debug

50+ Years of Transistor Scaling

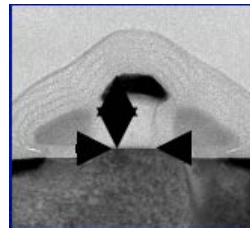
Accelerated scaling of planar transistors from 2001



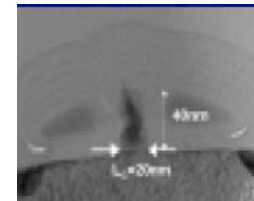
130nm Node
(Production 2001)



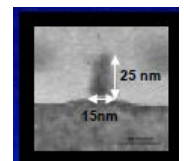
90nm Node
(Production 2003)



65nm Node
(Production 2005)



45nm Node
(Production 2007)

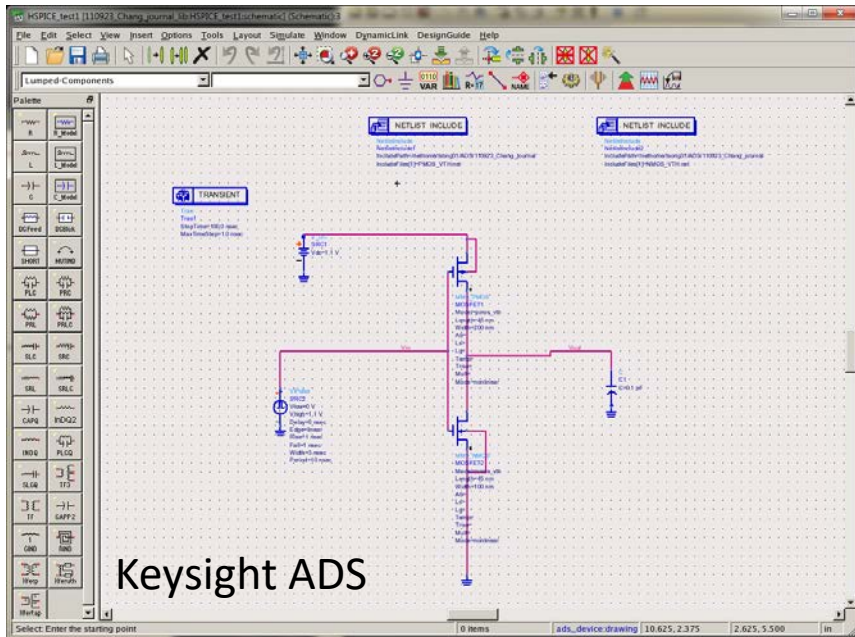


32nm Node
(Production 2009)

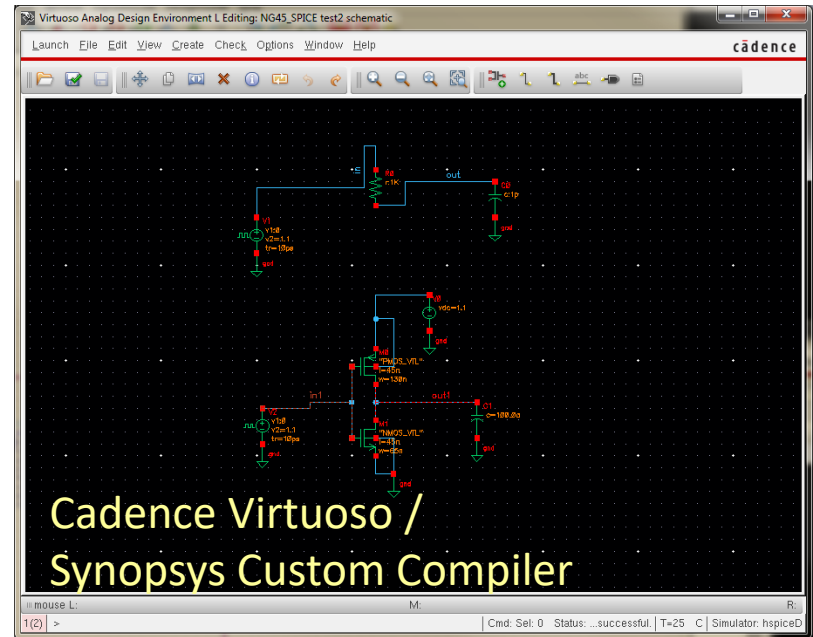
Source: Intel
Gerald Marcyk, "High Performance Non-planar Tri-gate Transistor Architecture"

Schematic vs. Verilog

Which is more simple?



Keysight ADS



Cadence Virtuoso /
Synopsys Custom Compiler

1. module inv(input A, output B);
- 2.
3. //-- Both the input and the output are "wires"
4. wire A;
5. wire B;
- 6.
7. //-- Assign the inverse of the input, to the output
8. assign B = ~A;
- 9.
10. endmodule

Verilog HDL

Popularity of Verilog HDLs

- General-purpose hardware description language
 - Similar to C language (easy to use).
- Allows different levels of abstraction to be mixed
 - Switches, gates, RTL, or behavioral code
- Popular logic synthesis tools support Verilog HDL
 - Synopsys Design compiler, Cadence Genus ... etc
- Abundant libraries
 - All fabrication vendors provide Verilog HDL libraries for post-logic synthesis simulation
- Programming Language Interface (PLI)
 - Other languages to interact with Verilog HDL

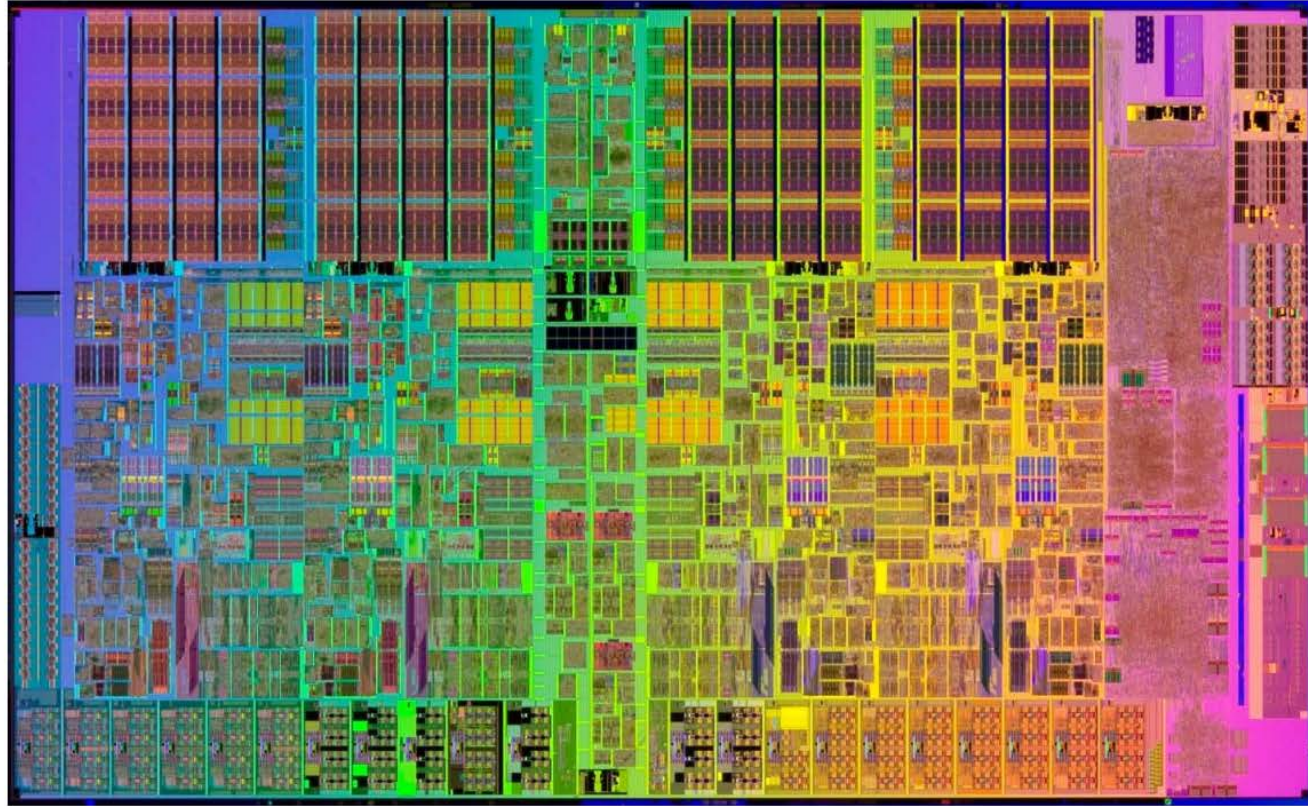
Trends in HDLs

- To design HDLs in an RTL level
 - From now on, **let's use the term RTL** for Verilog source coding
- Formal verification and assertion checking techniques emerged
- New verification languages
- For very high-speed and timing-critical circuits like microprocessors, gate-lv netlists by logic synthesis tools is not optimal.
 - Often gate-lv description directly mixed into RTL coding
- Mixed bottom-up methodology for system-lv design
 - A mix of RTL (e.g., CPU) and behavioral modules (e.g., I/O, GPU, bus ...etc)

Why Not Design a Complex IC?

(*Integrated **C**ircuits*)

- Can I make this using Verilog HDL?
 - Yes!!!



Source: Intel

So, Now What?

- In this class, let's target in designing a reasonable logic structure
 - Say, a calculator

Amazon's **Choice**

Calculator, Helect Standard Function
Desktop Calculator - H1001



https://www.amazon.com/Calculator-Helect-Standard-Function-Desktop/dp/B01B5MU6JG/ref=sr_1_4?keywords=calculator&qid=1551576516&s=gateway&sr=8-4

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Let's Design a Calculator

*That's **all** you need for this semester*

- Primary function:
- Ingredients: VDD/VSS, logic gates
- Questions
 - How would I want to add numbers?
 - Numbers... how do I represent them?
 - How do I represent addition?
 - What more?