HW#3 design an inverter that models delay

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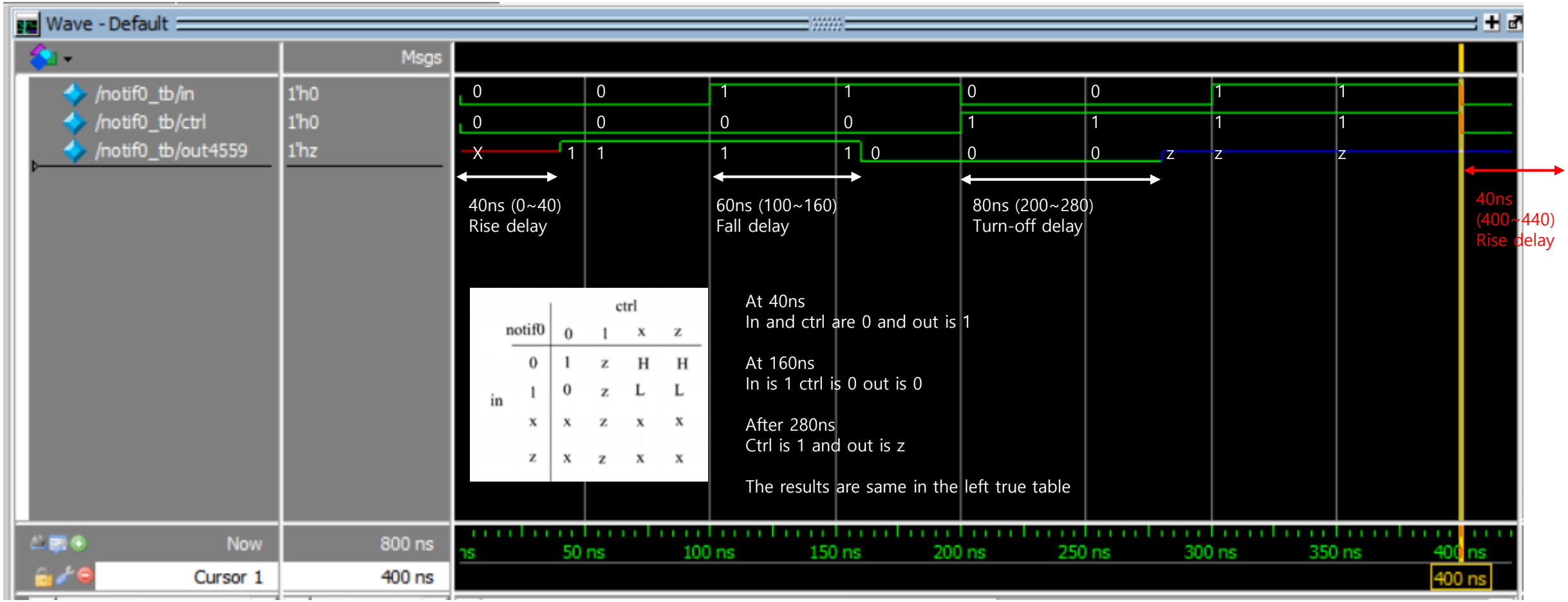
notif0_tb.v

```
1  module notif0_tb();
2      reg in,ctrl;
3      wire out4559;
4
5      notif0 #(40,60,80) n1(out4559,in,ctrl);
6
7      initial begin
8          in=0;
9          ctrl=0;
10     end
11
12     always
13         #100 in=~in;
14     always
15         #200 ctrl=~ctrl;
16
17 endmodule
```

I set Rise delay 40 , fall delay 60 , turn-off delay 80

Input chainges in every 100ns
Control changes in every 200ns

Waveform Result



notif0 \ ctrl	0	1	x	z
0	1	z	H	H
1	0	z	L	L
x	x	z	x	x
z	x	z	x	x

(in)