HW2 Design a 4:1 mux

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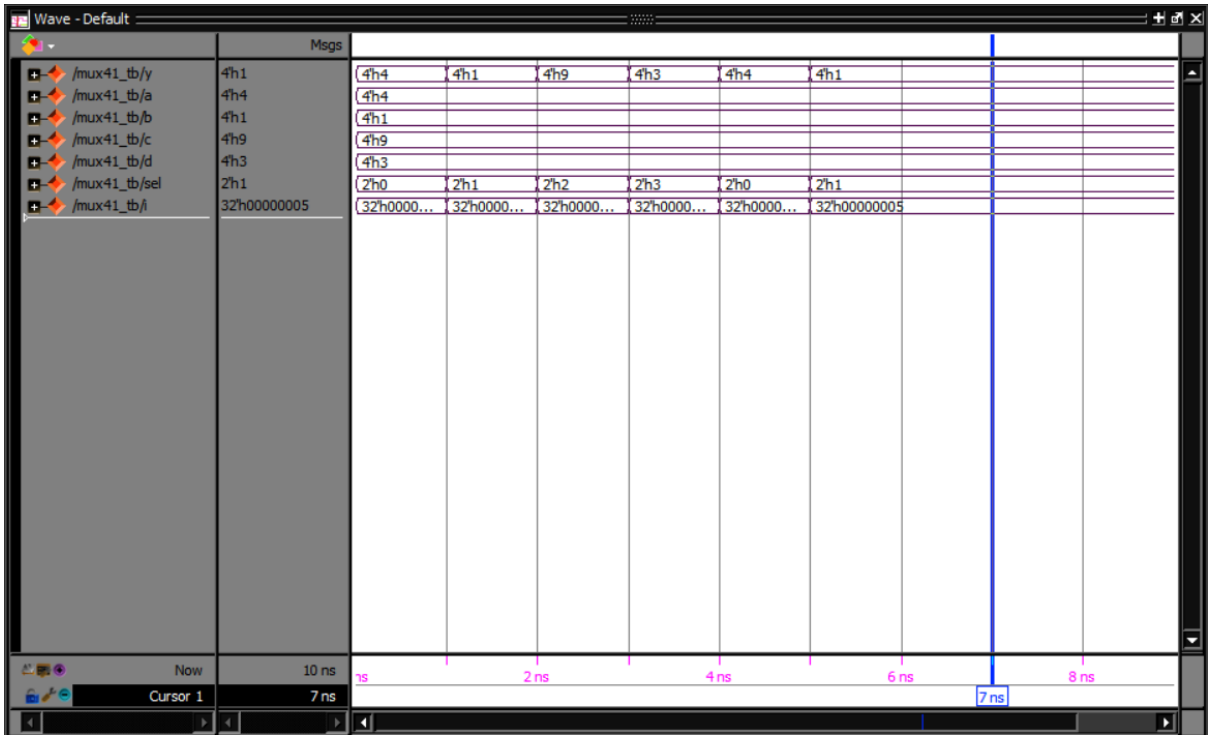
```v
module mux41(a,b,c,d,sel,y);
    input [3:0] a,b,c,d;
    input [1:0] sel;
    output reg [3:0] y;

    always@(*) begin
        case(sel)
        2'b00: y=a;
        2'b01: y=b;
        2'b10: y=c;
        2'b11: y=d;
        endcase
    end
endmodule

//mux41.v
```

```v
`timescale 1ns/1ns
module mux41_tb();
    wire [3:0] y;
    reg [3:0] a,b,c,d;
    reg [1:0] sel;
    integer i;

    mux41 m1 (a,b,c,d,sel,y);

    initial begin
        a=$random;
        b=$random;
        c=$random;
        d=$random;
        sel=0;
        for(i=0; i<5; i=i+1)
            #1 sel = sel+1;
    end
endmodule
//mux41_tb.v
```



I make 4:1 mux using case and set input and output 4bits [3:0] , sel 2bits [1:0]

In testbench I initialized reg a,b,c,d randomly by using $random and use for to change sel value I add #1 at line 17 because in initial they didn`t show the changes of sel values