fractal and fractional

MDPI

Article

Hardware Implementation and Performance Study of Analog PI$^{\lambda}$D$^{\mu}$ Controllers on DC Motor

Dina A. John [1,*], Saket Sehgal [2] and Karabi Biswas [1]

[1] Department of Electrical Engineering, IIT Kharagpur, West Bengal 721302, India; karabi@ee.iitkgp.ac.in
[2] Indian Air Force, Vayu Bhawan, New Delhi 110004, India; saket.sehgal@gmail.com
* Correspondence: dinaanna@ee.iitkgp.ernet.in

Received: 14 April 2020; Accepted: 7 July 2020; Published: 15 July 2020

Abstract: In this paper, the performance of an analog PI$^{\lambda}$D$^{\mu}$ controller is done for speed regulation of a DC motor. The circuits for the fractional integrator and differentiator of PI$^{\lambda}$D$^{\mu}$ controller are designed by optimal pole-zero interlacing algorithm. The performance of the controller is compared with another PI$^{\lambda}$D$^{\mu}$ controller—in which the fractional integrator circuit employs a solid-state fractional capacitor. It can be verified from the results that using PI$^{\lambda}$D$^{\mu}$ controllers, the speed response of the DC motor has improved with reduction in settling time (T_s), steady state error (SS error) and % overshoot (% M_p).

Keywords: DC motor emulator; fractional PI$^{\lambda}$D$^{\mu}$ controller; solid-state fractional capacitor; optimal pole-zero interlacing algorithm; rise time; settling time; steady state error; % overshoot

1. Introduction

PI$^{\lambda}$D$^{\mu}$ controllers exhibit promising features like minimizing the steady state error, robustness to plant gain variations, disturbance rejection and faster response over PID controllers [1,2]. Some of the works of PI$^{\lambda}$D$^{\mu}$ controllers are reported in [3–18]. Similarly, the works on a DC motor can be seen in [19–29]. Recent works of analog PI^{λ}D$^{\mu}$ controller on a DC motor includes implementation by Operational Transconductance Amplifiers (OTA) [30] or using CMOS op-amp [31]. Even though the above methods can provide electronic tunability, it has disadvantages such as: restriction on the maximum input signal that the circuits can handle (which is less than 1 V), requirement of more active components, resistors and capacitors for its implementation and only simulation studies are published. On the counterpart, a discrete version of the controller on a DC motor can be seen in [32,33] where special care must be taken for choosing the following: sampling rate, A/D and D/A converters, type of discretization rule used, skills in coding, computational and memory requirements. All the above methods utilize frequency domain approach for designing the controller and for that, the model of the plant is essential, and in [34], simulation studies on a model free technique for the design of a data driven fractional PID controller is demonstrated. The algorithm uses iterative computation and hence, it requires a computer.

From the above, it can be seen that the majority of the works done on a DC motor uses discrete type fractional controllers and for analog implementation of PI$^{\lambda}$D$^{\mu}$ controller, one needs op-amp/other active elements and fractional order elements. The fractional order elements can be implemented either by a multicomponent method (e.g., ladder circuits [35]) or single component fractional capacitors (like the fractional capacitor reported in [36]). The major issue is that the single component fractional capacitors (which reduces the circuit complexity) are not yet commercialized. So in this paper, we will show the performance comparison of two types of analog PI$^{\lambda}$D$^{\mu}$ controllers on a DC motor emulator in real time. One PI$^{\lambda}$D$^{\mu}$ controller is employing the commercially available op-amp, resistors and

capacitors for its realization and it is compared with the controller implemented using a single component fractional capacitor.

This paper is an extension of the work reported in [37]. In that paper, we have studied the performance of a solid-state fractional capacitor based $PI^{\lambda}D^{\mu}$ controller where the analog fractional integrator has the stated fractional capacitor in the feedback path of the circuit. In this research work, we will develop optimal pole-zero interlacing algorithm based analog I^{λ} and D^{μ} circuits; and the $PI^{\lambda}D^{\mu}$ controller based on this (termed as Type A controller) is implemented on hardware. The performance of Type A $PI^{\lambda}D^{\mu}$ controller is compared with the previously reported $PI^{\lambda}D^{\mu}$ controller (named as Type B: where fractional integrator employs solid-state fractional capacitor). The study is done on the speed regulation of the DC motor emulator. Thus, the paper focuses on the comparison of the performance of these two types of analog $PI^{\lambda}D^{\mu}$ controllers (one by the multicomponent approach and the other by a single component fractional capacitor) and present its advantages.

The paper is divided into six sections. Section 1 deals with the introduction. Section 2 describes Type A and Type B $PI^{\lambda}D^{\mu}$ controllers. The details of the hardware implementation and the tuning algorithm for the fractional PID controller are given in Sections 3 and 4, respectively. Then, the results are elaborated in Section 5 and the conclusion in Section 6.

2. Theory

2.1. DC Motor Emulator

The transfer function of the DC motor [37] under study is given as:

$$G(s) = \frac{V_{\omega}(s)}{V_a(s)} = \frac{1.91 \times 10^6}{s^2 + 666.7s + 1.948 \times 10^6} \tag{1}$$

where $V_{\omega}(s)$ is the voltage corresponding to speed and $V_a(s)$ is the armature input voltage to the DC motor. Equation (1) is implemented using resistors, capacitors and op-amps to emulate the DC motor which has a gain stage followed by two integration stages (as illustrated in Figure 1), and on this emulated circuit, the comparison studies of Type A and Type B fractional PID controllers have been carried out.

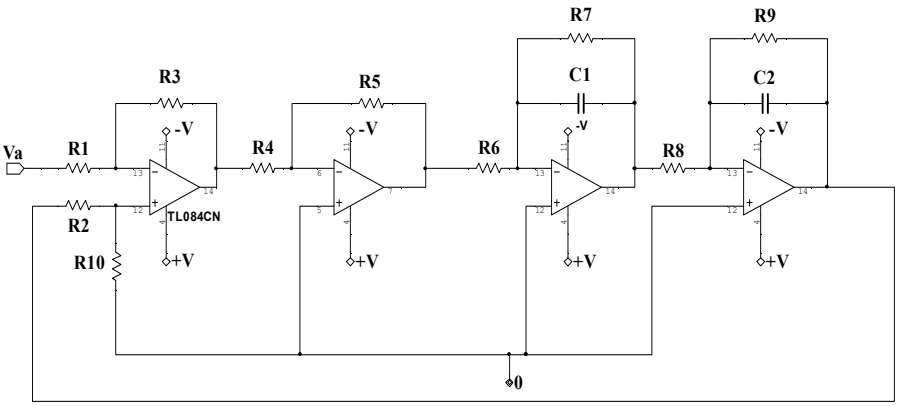


Figure 1. Circuit diagram of DC motor emulator.

2.2. Type A and Type B $PI^{\lambda}D^{\mu}$ Controllers

The block diagram of the controlled DC motor emulator is shown in Figure 2. As mentioned before, the analog implementation of the fractional order $PI^{\lambda}D^{\mu}$ controller is done by two methods: (1) Type A controller, which employs the optimal pole-zero interlacing algorithm [26] for the design of both

fractional integrator and differentiator circuits; and (2) Type B controller–here, the fractional integrator block in Type A controller is replaced by a solid-state fractional capacitor [37] circuit. In the case of Type A controller, for I^{λ} implementation, there are separate circuits for K_i and $s^{-\lambda}$. However, for the I^{λ} circuit of Type B controller, the gain is adjusted by the input potentiometer (R1), as shown in Figure 3.

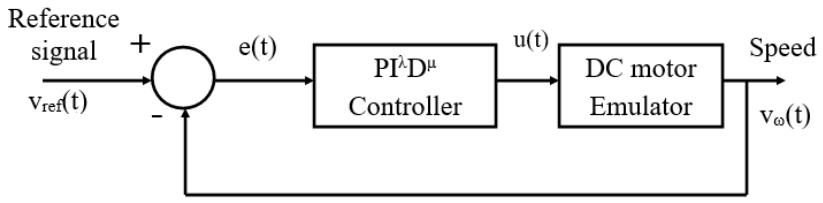


Figure 2. Block diagram of the controlled DC motor emulator.

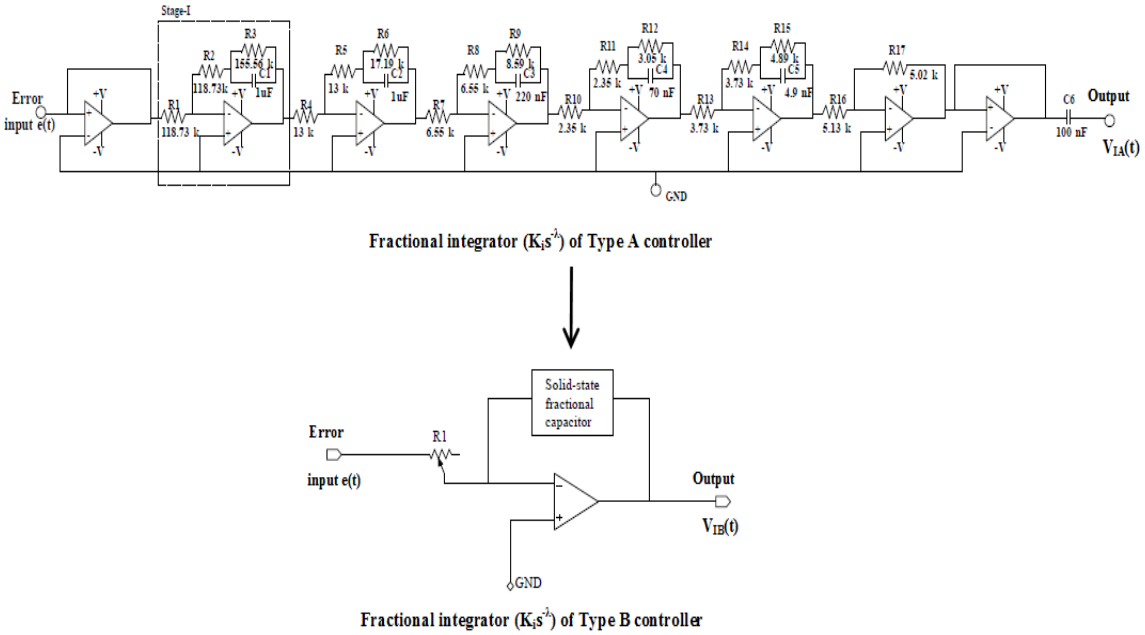


Figure 3. Circuit diagrams of fractional integrator ($K_i s^{-\lambda}$) for Type A and Type B controllers with $\lambda = 0.4$.

In general, the control signal from $PI^{\lambda}D^{\mu}$ controller is given as

$$U(s) = K_p E(s) + \frac{K_i}{s^{\lambda}} E(s) + K_d s^{\mu} E(s) \tag{2}$$

where *U(s)* is the control signal, *E(s)* is the error signal, K_p, K_i and K_d are the proportional, integral and differential gains and λ, μ are the fractional exponents of integrator and differentiator, respectively. The description of Type A controller is provided in Section 2.3, which is followed by Type B controller in Section 2.4.

2.3. Fractional $PI^{\lambda}D^{\mu}$ Controller Using Optimal Pole-Zero Interlacing Algorithm (Type A Controller)

2.3.1. Optimal Pole-Zero Interlacing Algorithm Based Fractional I^{λ} Controller

The optimal pole-zero interlacing algorithm [26] tries to find the rational approximation of the fractional operator in s-domain. It is one of the techniques available in the literature that can be used for the realization of the fractional integral operator. The optimization function used is the rms error of phase angle in the desired band of frequencies and the algorithm tries to find the poles and zeros such

that the phase error is less than 1°. If one uses ladder fractor, then the phase deviation that is obtained will be greater than 1° for 12 resistor and 12 capacitor combination [35].

Now comparing with the other approximation methods like Charef [38], Oustaloup [39] and Xue [19], these methods require a higher order of the polynomial and the phase error obtained is also greater than 1°. Considering the analog realization in [40], it requires three resistors, two capacitors and one op-amp for one pole-zero implementation. For that case, the phase error >1° and the realization have issues in low frequency operation.

Hence, from the above discussion, it can be specified that the order of the optimal pole-zero interlacing algorithm is less when correlated with the other algorithms. Also, in optimal pole-zero analog implementation, it requires three resistors, one op-amp and one capacitor for one pole-zero combination. Thus, it requires fewer components in comparison to the implementation published in [40]. Because of the above advantages, we will use the same for analog implementation of the fractional PID controller.

Next, the approximated transfer function from the optimal pole-zero interlacing algorithm for a fractional integrator with λ = 0.4 which replicates the solid-state fractional capacitor (fabricated by the authors and reported in [41]) is given as:

$$C_{IA}(s) = \frac{(s + 9.64 \times 10^4)(s + 1.077 \times 10^4)(s + 1203)(s + 134.3)(s + 15)}{(s + 4.173 \times 10^4)(s + 4661)(s + 520.5)(s + 58.14)(s + 6.493)} \quad (3)$$

The values of R's and C's for analog implementation of fractional integrator given by Equation (3) is calculated based on the algorithm. It has five stages of pole-zero combination. The analog implementation of the fractional integrator ($K_i s^{-0.4}$) requires 8 op-amps, 17 resistors and 6 capacitors, as shown in Figure 3.

2.3.2. Fractional Differentiator (D^{μ}) Using Optimal Pole-Zero Interlacing Algorithm

The transfer function of fractional differentiator (with μ = 0.4) by the optimal pole-zero interlacing algorithm is:

$$C_{DA}(s) = \frac{(s + 4.173 \times 10^4)(s + 4661)(s + 520.5)(s + 58.14)(s + 6.493)}{(s + 9.64 \times 10^4)(s + 1.077 \times 10^4)(s + 1203)(s + 134.3)(s + 15)} \quad (4)$$

The circuit diagram of the fractional differentiator by optimal pole-zero interlacing algorithm is similar to the fractional integrator circuit but the feedback impedance and input impedance of each stage needs to be interchanged.

2.4. Fractional $PI^{\lambda}D^{\mu}$ Controller Using Solid-State Fractional Capacitor (Type B Controller)

The details of the Type B controller using a solid-state fractional capacitor are provided in [37]. The solid-state fractional capacitor (used in the fractional integrator circuit) has Constant Phase (CP) = $-31.55° \pm 6.75°$ (taken as λ = 0.4) in the frequency range 15 Hz–1 kHz. The fractional differentiator (implemented using optimal pole-zero interlacing algorithm) for this controller will have the same transfer function as in Equation (4) but the K_d will be different.

3. Details of Hardware Implementation

The details of components and instruments employed for the hardware realization are listed below.

1. Type of DC motor emulator: Armature controlled DC motor
2. Op-amp IC used for DC motor emulator and analog $PI^{\lambda}D^{\mu}$ controller: TL084
3. Supply voltage for TL084 IC: ±12 V

4. Reference signal: 1 V_p, 25 Hz square wave signal from an arbitrary function generator (Model number: AFG 3052C, 50 MHz, 1 GS/s)
5. Oscilloscope for capturing output: Lecroy oscilloscope (Model number: Waverunner 604 zi, 400 MHz, 20 G/s).

4. Tuning PI$^{\lambda}$D$^{\mu}$ Controllers

The tuning algorithm mentioned in [37] has been utilized here and is summarized as

1. The Simulink model (in MATLAB 2016b) of the controller DC motor system is generated with an input of 1 V.
2. We define the step response requirements in "Check Response Characteristics" block of MATLAB with rise time <1.98 ms, settling time <13 ms and overshoot ≤12%.
3. The variable set is designed with K_p = [0,10], K_i = [0,200] and K_d = [0,10]. These values are the maximum gains from the analog circuit of PI$^{\lambda}$D$^{\mu}$ controller, which provides a stable output.
4. Once the model is created, the pattern search optimization method [42] is run to obtain the tuned parameters K_p, K_i and K_d for Type A and Type B controllers.

The parameters of Type A controller are obtained by the above algorithm. The tuning technique provides the optimal values of the parameters satisfying the time domain specifications: rise time <1.98 ms, settling time <13 ms and overshoot ≤12%.

5. Results and Discussion

The fractional integrator circuit obtained by optimal pole-zero interlacing algorithm has a constant phase angle of $-34.5 \pm 1.40^{\circ}$ in the frequency range of 10 Hz to 1 kHz. Whereas, for the fractional differentiator, the constant phase angle is $31.48 \pm 2.31^{\circ}$ in the frequency range from 10 Hz to 900 Hz (from the hardware implemented D$^{\mu}$ circuit). The tuning algorithm mentioned in Section 4 is run to get the values of controller parameters. For Type A controller [K_p, K_i, K_d] = [3.45, 66.06, 1.67]; and the values for the Type B controller are [K_p, K_i, K_d] = [3.45, 165.95, 2.52]. For both the controllers, it is assumed that $\lambda = \mu = 0.4$ as the hardware results shown in [37] are having the above-mentioned values for λ and μ. The final control signal by Type A controller is given as:

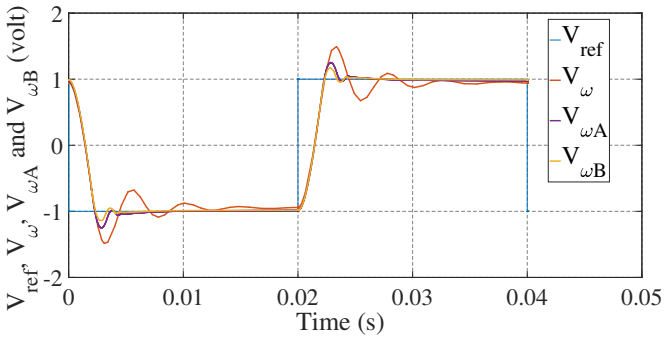
$$U_A(s) = 3.45 + \frac{66.06}{s^{0.4}} + 1.67s^{0.4} \tag{5}$$

whereas, the control signal by the Type B controller is as below:

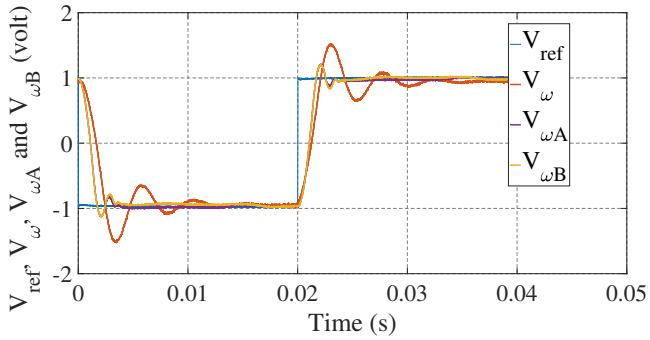
$$U_B(s) = 3.45 + \frac{165.95}{s^{0.4}} + 2.52s^{0.4} \tag{6}$$

There is a difference in the K_i and K_d values (in Equations (5) and (6)) as the solid-state fractional capacitor is matching only the phase characteristics of the fractional integrator circuit by the optimal pole-zero interlacing algorithm and there is a difference in their impedance characteristics, which have caused the change in the controller gain values.

With the above-designed controllers, a square wave reference signal (V_{ref} = 1 V_p, 25 Hz) is given to a cascaded fractional PI$^{\lambda}$D$^{\mu}$ controlled DC motor emulator and the simulated as well as the real time response graphs are plotted. The simulation (using Multisim) and experimental results for Type A and Type B controlled DC motor emulator are shown in Figure 4, and the corresponding performance metrics are tabulated in Table 1.



(**a**) Simulation results from Multisim.



(**b**) Experimental results from hardware setup.

Figure 4. Comparison of results. V_{ref} = reference signal, V_{ω} = DC motor response, $V_{\omega A}$ = response from Type A controlled DC motor and $V_{\omega B}$ = response from Type B controlled DC motor.

Table 1. Performance measures (in time domain) of the controlled DC motor obtained in simulation (Multisim) and experimental setup.

Controller Type	% Overshoot	T_r (Rise Time)	T_s (Settling Time)	SS Error
		Multisim		
DC motor	28.5%	1.79 ms	13.8 ms	54.2 mV
Type A controller	13.4%	0.8 ms	6.02 ms	23.1 mV
Type B controller	7.4%	0.8 ms	4.55 ms	16.3 mV
		Experimental		
DC motor	31.1%	1.9 ms	16.9 ms	67 mV
Type A controller	11.78%	0.580 ms	6.8 ms	12.4 mV
Type B controller	11%	0.58 ms	4.6 ms	12 mV

The simulation results are showing that Type B controller is better in terms of % overshoot, settling time and steady state error (SS error). Whereas, from the experimental results, it is apparent that the performance measures of Type A controller and Type B controllers are comparable. The difference between the simulation and the hardware results are due to the tolerance of the components used in the hardware.

5.1. Discussion on the Fractional $PI^{\lambda}D^{\mu}$ Controller Designed by Pole-Zero Interlacing Algorithm

5.1.1. Fractional Integration of Type A Controller

The fractional integral action on the error signal for Type A controller is graphically shown in Figure 5 (the zoomed version of the error signal is at the right bottom of the figure). The details of the fractional integral action considering error voltage in each section (0-A, A-B, B-C) as sine waves are tabulated in Table 2.

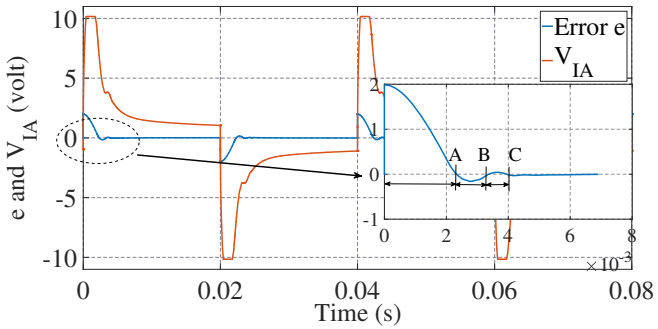


Figure 5. Error voltage (e) and $K_i I^{\lambda}$ voltage (V_{IA}) of Type A controller.

Table 2. Details of fractional integration and fractional differentiation of Type A controller.

Section	Frequency (Hz)	Calculated Gain	e	V_{IA}/V_{DA}	Actual Gain	Phase (in deg)
Fractional Integration (V_{IA})						
0-A	106	5.63	2 V_p	10.44 V_p	5.24	−33
A-B	1000	2.83	155 mV_p	548 mV_p	3.53	−33
B-C	1500	1.87	35 mV_p	106 mV_p	3.08	−35.6
Fractional Differentiation (V_{DA})						
0-A	106	17.34	2 V_p	10.44 V_p	5.09	33
A-B	1000	33.22	155 mV_p	4.5 V_p	32.2	30.9
B-C	1500	33.8	35 mV_p	1.26 V_p	36.11	29.7

From point C to t = 0.02 s, the output of the fractional integrator is illustrated by Figure 5 as in that range, the error is not sinusoidal. The algorithm mentioned in Section 4 tries to find the gain K_i so that the output from the fractional integrator has a value of around 1 V (as we are giving V_{ref} = 1 V) at half the time period of the input signal.

The calculated gain (Table 2) is the ideal case and is not dependent on input amplitude with its value equal to $K_i \times (2 \times 3.14 \times f)^{-\lambda}$. However, actual gain is influenced by the input amplitude and saturation limit of the op-amp. For instance, if the gain is 5.63, for an input of 2 V_p, the output amplitude should be 11.26 V_p and cannot be obtained in this case as the output is bounded to $\pm$10.44 V_p (the op-amp used to implement the circuit saturates at $\pm$10.44 V_p). So, for each case, the actual gain will not be equal to the ideal gain of the fractional integrator. It has been observed that with increase in frequency, the calculated gain as well as the actual gain decreases.

5.1.2. Fractional Differentiation of Type A Controller

The fractional derivative action on the error signal is shown in Figure 6; and the details of the fractional differentiation considering error voltage in each section (0-A, A-B, B-C) as sine waves are given in Table 2. From point C to t = 0.02 s, the output of the fractional differentiator is graphically shown in Figure 6.

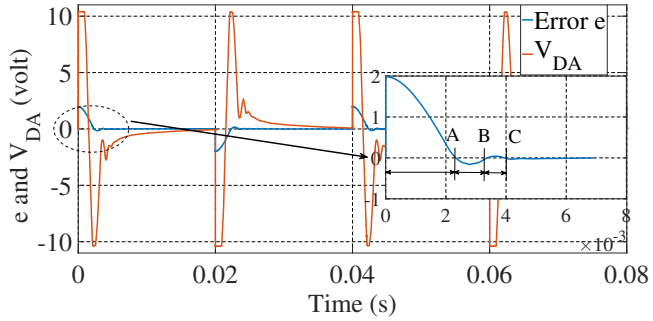


Figure 6. Error voltage (e) and $K_d \mathrm{D}^{\mu}$ voltage (V_{DA}) of Type A controller.

For the fractional differentiator also, the computed gain and the experimental gain are listed in Table 2. The calculation of gain from a fractional differentiator is given by $K_d \times (2 \times 3.14 \times f)^{\mu}$ and it is unrelated with input amplitude and saturation limit. However, experimental gain has an influence from input amplitude as mentioned above. Due to which, the calculated gain and actual gain will not be the same. The value of gain increases with increase in frequency for both the calculated gain and the actual gain, that is, it follows the frequency characteristics of the differentiator.

The final controller output, which is the summation of controller efforts from the proportional, fractional integrator and fractional differentiator, will be given to the DC motor emulator. It is mentioned in Section 2 that the DC motor emulator has one gain stage and two integrators (see Figure 1). From Figure 7, we can see that the output from the gain stage of the DC motor (V_G) is the square wave of small intervals, which makes the integrator-1 output (V_{I1}) to charge to a lower voltage and the output of integrator-2 ($V_{\omega A}$) has a minor overshoot; hence making the output value close to 1 V. The short interval square wave is produced from the fractional controller. Also, the saturation element in the fractional controller and the DC motor emulator has an effect on reducing the % overshoot of the DC motor. Whereas, the fractional integrator tries to reduce the steady state error in the speed response.

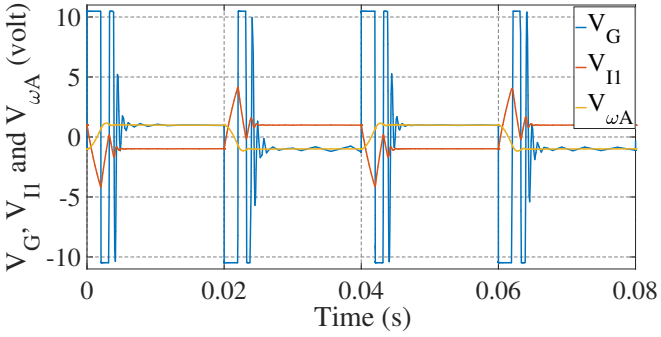


Figure 7. Gain stage output (V_G), Integrator-1 output (V_{I1}) and Integrator-2 output ($V_{\omega A}$) of a DC motor with Type A controller.

The comparison results show that the performance measures are almost the same for Type A and Type B controller but the number of components can be greatly reduced if one uses a Type B controller (which employs the solid-state fractional capacitors). As mentioned before, the number of components required for implementing fractional integrator (including K_i gain block) in Type A controller are: 8 op-amps, 17 resistors and 6 capacitors and the fractional integrator in Type B controller requires: one op-amp, one resistor and the solid-state fractional capacitor. From Table 1, it can be seen that the performance of the DC motor has improved (decrease in T_s, % overshoot and steady state (SS) error) when employing fractional $\mathrm{P}I^{\lambda}D^{\mu}$ controllers.

6. Conclusions

In this paper, performance comparison of two types of analog PI$^{\lambda}$D$^{\mu}$ controllers implemented in hardware and tested on a DC motor emulator is presented. Type B controller uses a solid-state fractional capacitor in the fractional integrator circuit and this controller has an advantage over Type A controller by reducing the number of components in the hardware implementation; but both the controllers' performance measures are comparable. Hence, this study shows that if one does not have a single component fractional capacitor, then also the same performance can be attained using the optimal pole-zero interlacing technique. Apart from the above, it also validates the applicability of the tuning algorithm for Type A controller, which was developed for the Type B controller by the authors in their earlier work. As a future work, the fractional PI$^{\lambda}$D$^{\mu}$ controllers can be implemented on other systems employing the tuning algorithm proposed and also comparison studies with a digital controller. In addition, analog implementation of PI$^{\lambda}$D$^{\mu}$ controllers with other components, which reduces the circuit complexity, needs to be explored.

Author Contributions: D.A.J. and S.S. implemented the hardware circuit for fractional PI$^{\lambda}$D$^{\mu}$ controller and the DC motor emulator and then carried out the experiment to measure the time domain performance measures of the controlled DC motor emulator. The experiments were done under the supervision of K.B. The initial draft of the paper was written by D.A.J.; review and editing were done by K.B. and S.S. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Acknowledgments: This article is based upon work of European "COST Action CA15225", which is on "Fractional-order systems: analysis, synthesis and their importance for future design". The authors would like to thank M. V. Aware and Swapnil Khulbalkar of VNIT Nagpur, India, for their valuable suggestions.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Astrom, K.J.; Hagglund, T. *PID Controllers: Theory, Design and Tuning*; Instrument Society of America: Research Triangle, NC, USA, 1995.
2. Astrom, K.; Hagglund, T. The future of PID control. *Control. Eng. Pract.* **2001**, *9*, 1163–1175. [CrossRef]
3. Podlubny, I.; Petráš, I.; Vinagre, B.M.; O'Leary, P.; Dorčák, L'. Analogue Realizations of Fractional-Order Controllers. *Nonlinear Dyn.* **2002**, *29*, 281–296. [CrossRef]
4. Zhao, C.; Xue, D.; Chen, Y. A fractional order PID tuning algorithm for a class of fractional order plants. In Proceedings of the IEEE International Conference Mechatronics and Automation, Niagara Falls, ON, Canada, 29 July–1 August 2005; Volume 1, pp. 216–221.
5. Valério, D.; da Costa, J.S. Tuning of Fractional PID Controllers with Ziegler-Nichols-type Rules. *Signal Process.* **2006**, *86*, 2771–2784. [CrossRef]
6. Monje, C.; Vinagre, B.; Feliu, V.; Chen, Y. Tuning and auto-tuning of fractional order controllers for industry applications. *Control. Eng. Pract.* **2008**, *16*, 798–812. [CrossRef]
7. Chen, Y.; Bhaskaran, T.; Xue, D. Practical Tuning Rule Development for Fractional Order Proportional and Integral Controllers. *J. Comput. Nonlinear Dyn.* **2008**, *3*, 021403. [CrossRef]
8. Biswas, A.; Das, S.; Abraham, A.; Dasgupta, S. Design of fractional-order $PI^{\lambda}D^{\mu}$ controllers with an improved differential evolution. *Eng. Appl. Artif. Intell.* **2009**, *22*, 343–350. [CrossRef]
9. Ahn, H.; Bhambhani, V.; Chen, Y. Fractional-order integral and derivative controller for temperature profile tracking. *Sadhana Acad. Proc. Eng. Sci.* **2009**, *34*, 833–850. [CrossRef]
10. Tepljakov, A.; Petlenkov, E.; Belikov, J. FOMCON: A MATLAB toolbox for fractional-order system identification and control. *Int. J. Microelectron. Comput. Sci.* **2011**, *2*, 51–62.
11. Pan, I.; Das, S. Chaotic multi-objective optimization based design of fractional order $PI^{\lambda}D^{\mu}$ controller in AVR system. *Int. J. Electr. Power Energy Syst.* **2012**, *43*, 393–407. [CrossRef]
12. Das, S.; Pan, I.; Das, S.; Gupta, A. Improved model reduction and tuning of fractional-order $PI^{\lambda}D^{\mu}$ controllers for analytical rule extraction with genetic programming. *ISA Trans.* **2012**, *51*, 237–261. [CrossRef]
13. Caponetto, R. Auto-Tuning and Fractional Order Controller Implementation on Hardware in the Loop System. *J. Optim. Theory Appl.* **2013**, *156*, 141–152. [CrossRef]

14. Caponetto, R.; Dongola, G. A numerical approach for computing stability region of FO-PID controller. *J. Frankl. Inst.* **2013**, *350*, 871–889. [CrossRef]
15. Oustaloup, A. *Diversity and Non-Integer Differentiation for System Dynamics*; Wiley-ISTE: London, UK, 2014.
16. Caponetto, R.; Dongola, G.; Maione, G.; Pisano, A. Integrated technology fractional order proportional-integral-derivative design. *J. Vib. Control* **2014**, *20*, 1066–1075. [CrossRef]
17. Sabatier, J.; Lanusse, P.; Melchior, P.; Oustaloup, A. *Fractional Order Differentiation and Robust Control Design: CRONE, H-Infinity and Motion Control*; Springer: Berlin, Germany, 2015.
18. Shah, P.; Agashe, S. Review of fractional PID controller. *Mechatronics* **2016**, *38*, 29–41. [CrossRef]
19. Xue, D.; Zhao, C.; Chen, Y. Fractional order PID control of a DC-motor with elastic shaft: A case study. In Proceedings of the 2006 American Control Conference, Minneapolis, MN, USA, 14–16 June 2006; p. 6.
20. Petráš, I. Fractional-Order feedback control of a DC motor. *J. Electr. Eng.* **2009**, *60*, 117–128.
21. Mehra, V.; Srivastava, S.; Varshney, P. Fractional-order PID controller design for speed control of DC motor. In Proceedings of the 2010 3rd International Conference on Emerging Trends in Engineering and Technology, Goa, India, 19–21 November 2010; pp. 422–425.
22. Lazarević, M.P.; Batalov, S.A.; Latinović, T.S. Fractional PID Controller Tuned by Genetic Algorithms for a Three DOF's Robot System Driven by DC motors. *IFAC Proc. Vol.* **2013**, *46*, 385–390. [CrossRef]
23. Roy, A.; Srivastava, S. Design of optimal $PI^{\lambda}D^{\mu}$ controller for speed control of DC motor using constrained particle swarm optimization. In Proceedings of the IEEE International Conference on Circuit, Power and Computing Technologies, ICCPCT 2016, Kumaracoil, India, 18–19 March 2016.
24. Viola, J.; Angel, L.; Sebastian, J. Design and robust performance evaluation of a fractional order PID controller applied to a DC motor. *IEEE/CAA J. Autom. Sin.* **2017**, *4*, 304–314. [CrossRef]
25. Jain, R.V.; Aware, M.; Junghare, A. Tuning of Fractional Order PID controller using particle swarm optimization technique for DC motor speed control. In Proceedings of the 2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), Delhi, India, 4–6 July 2016; pp. 1–4.
26. Aware, M.; Junghare, A.; Khubalkar, S.; Dhabale, A.; Das, S.; Dive, R. Design of new practical phase shaping circuit using optimal pole-zero interlacing algorithm for fractional order PID controller. *Analog. Integr. Circuits Signal Process.* **2017**, *91*, 131–145. [CrossRef]
27. Dimeas, I.; Petráš, I.; Psychalinos, C. New analog implementation technique for fractional-order controller: A DC motor control. *AEU Int. J. Electron. Commun.* **2017**, *78*, 192–200. [CrossRef]
28. Kumar, A.; Kumar, V. Hybridized ABC-GA optimized fractional order fuzzy pre-compensated FOPID control design for 2-DOF robot manipulator. *AEU Int. J. Electron. Commun.* **2017**, *79*, 219–233. [CrossRef]
29. John, D.A.; Biswas, K. Analysis of disturbance rejection by PI^{λ} controller using solid state fractional capacitor. In Proceedings of the 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 27–30 May 2018; pp. 1–5.
30. Kapoulea, S.; Psychalinos, C.; Petráš, I. Simple Design of Fractional-Order DC Motor Controller. In Proceedings of the 2019 6th International Conference on Control, Decision and Information Technologies (CoDIT), Paris, France, 23–26 April 2019; pp. 867–871.
31. Herencsar, N.; Kartci, A.; Koton, J.; Sotner, R.; Alagoz, B.B.; Yeroglu, C. Analogue Implementation of a Fractional-PI^{λ} Controller for DC Motor Speed Control. In Proceedings of the 2019 IEEE 28th International Symposium on Industrial Electronics (ISIE), Vancouver, BC, Canada, 12–14 June 2019; pp. 467–472.
32. Copot, C.; Muresan, C.; Ionescu, C.M.; De Keyser, R. Fractional order control of a DC motor with load changes. In Proceedings of the 2014 International Conference on Optimization of Electrical and Electronic Equipment (OPTIM), Brasov, Romania, 22–24 May 2014; pp. 956–961.
33. Lino, P.; Maione, G.; Stasi, S.; Padula, F.; Visioli, A. Synthesis of fractional-order PI controllers and fractional-order filters for industrial electrical drives. *IEEE/CAA J. Autom. Sin.* **2017**, *4*, 58–69. [CrossRef]
34. Villagra, J.; Vinagre, B.; Tejado, I. Data-driven fractional PID control: Application to DC motors in flexible joints. *IFAC Proc. Vol.* **2012**, *45*, 709–714. [CrossRef]
35. Adhikary, A.; Sen, P.; Sen, S.; Biswas, K. Design and Performance Study of Dynamic Fractors in Any of the Four Quadrants. *Circuits Syst. Signal Process.* **2016**, *35*, 1909–1932. [CrossRef]
36. John, D.A.; Banerjee, S.; Biswas, K. A CNT-Epoxy Nanoparticle Based Fractional Capacitor and a Method for Fabricating the Same. Patent Application No. 20,163,1042,210, 15 June 2018.

37. John, D.A.; Aware, M.V.; Junghare, A.S.; Biswas, K. Performance Analysis of Solid-State Fractional Capacitor-Based Analog PI$^{\lambda}$D$^{\mu}$ Controller. *Circuits Syst. Signal Process.* **2020**, *39*, 1815–1830. [CrossRef]
38. Charef, A. Analogue realisation of fractional-order integrator, differentiator and fractional PI/spl lambda/D/spl mu/ controller. *IEE Proc. Control Theory Appl.* **2006**, *153*, 714–720. [CrossRef]
39. Oustaloup, A.; Levron, F.; Mathieu, B.; Nanot, F. Frequency-band complex noninteger differentiator: Characterization and synthesis. *IEEE Trans. Circuits Syst. Fundam. Theory Appl.* **2000**, *47*, 25–39. [CrossRef]
40. Khanra, M.; Pal, J.; Biswas, K. Rational Approximation and Analog Realization of Fractional Order Transfer Function with Multiple Fractional Powered Terms. *Asian J. Control* **2013**, *15*, 723–735. [CrossRef]
41. John, D.A.; Banerjee, S.; Bohannan, G.W.; Biswas, K. Solid-state fractional capacitor using MWCNT-epoxy nanocomposite. *Appl. Phys. Lett.* **2017**, *110*, 163504. [CrossRef]
42. Simulink Design Optimization. Available online: http://www.apmath.spbu.ru/ru/staff/smirnovmn/files/sldo_ug.pdf/ (accessed on 26 June 2020).