• Bit 2:0 - CSn2:0: Clock Select

The three clock select bits select the clock source to be used by the Timer/Counter, see Figure 17-10 and Figure 17-11 on page 152.

Table 17-6. Clock Select Bit Description

CSn2	CSn1	CSn0	Description
0	0	0	No clock source. (Timer/Counter stopped)
0	0	1	clk _{I/O} /1 (No prescaling
0	1	0	clk _{I/O} /8 (From prescaler)
0	1	1	clk _{I/O} /64 (From prescaler)
1	0	0	clk _{I/O} /256 (From prescaler)
1	0	1	clk _{I/O} /1024 (From prescaler)
1	1	0	External clock source on Tn pin. Clock on falling edge
1	1	1	External clock source on Tn pin. Clock on rising edge

If external pin modes are used for the Timer/Countern, transitions on the Tn pin will clock the counter even if the pin is configured as an output. This feature allows software control of the counting.

17.11.9 TCCR1C - Timer/Counter 1 Control Register C

Bit	7	6	5	4	3	2	1	0	
(0x82)	FOC1A	FOC1B	FOC1C	-	-	-	-	-	TCCR1C
Read/Write	W	W	W	R	R	R	R	R	_
Initial Value	0	0	0	0	0	0	0	0	

17.11.10 TCCR3C - Timer/Counter 3 Control Register C

Bit	7	6	5	4	3	2	1	0	
(0x92)	FOC3A	FOC3B	FOC3C	-	-	-	-	-	TCCR3C
Read/Write	W	W	W	R	R	R	R	R	_
Initial Value	0	0	0	0	0	0	0	0	

17.11.11 TCCR4C - Timer/Counter 4 Control Register C

Bit	7	6	5	4	3	2	1	0	
(0xA2)	FOC4A	FOC4B	FOC4C	-	-	_	-	-	TCCR4C
Read/Write	W	W	W	R	R	R	R	R	-
Initial Value	0	0	0	0	0	0	0	0	

17.11.12 TCCR5C - Timer/Counter 5 Control Register C

Bit	7	6	5	4	3	2	1	0	
(0x122)	FOC5A	FOC5B	FOC3C	-	-	-	-	-	TCCR5C
Read/Write	W	W	W	R	R	R	R	R	_
Initial Value	0	0	0	0	0	0	0	0	

- Bit 7 FOCnA: Force Output Compare for Channel A
- Bit 6 FOCnB: Force Output Compare for Channel B
- Bit 5 FOCnC: Force Output Compare for Channel C

The FOCnA/FOCnB/FOCnC bits are only active when the WGMn3:0 bits specifies a non-PWM mode. When writing a logical one to the FOCnA/FOCnB/FOCnC bit, an immediate compare match is forced on the waveform generation unit. The OCnA/OCnB/OCnC output is changed according to its COMnx1:0 bits setting. Note that the

