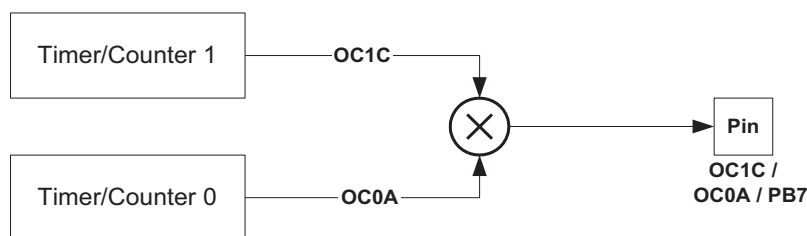


19. Output Compare Modulator (OCM1C0A)

19.1 Overview

The Output Compare Modulator (OCM) allows generation of waveforms modulated with a carrier frequency. The modulator uses the outputs from the Output Compare Unit C of the 16-bit Timer/Counter1 and the Output Compare Unit A of the 8-bit Timer/Counter0. For more details about these Timer/Counters see “[Timer/Counter 0, 1, 3, 4, and 5 Prescaler](#)” on page 164 and “[8-bit Timer/Counter2 with PWM and Asynchronous Operation](#)” on page 169.

Figure 19-1. Output Compare Modulator, Block Diagram



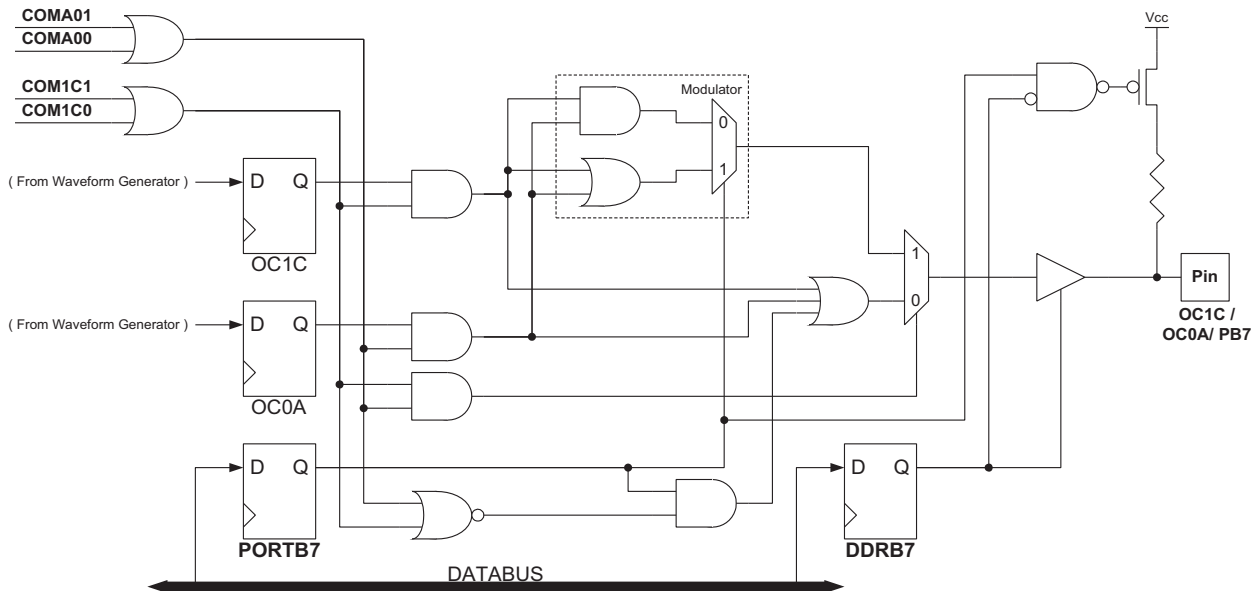
When the modulator is enabled, the two output compare channels are modulated together as shown in the block diagram (see [Figure 19-1](#)).

19.2 Description

The Output Compare unit 1C and Output Compare unit 2 shares the PB7 port pin for output. The outputs of the Output Compare units (OC1C and OC0A) overrides the normal PORTB7 Register when one of them is enabled (that is, when COMnx1:0 is not equal to zero). When both OC1C and OC0A are enabled at the same time, the modulator is automatically enabled.

The functional equivalent schematic of the modulator is shown on [Figure 19-2](#). The schematic includes part of the Timer/Counter units and the port B pin 7 output driver circuit.

Figure 19-2. Output Compare Modulator, Schematic

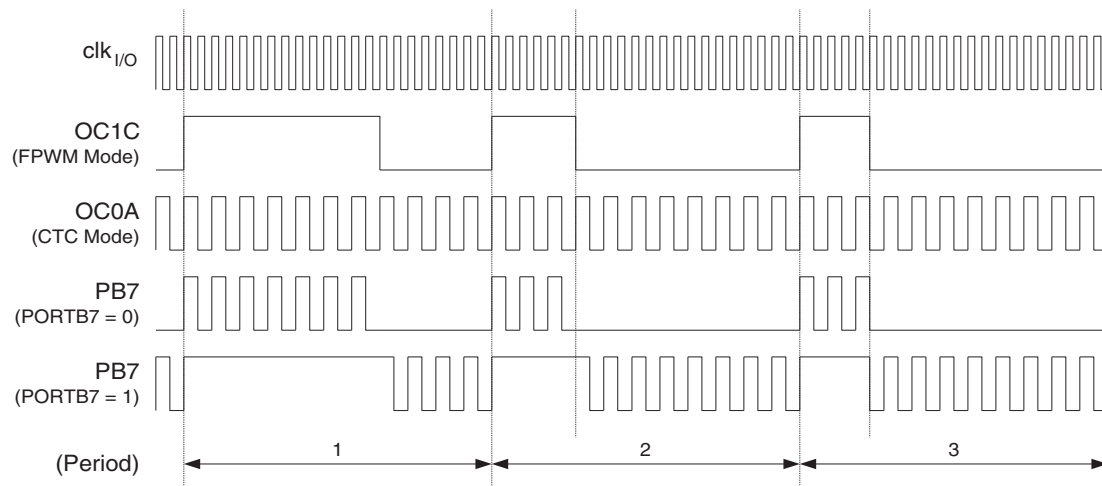


When the modulator is enabled the type of modulation (logical AND or OR) can be selected by the PORTB7 Register. Note that the DDRB7 controls the direction of the port independent of the COMnx1:0 bit setting.

19.2.1 Timing example

Figure 19-3 illustrates the modulator in action. In this example the Timer/Counter1 is set to operate in fast PWM mode (non-inverted) and Timer/Counter0 uses CTC waveform mode with toggle Compare Output mode (COMnx1:0 = 1).

Figure 19-3. Output Compare Modulator, Timing Diagram



In this example, Timer/Counter2 provides the carrier, while the modulating signal is generated by the Output Compare unit C of the Timer/Counter1.

The resolution of the PWM signal (OC1C) is reduced by the modulation. The reduction factor is equal to the number of system clock cycles of one period of the carrier (OC0A). In this example the resolution is reduced by a factor of two. The reason for the reduction is illustrated in Figure 19-3 at the second and third period of the PB7 output when PORTB7 equals zero. The period 2 high time is one cycle longer than the period 3 high time, but the result on the PB7 output is equal in both periods.