The Design of a Low-Voltage Bandgap Reference Report

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Abstract. Most integrated circuits incorporate bandgap references to define certain dc voltages or currents that serve various building blocks. In this report, we design the circuit in 180-nm CMOS technology which meets the specifications in Table1.

Table 1. Circuit Specification

0.18um Virtual Process	
Single supply voltage	$1.5V \pm 10\%$
Output voltage	$0.4 \sim 0.5V$
Output voltage variation	<5mV from 0°C to 100°C
Power supply rejection ratio	>40dB
Power	<2mW

(a) Design Procedure

We use bandgap circuit with regulated cascode [see Figure 1] introduced in paper to complete the design. However, due to different fabrication technology and specification, we need to adjust the parameters of each components.

Two-stage op amp design

The two-stage op amp A_1 and A_2 [see Figure 1 and 2] designed in paper are wrong due to the fact that the first stage amp output is not connected to the second stage amp. Therefore, we use two-stage op amp design in Figure 3 instead.

Due to 0.18um CMOS fabrication, we select $(W/L)_{1,2}$ = 75μm / 0.18μm, R_a = R_b = 40kΩ, and I_{SS} = 50μA. After adjusting the circuit, total gain of two-stage op amp is enough for limiting $V_X = V_Y$, providing more accurate result.

Overall bandgap reference circuit design

After designing two-stage op amp, we only need to choose the dimensions of the transistors. For the PMOS transistors, the channel area must be large enough to minimize mismatch and flicker noise, and the length must be long enough to ensure that channel-length modulation does not limit the supply rejection. Based on these considerations, we select $(W/L)_{1,2}$ = 100μm / 0.32μm. Noticed that all the transistors in the circuit must connect its source to its body to avoid body effect.

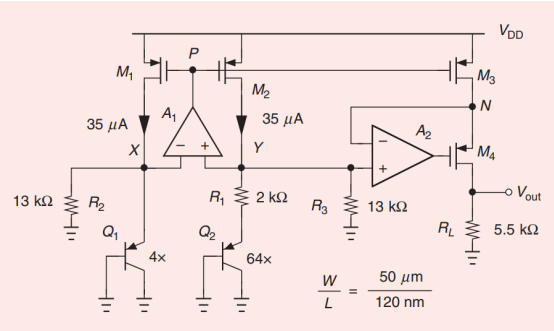

Figure 1. Bandgap circuit with a regulated cascode

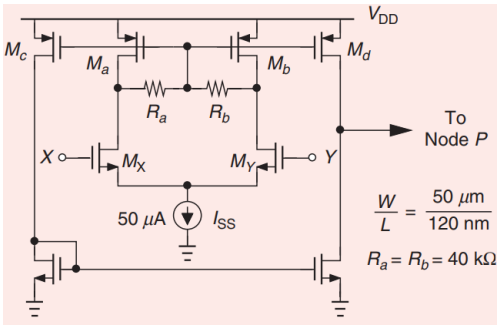

Figure 2. Original two-stage op amp design

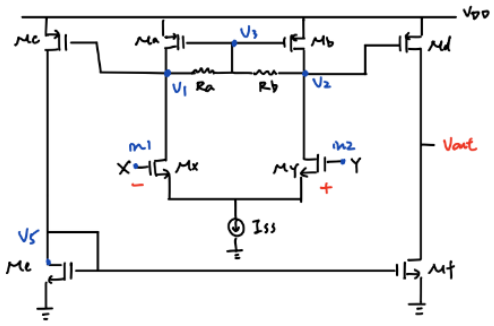

Figure 3. Two-stage op amp design

However, the simulation output voltage variation is still larger than 5mV. To address this problem, we first think about the voltage at the output

$$V_{out} = \frac{R_L}{R_3}\left(\frac{R_3}{R_1} V_T \ln n + |V_{BE}|\right) \tag{1}$$

to generate a voltage that is nominally independent of the temperature, we obtain

$$\frac{R_3}{R_1}\frac{\partial V_T}{\partial T} \ln n + \frac{\partial |V_{BE}|}{\partial T} = 0 \tag{2}$$

therefore, we focus on adjusting the dimensions of bipolar transistors and the value of resistance. We choose R_1 = 2kΩ, $R_2 = R_3$ = 13kΩ, R_L = 4.8kΩ, 4 units transistors for Q_1 and 67 units transistors for Q_2.

(b) Simulation Result

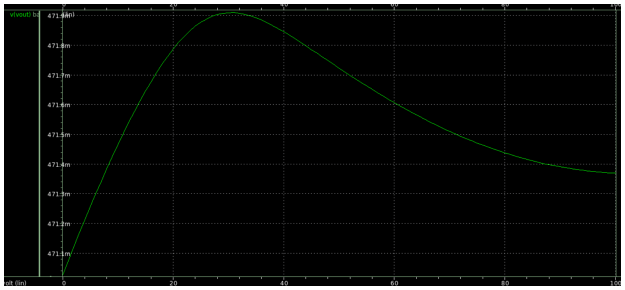

Figure 4. Output volatage when VDD = 1.5V

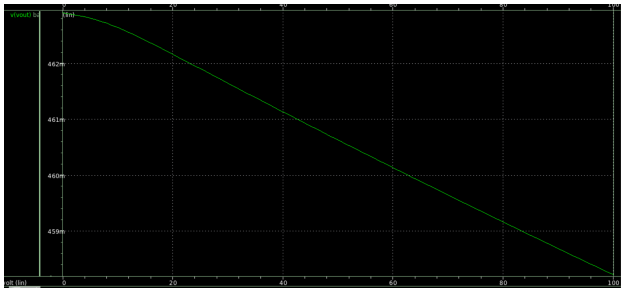

Figure 5. Output volatage when VDD = 1.35V

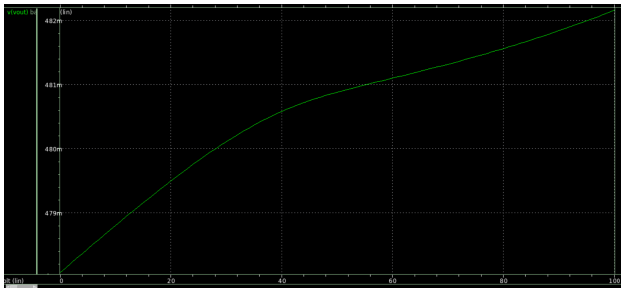

Figure 6. Output volatage when VDD = 1.65V

The results [see Figure 4, 5 and 6] show that even if supply voltage varies with ±10%, the output voltage variation is still smaller than 5mV from 0°C to 100°C and within the range (0.4V, 0.5V), which meets the specification in Table 1.

```
**** voltage sources

subckt
element  0:vdd
 volts      1.5000
 current -797.0908u
 power      1.1956m

    total voltage source power dissipation=    1.1956m       watts
```

Figure 7. Power consumption when VDD = 1.5V

```
**** voltage sources

subckt
element  0:vdd
 volts      1.6500
 current -654.8286u
 power      1.0805m

    total voltage source power dissipation=    1.0805m       watts
```

Figure 8. Power consumption when VDD = 1.65V

```
**** voltage sources

subckt
element  0:vdd
 volts      1.3500
 current   -1.3714m
 power      1.8513m

    total voltage source power dissipation=    1.8513m       watts
```

Figure 9. Power consumption when VDD = 1.35V

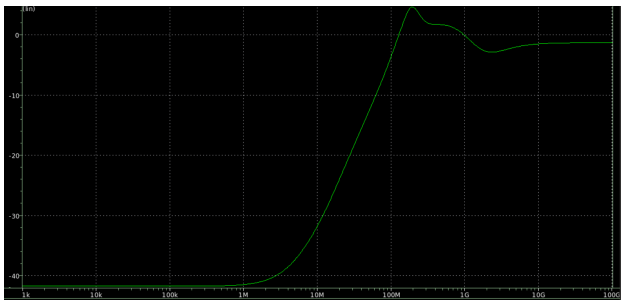

Figure 10. Power supply rejection ratio

The results [see Figure 7, 8, 9 and 10] show that with voltage variations, power consumption and PSRR still meet the specification in Table1.