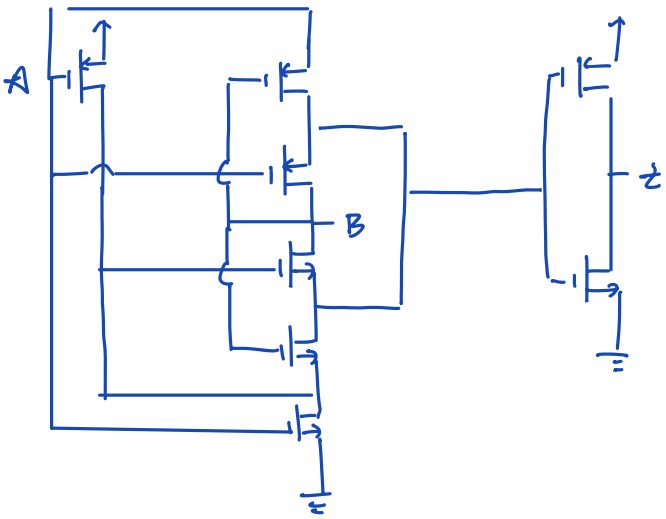
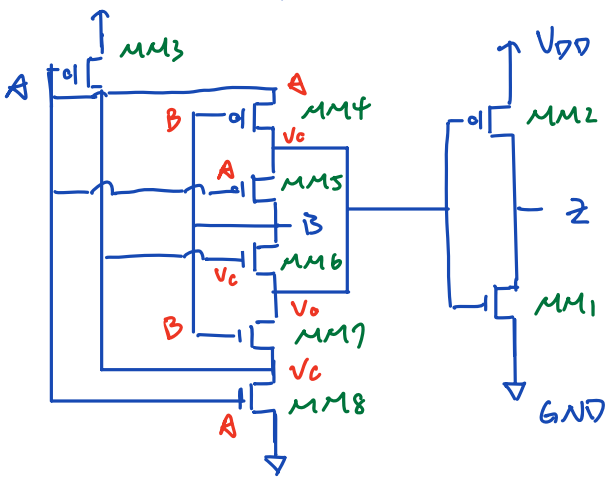
1. (a) EN

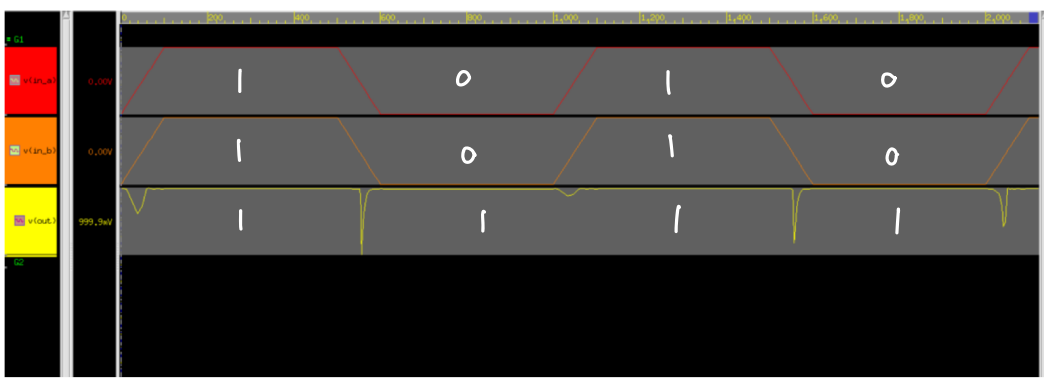


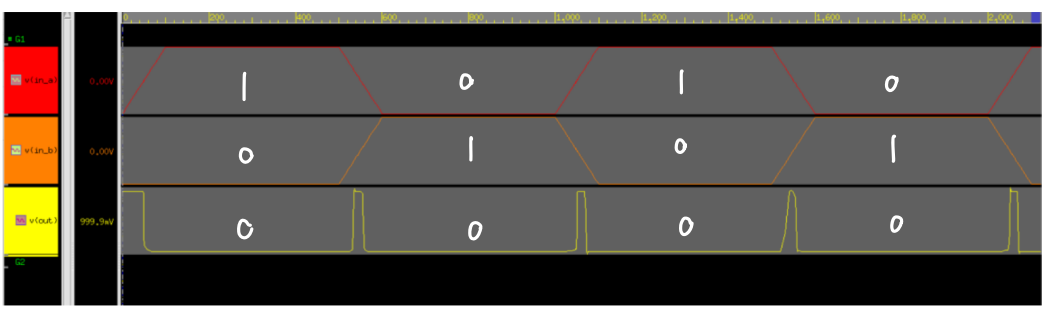
transistor - level diagrams :



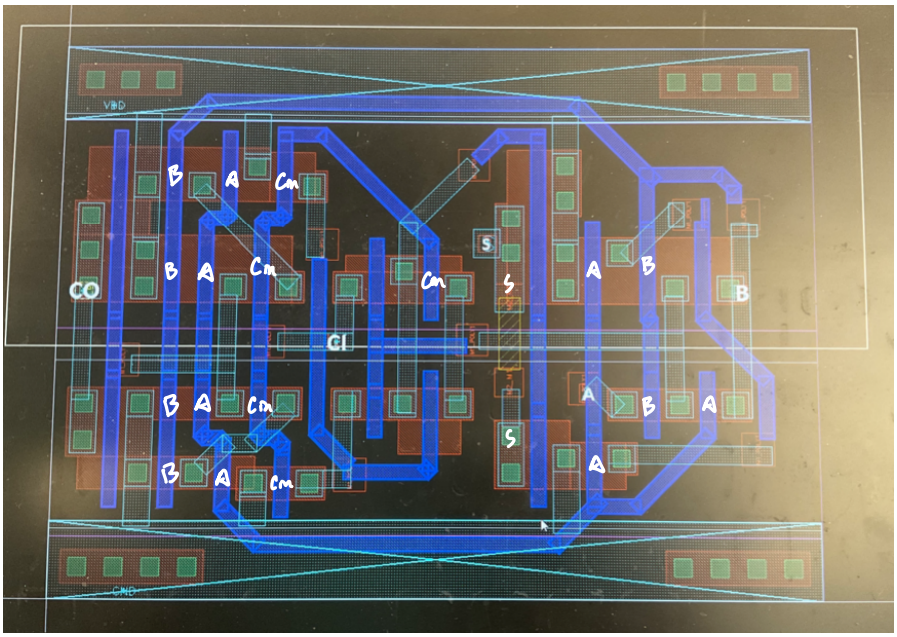
truth table :

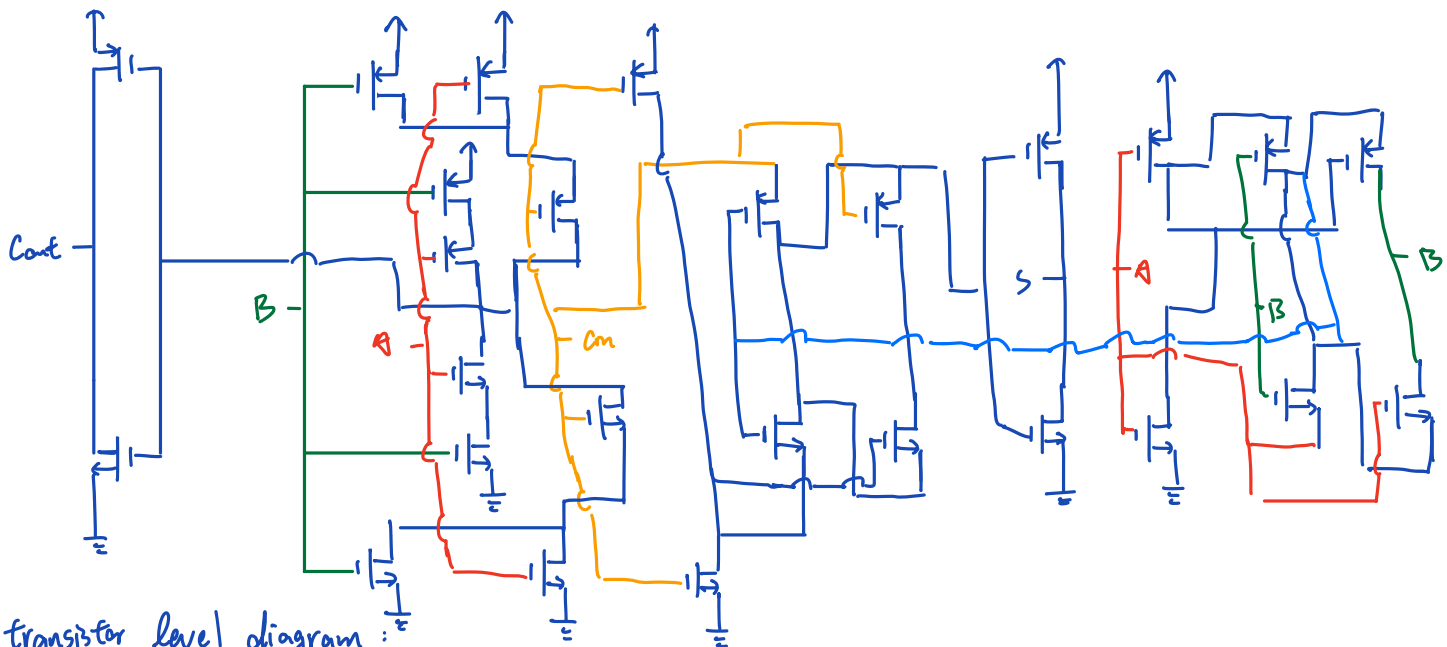
A	B	Z
0	0	1
0	1	0
1	0	0
1	1	1



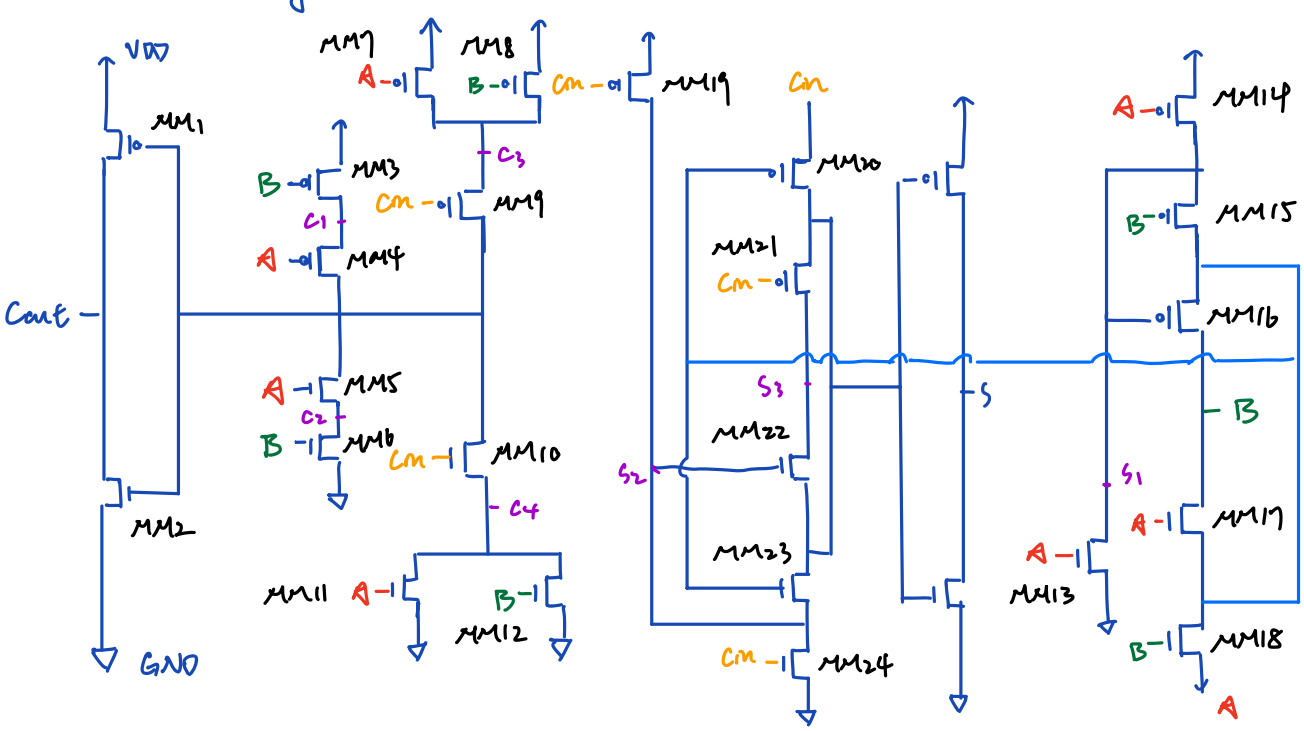


(b) FA



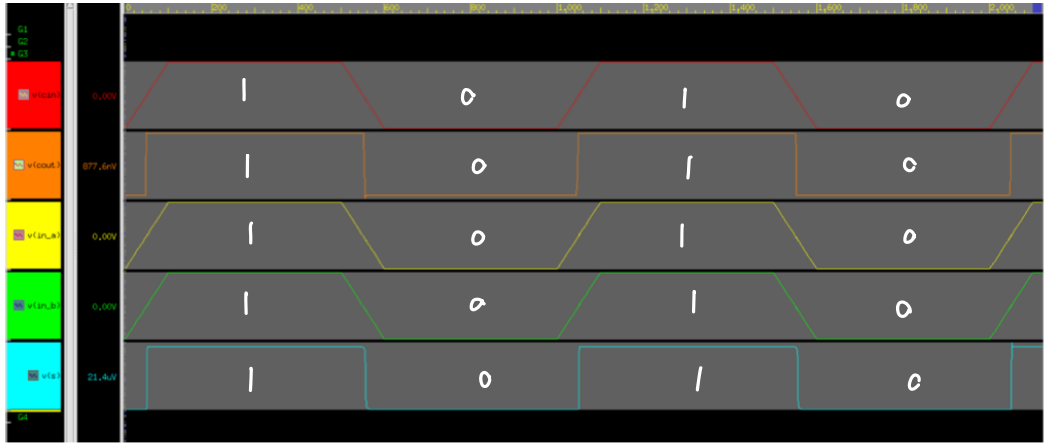


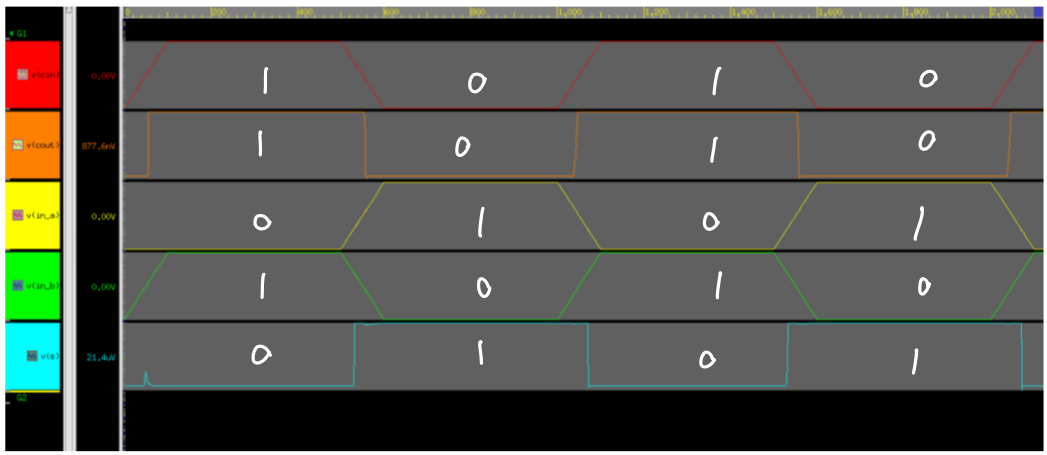
transistor level diagram :

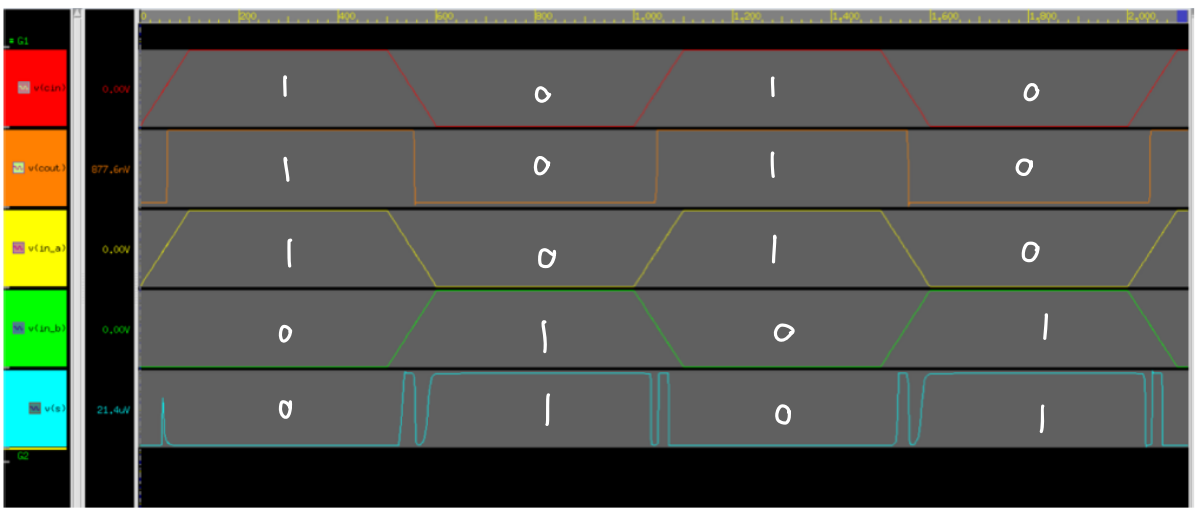


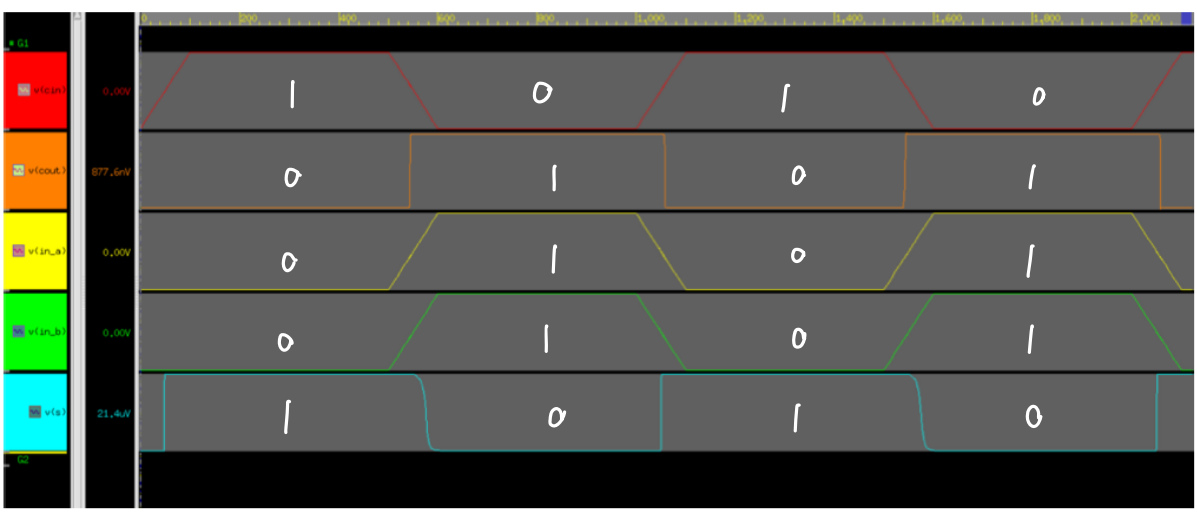
truth table:

A	B	Cin	Cout	S
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

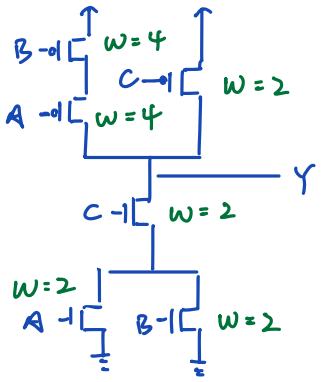






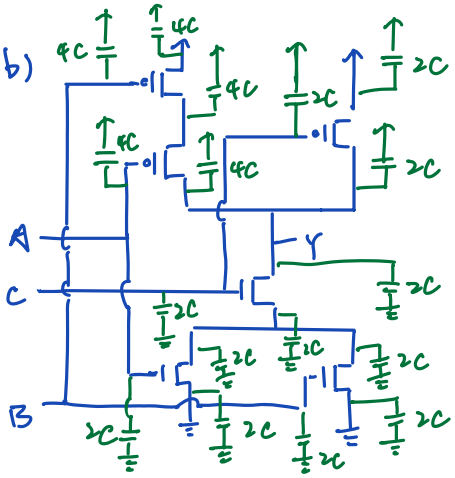


2. (a)



assume that $\mu_n = 2\mu_p$

(b)



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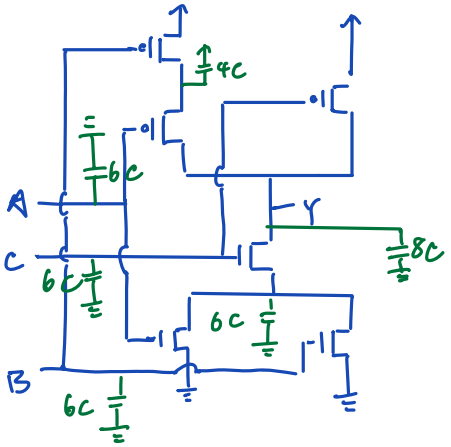
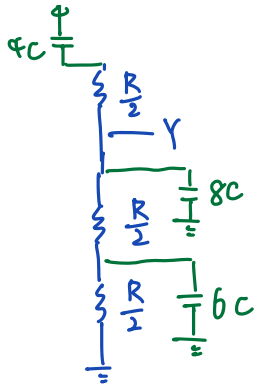


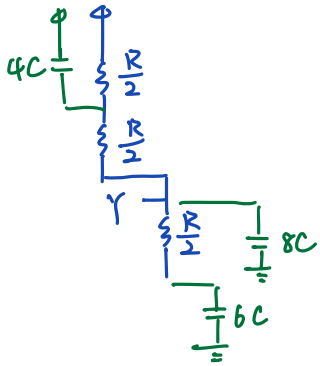
for falling delays (worst case)



$t_{pdf} = \frac{R}{2}\cdot 6C + (\frac{R}{2}+\frac{R}{2})\cdot 8C + (\frac{R}{2}+\frac{R}{2})4C$

$= 15RC$ #

for rising delays (worst case)



$t_{pdr} = \frac{R}{2}\cdot 4C + (\frac{R}{2}+\frac{R}{2})(8C+6C)$

$= 16RC$ #

3. for n_1, $P_{n1} = \frac{1}{2}$. $\alpha = P_{n1}\cdot\overline{P_{n1}} = \frac{1}{4}$ #

for n_2, $n_2 = (A\cdot n_1)' = A' + n_1' \Rightarrow P_{n2} = \frac{3}{4}$, $\alpha = P_{n2}\cdot\overline{P_{n2}} = \frac{3}{16}$ #

for n_3, $n_3 = (D+n_1)' = n_1'D' \Rightarrow P_{n3} = \frac{1}{4}$, $\alpha = P_{n3}\cdot\overline{P_{n3}} = \frac{3}{16}$ #

for n_4, $n_4 = n_1' \Rightarrow P_{n4} = \frac{1}{2}$, $\alpha = P_{n4}\cdot\overline{P_{n4}} = \frac{1}{4}$ #

for n_5, $n_5 = (n_2\cdot n_3)' = n_2' + n_3' = An_1 + Dn_1 = n_1(A+D) \Rightarrow P_{n5} = \frac{3}{4}$, $\alpha = P_{n5}\cdot\overline{P_{n5}} = \frac{3}{16}$ #

B	C	A	D	n_1	n_2	n_3	n_5
0	0	0	0	0	1	1	0
0	0	0	1	0	1	0	1
0	0	1	1	0	1	0	1
0	0	1	0	0	1	1	0

B	C	A	D	n_1	n_2	n_3	n_5
0	1	0	0	1	1	0	1
0	1	0	1	1	1	0	1
0	1	1	1	1	0	0	1
0	1	1	0	1	0	0	1

B	C	A	D	n_1	n_2	n_3	n_5
1	0	0	0	1	1	0	1
1	0	0	1	1	1	0	1
1	0	1	1	1	0	0	1
1	0	1	0	1	0	0	1

B	C	A	D	n_1	n_2	n_3	n_5
1	1	0	0	0	1	1	0
1	1	0	1	0	1	0	1
1	1	1	1	0	1	0	1
1	1	1	0	0	1	1	0