JESD204B Overview

Texas Instruments High Speed Data Converter Training

Outline

- JESD204B Standard at a Glance
- Benefits / Cost
- Timing Signals
- Layers Overview (Transport, Link, Physical)
- Deterministic Latency
- Subclasses

JESD204B Standard at a Glance

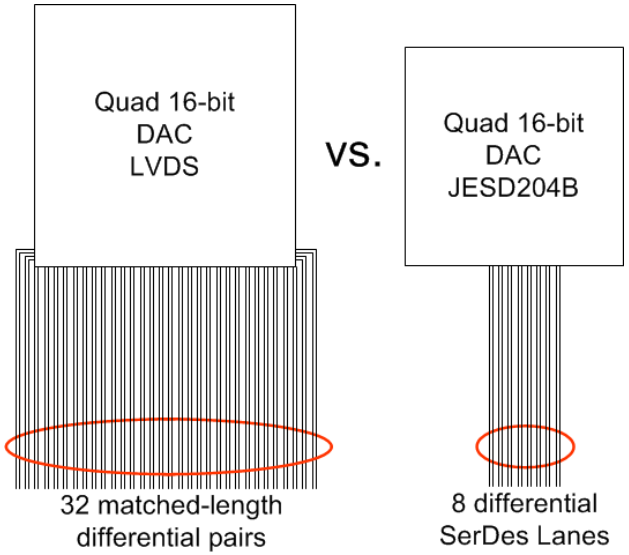
- A standardized serial interface between data converters (ADCs and DACs) and logic devices (FPGAs or ASICs)
- Serial data rates up to 12.5 Gbps
- Mechanism to achieve deterministic latency across the serial link
- Uses 8b/10b encoding for SerDes synchronization, clock recovery and DC balance
- **JESD204B is a must for high density systems!**

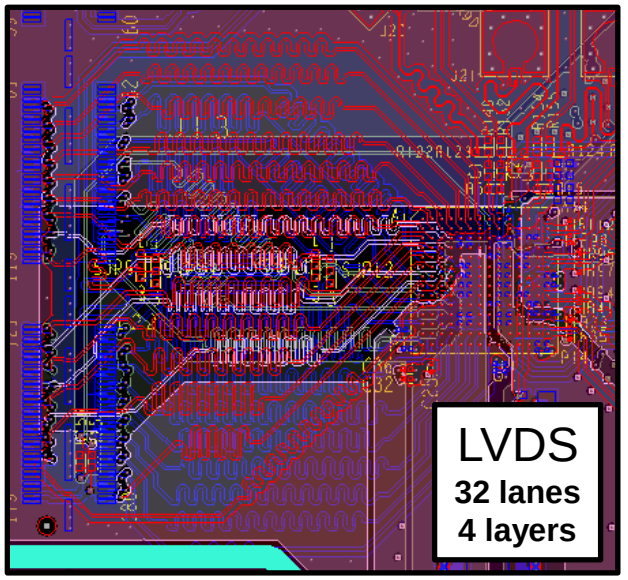
JESD204B Standard at a Glance

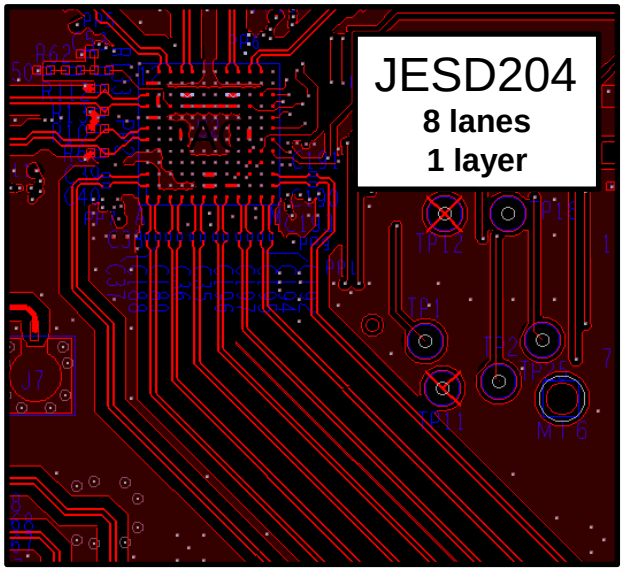
Feature	JESD204	JESD204A	JESD204B
Introduction of Standard	2006	2008	2011
Maximum Lane Rate	3.125 Gbps	3.125 Gbps	**12.5 Gbps**
Multiple Lane Support	No	**Yes**	**Yes**
Multi-Lane Synchronization	No	**Yes**	**Yes**
Multi-Device Synchronization	No	**Yes**	**Yes**
Deterministic Latency	No	No	**Yes**
Harmonic Clocking	No	No	**Yes**

JESD204B Benefits

- Reduced/simplified PCB area
- Reduced package size
- Comparable power for large throughput
- Scalable to higher frequencies
- Simplified interface timing
- Standard interface







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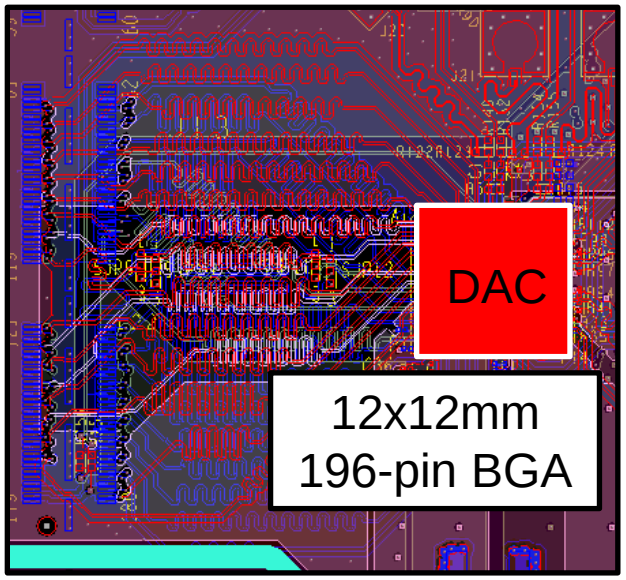

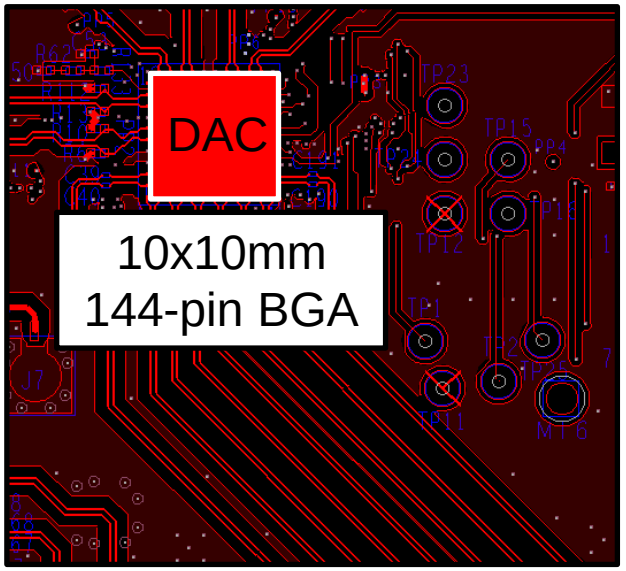

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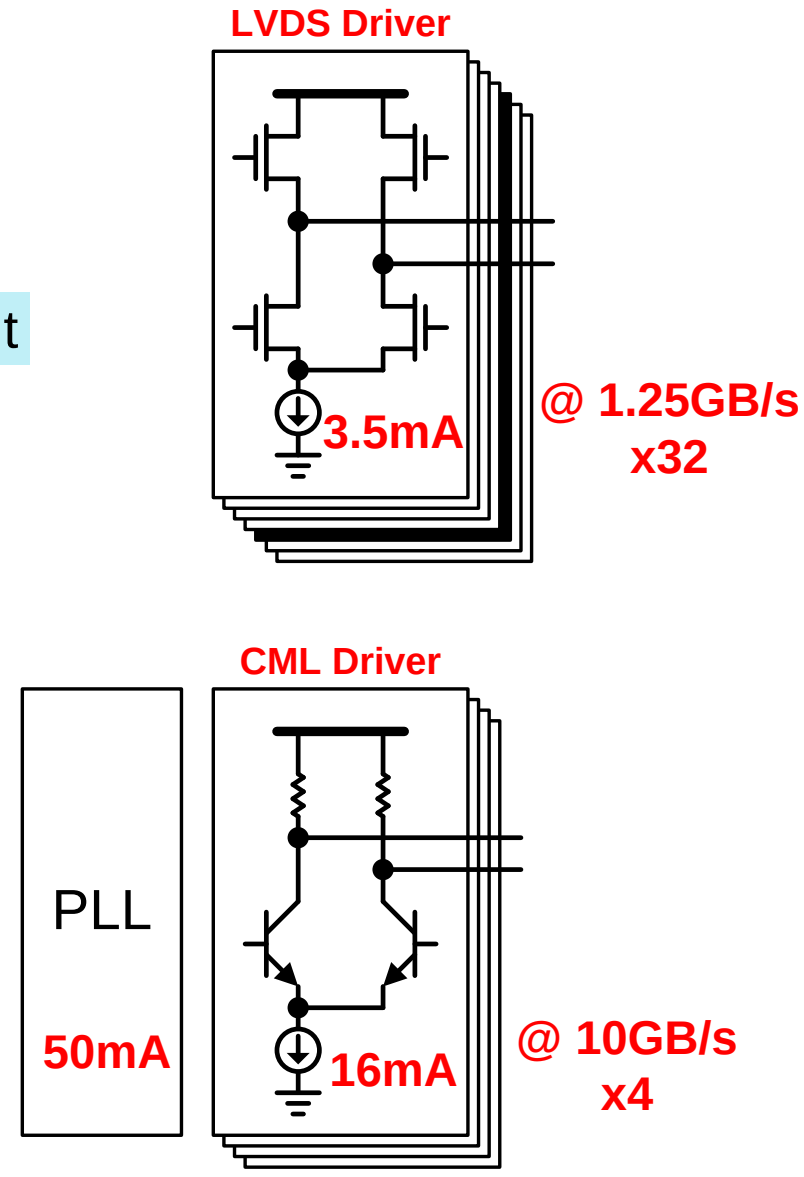

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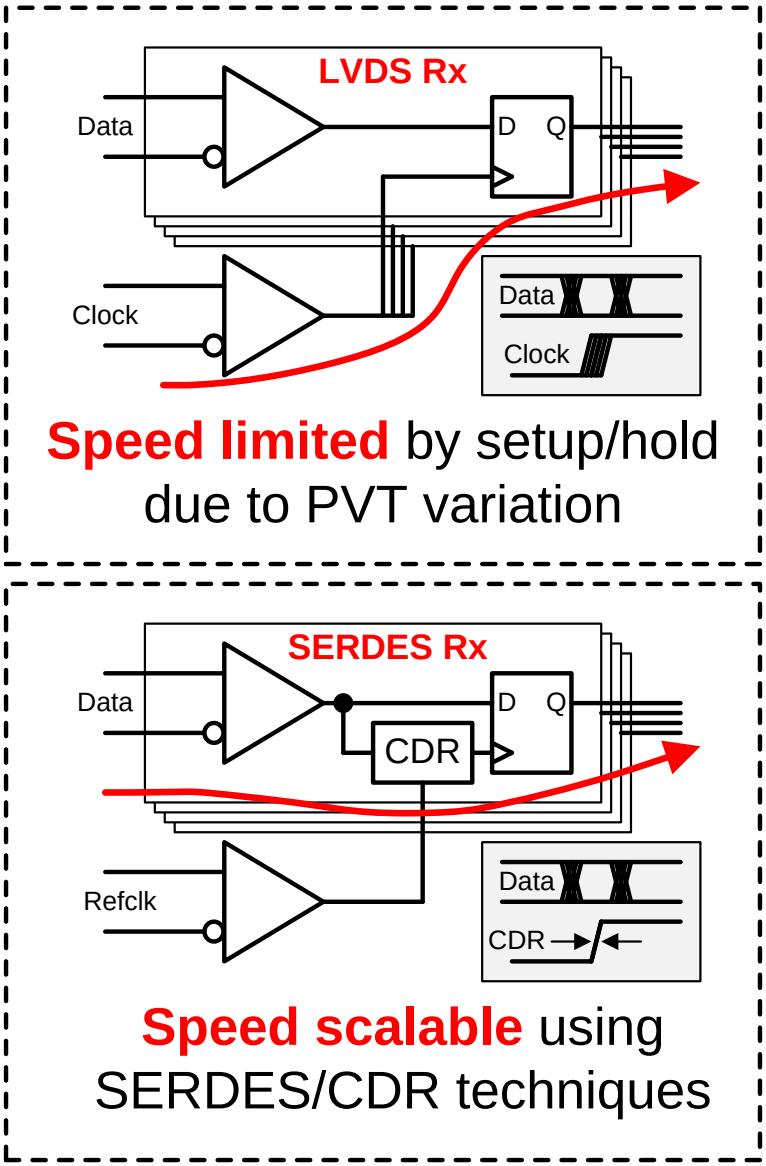

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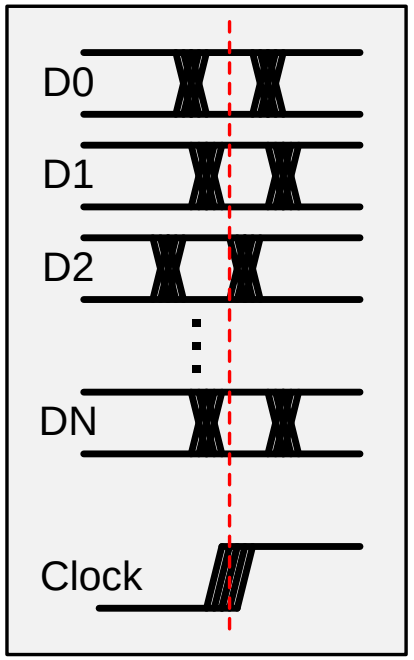
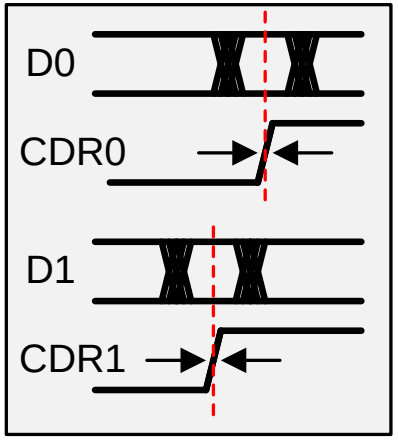
LVDS Timing



SERDES Timing



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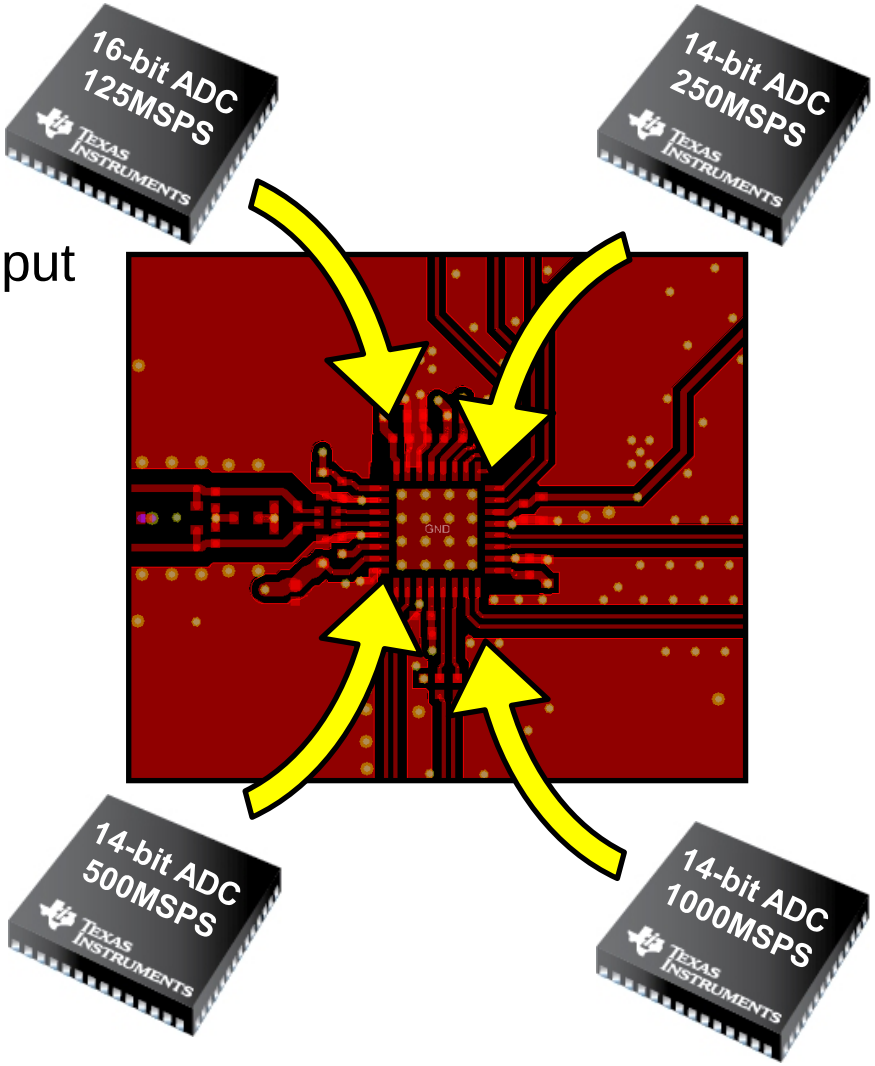
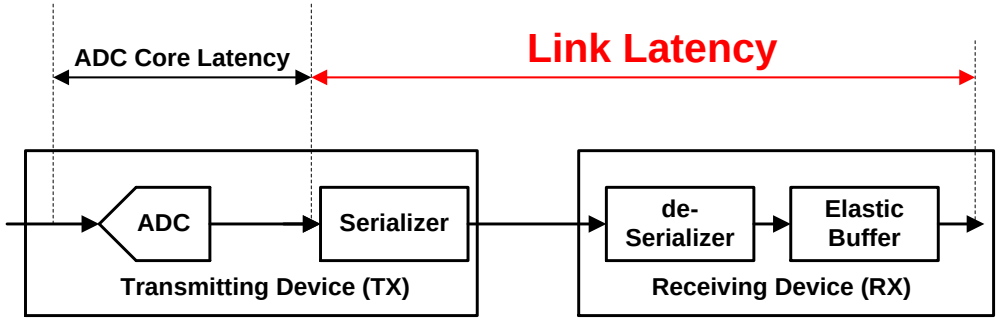
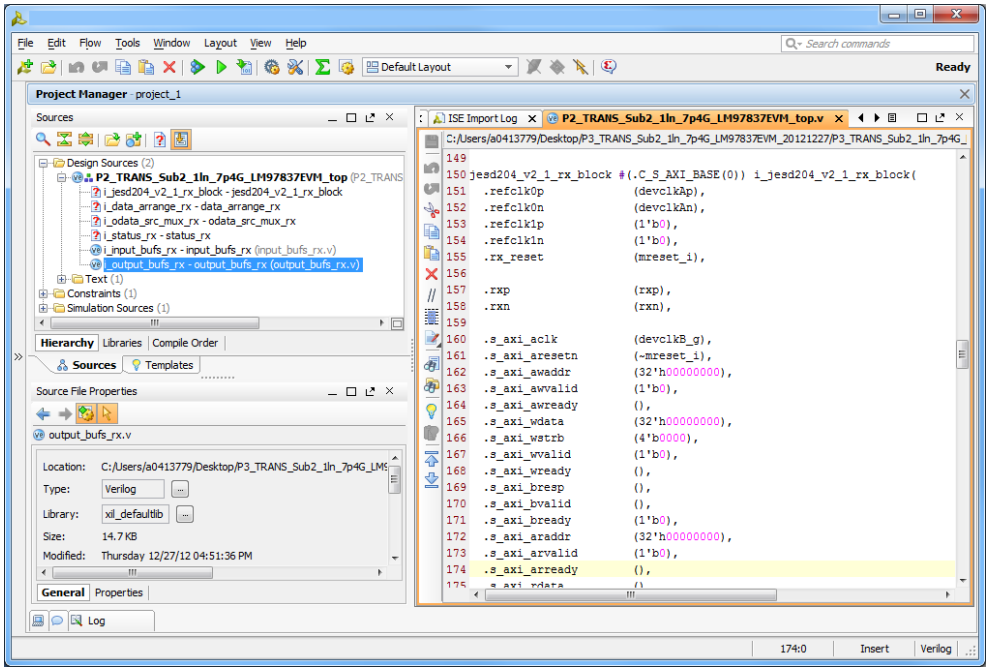


JESD204B Costs

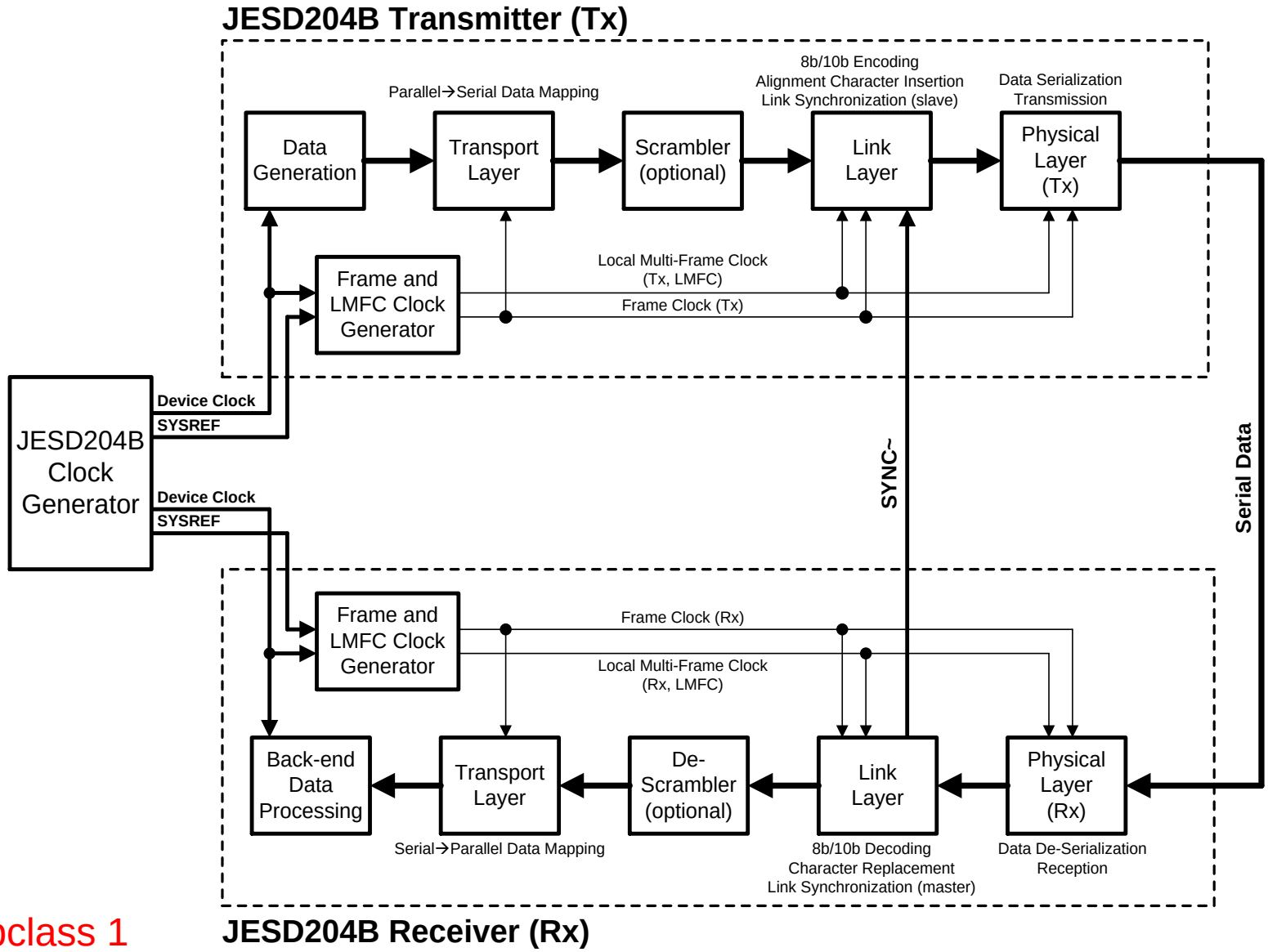
- Increased interface latency



- Increased FPGA firmware complexity / licensing



JESD204B Link Data Flow and Protocol Layer Diagram



*Subclass 1

JESD204 Timing Signals/Terminology

Frame Clock

- Data frame of the transport layer is aligned to the frame clock
- Frame clock period in all the TX and RX devices must be identical

Local Multi-Frame Clock (LMFC)

- Multi-Frame is composed of ‘K’ Frames
- LMFC is aligned to the multi-frame boundary
- Acts as a low-frequency reference to resolve frame clock phase ambiguity across multiple devices
- LMFC period in all TX and RX devices must be identical

JESD204 Timing Signals/Terminology

Device Clock

- System clock from which the device's frame, sampling, LMFC clocks are derived (externally applied)

Sample Clock

- Internal conversion clock of data converter
- Derived from Device Clock (via multipliers or dividers)
- Relationship to frame clock depends on packing of data into frame

SYSREF

- Timing phase reference from which LMFC clocks are generated in subclass 1 implementations (externally applied)
- Must be source synchronous with Device Clock
- Rising edge transition determines LMFC alignment

JESD204 Timing Signals/Terminology

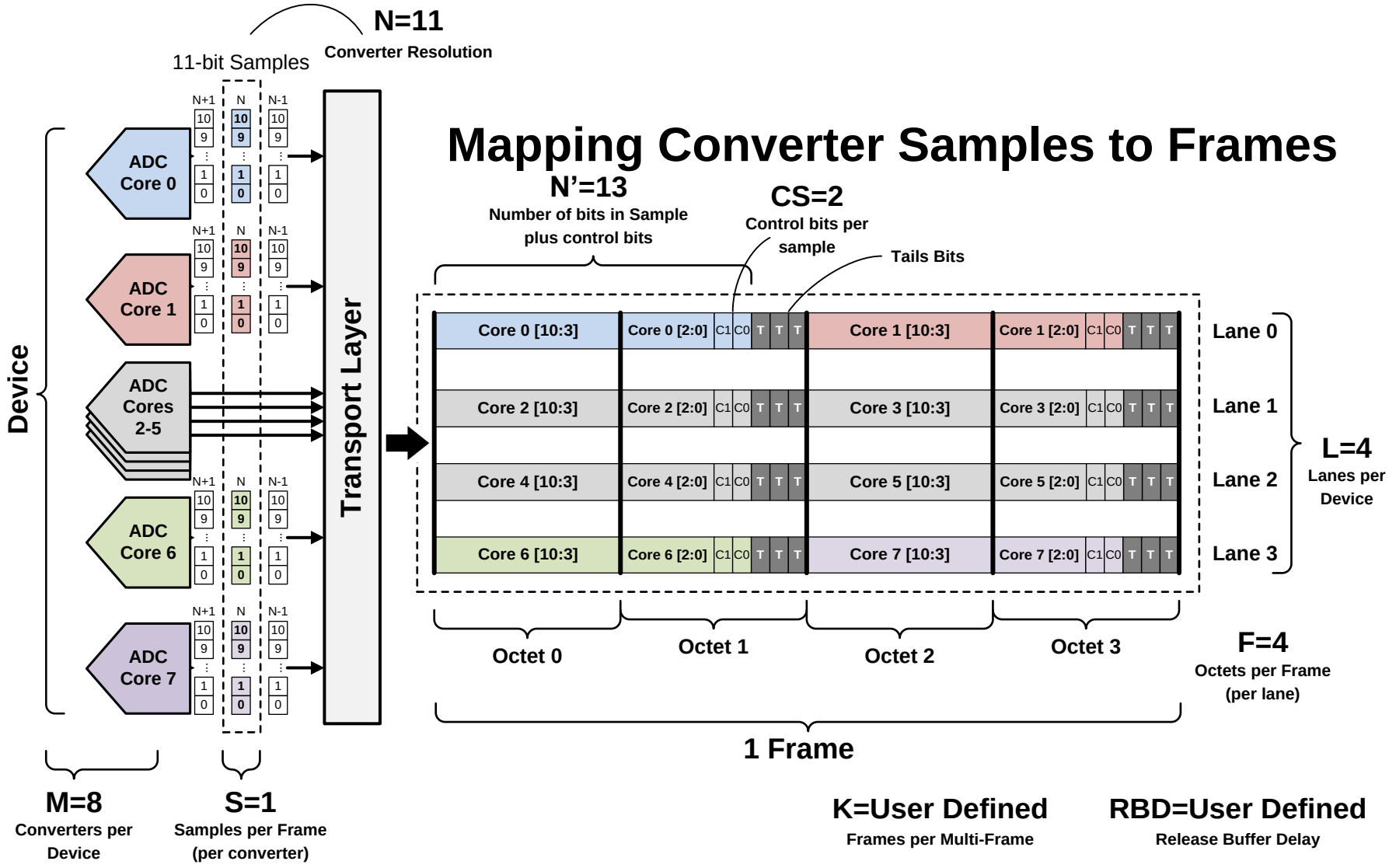
SYNC

- Unidirectional, Receiver-to-Transmitter
- Active low signaling, often referred to as ‘SYNC~’ or ‘SYNCb’
- Mainly used for device synchronization requests and error reporting
- Aligns LMFC phase in Subclass 2 devices
- Options available for distributing SYNC to multiple devices

Transport Layer Overview

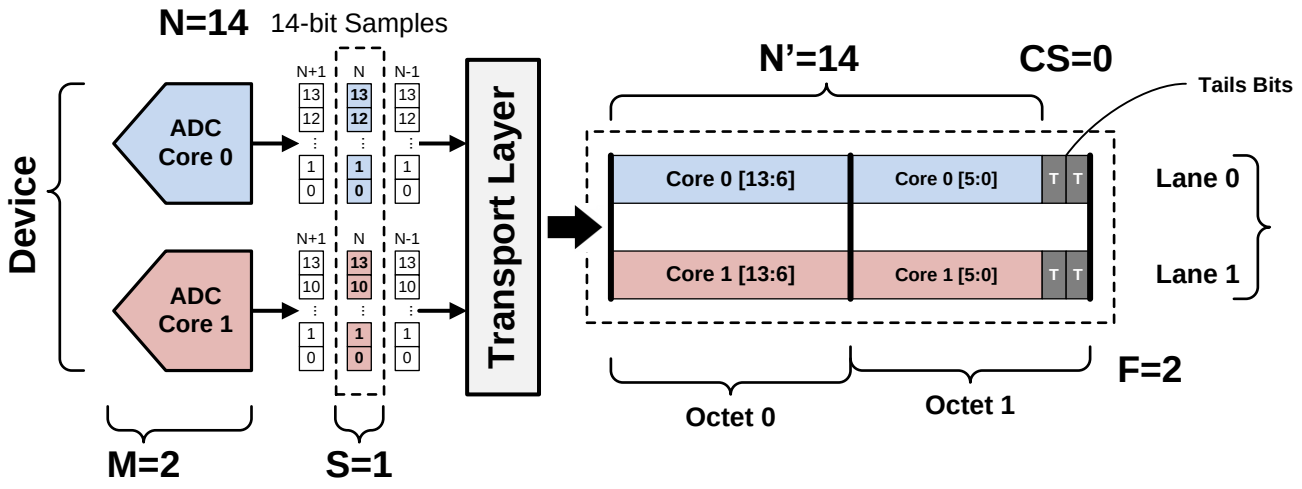
- Maps the data → octets → frames consisting of multiple octets
- Adds optional control bits to samples if needed
- Distinguishes the possible combinations of device/links/lanes/etc.
- Important parameters associated with transport layer include:
  - L # of lanes per converter device
  - M # of converters per device
  - F # of octets per frame (per lane)
  - S # of samples per converter per frame clock cycle
  - CS # of control bits per conversion sample

Transport Layer (Generic Example)

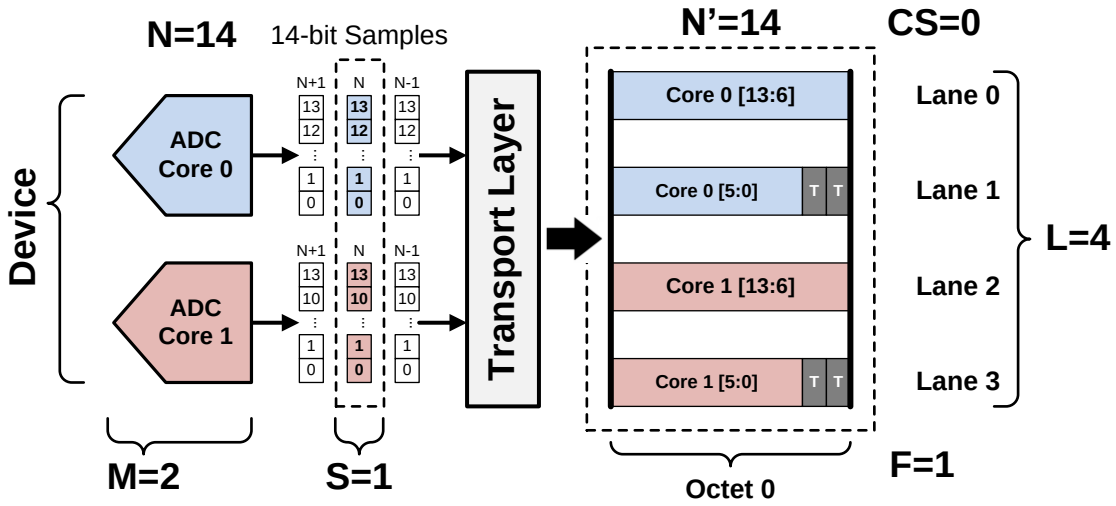


Transport Layer (ex. ADS42JB49)

LMFS 2221



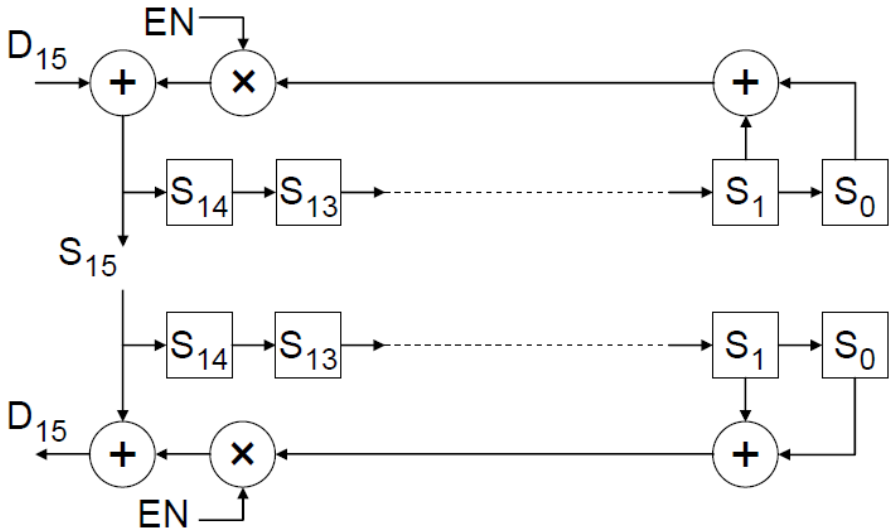
LMFS 4211



Note: Actual ADS42JB49 implementation defines N'=16 and inserts 0's into LSBs instead of defining tail bits

Scrambling

- Scrambling randomizes data and spreads the spectral content to reduce spectral peaks that could cause EMI and interference problems
- Transport layer output may be optionally scrambled with the polynomial: $1 + x^{14} + x^{15}$
- The RX descrambler self-synchronizes after receiving only two octets
- TX supports early-synchronization option that allows descrambler to self-synchronize during ILA



Data Link Layer

- 8b/10b Encoding
- Link Establishment, including frame and lane alignment
- Link Monitoring using control symbols

Data Link Layer: 8b/10b Encoding

- Encodes 8-bit “octets” into 10-bit symbols
- Octet to symbol mapping depends on running disparity (RD)
- Coding provides many bit-transitions to enable CDR techniques
- DC balancing enables AC coupling

5b/6b code

Input		RD = −1	RD = +1	Input		RD = −1	RD = +1
	EDCBA	abcdei			EDCBA	abcdei	
D.00	00000	100111	011000	D.16	10000	011011	100100
D.01	00001	011101	100010	D.17	10001	100011	
D.02	00010	101101	010010	D.18	10010	010011	
D.03	00011	110001		D.19	10011	110010	
D.04	00100	110101	001010	D.20	10100	001011	
D.05	00101	101001		D.21	10101	101010	
D.06	00110	011001		D.22	10110	011010	
D.07	00111	111000	000111	D.23 †	10111	111010	000101
D.08	01000	111001	000110	D.24	11000	110011	001100
D.09	01001	100101		D.25	11001	100110	
D.10	01010	010101		D.26	11010	010110	
D.11	01011	110100		D.27 †	11011	110110	001001
D.12	01100	001101		D.28	11100	001110	
D.13	01101	101100		D.29 †	11101	101110	010001
D.14	01110	011100		D.30 †	11110	011110	100001
D.15	01111	010111	101000	D.31	11111	101011	010100
				K.28	11100	001111	110000

3b/4b code

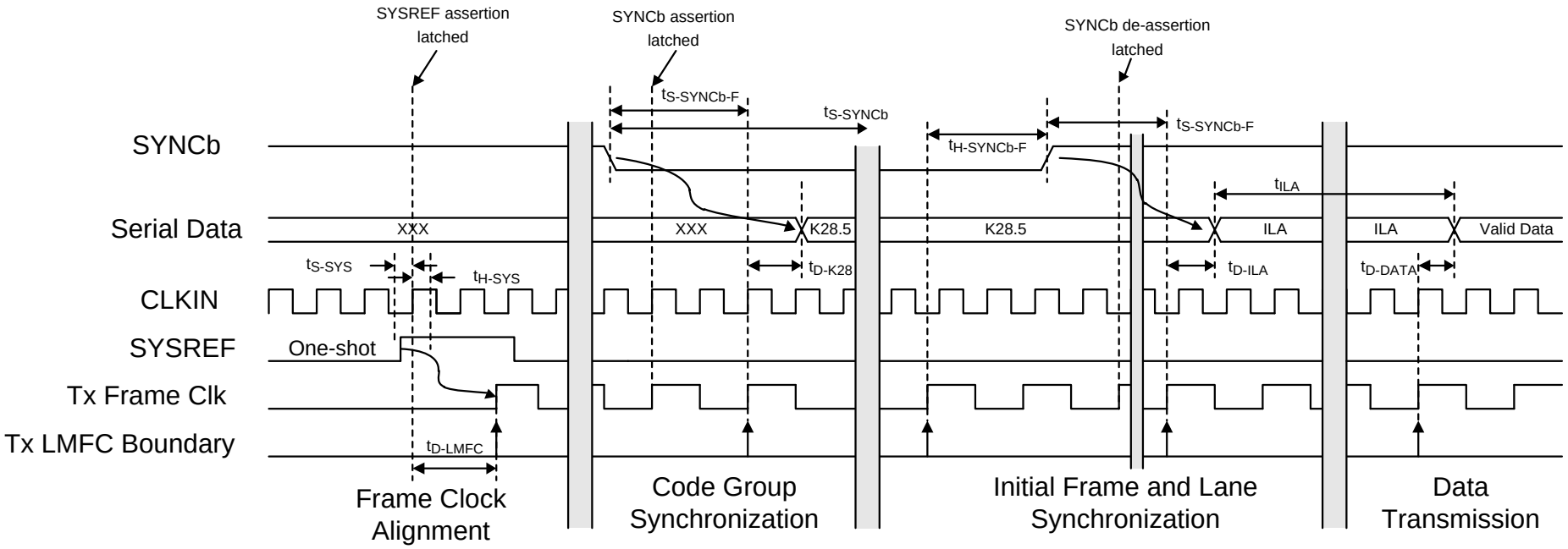
Input		RD = −1	RD = +1	Input		RD = −1	RD = +1
	HGF	fghj			HGF	fghj	
D.x.0	000	1011	0100	K.x.0	000	1011	0100
D.x.1	001	1001		K.x.1 ‡	001	0110	1001
D.x.2	010	0101		K.x.2 ‡	010	1010	0101
D.x.3	011	1100	0011	K.x.3 ‡	011	1100	0011
D.x.4	100	1101	0010	K.x.4	100	1101	0010
D.x.5	101	1010		K.x.5 ‡	101	0101	1010
D.x.6	110	0110		K.x.6 ‡	110	1001	0110
D.x.P7 †	111	1110	0001				
D.x.A7 †	111	0111	1000	K.x.7 †	111	0111	1000

Control symbols

Input				RD = −1	RD = +1
	DEC	HEX	HGF EDCBA	abcdei fghj	abcdei fghj
K.28.0	28	1C	000 11100	001111 0100	110000 1011
K.28.1 †	60	3C	001 11100	001111 1001	110000 0110
K.28.2	92	5C	010 11100	001111 0101	110000 1010
K.28.3	124	7C	011 11100	001111 0011	110000 1100
K.28.4	156	9C	100 11100	001111 0010	110000 1101
K.28.5 †	188	BC	101 11100	001111 1010	110000 0101
K.28.6	220	DC	110 11100	001111 0110	110000 1001
K.28.7 ‡	252	FC	111 11100	001111 1000	110000 0111
K.23.7	247	F7	111 10111	111010 1000	000101 0111
K.27.7	251	FB	111 11011	110110 1000	001001 0111
K.29.7	253	FD	111 11101	101110 1000	010001 0111
K.30.7	254	FE	111 11110	011110 1000	100001 0111

Data Link Layer: Link Establishment

- Link Establishment accomplishes TX and RX synchronization
  - Code Group Synchronization (CGS)
  - Initial Frame Synchronization
  - Initial Lane Synchronization



Physical Layer: Serial Lanes

- Physical layer defines the electrical and timing characteristics of data transfer
- Point-to-point, unidirectional serial interface
- AC or DC compliance
- 3 signal speed-grade variants
- Performance limited by SERDES, CDR and driver/receiver blocks

Parameter	LV-OIF-Sx15	LV-OIF-6G-SR	LV-OIF-11G-SR
Data Rates	312.5Mbps – 3.125Gbps	312.5Mbps - 6.375Gbps	312.5Mbps – 12.5Gbps
Differential Output Voltage	500 – 1000 (mV)	400 – 750 (mV)	360 – 770 (mV)
Bit Error Rate (BER)	≤ 1e-12	≤ 1e-15	≤ 1e-15

Deterministic Latency: Motivation

- Applications are often sensitive to the variation of system latency
  - Synchronous sampling
  - Multi-channel phase array alignment
  - Gain control loop stability

- JESD204 and JESD204A do not achieve known/constant latency across the link across temp/supply/reboot variation

- Providing support for devices with internal clock dividers introduces potential for even more latency uncertainty

Deterministic Latency: Achieved

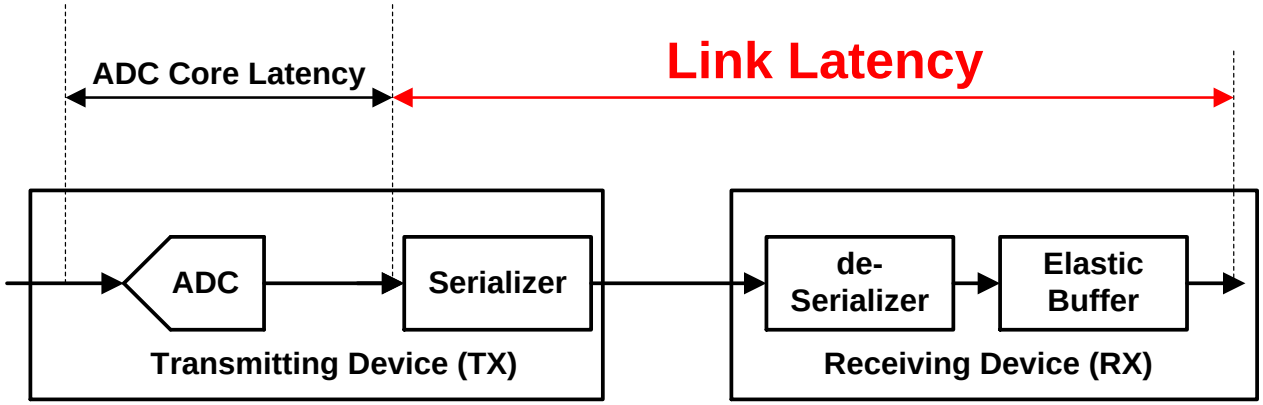
- JESD204B achieves deterministic latency: known/constant latency
  - Subclass 0: DL not achieved
  - Subclass 1: DL achieved using SYSREF with strict timing
  - Subclass 2: DL achieved using SYNC~ with strict timing

- Deterministic Latency achieved with these architecture features
  - SYSREF or SYNC~ are used to provide a deterministic reference phase to all devices for synchronization
  - LMFC provides a low frequency reference to avoid frame clock phase ambiguity in the presence of link delay changes
  - RX has an “elastic buffer” that absorbs link delay variation

- Texas Instruments recommends/supports subclass 1
  - LMFC phase easier to control with source synchronous SYSREF than with system synchronous SYNC~

JESD204B Subclasses

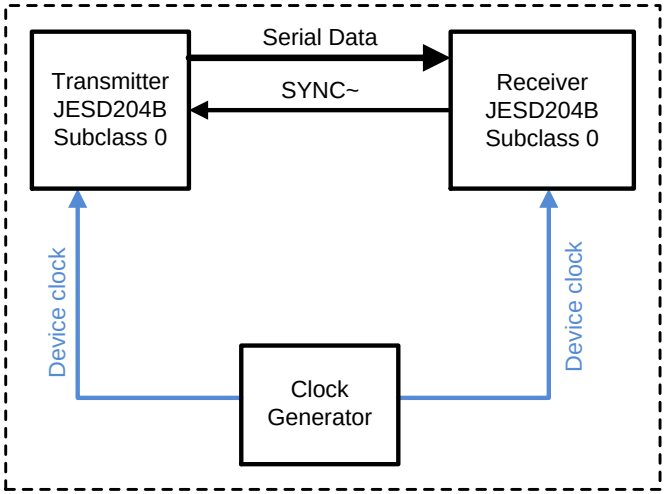
- Subclass distinction: Whether to, and how to achieve **time reference alignment** (as a requirement for **deterministic link latency**)



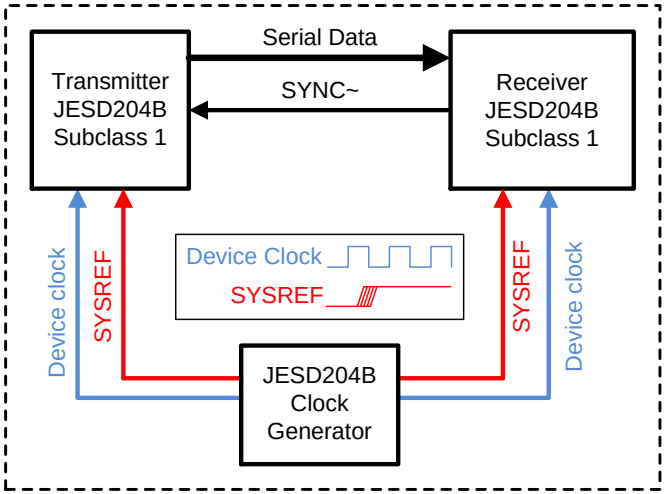
	Subclass 0	Subclass 1	Subclass 2
Deterministic Latency Supported?	No	Yes	Yes
How to achieve Deterministic Latency?	N/A	Time reference (LMFC) alignment using **SYSREF**	Time reference (LMFC) alignment using **~SYNC**

Subclass Signaling Requirements

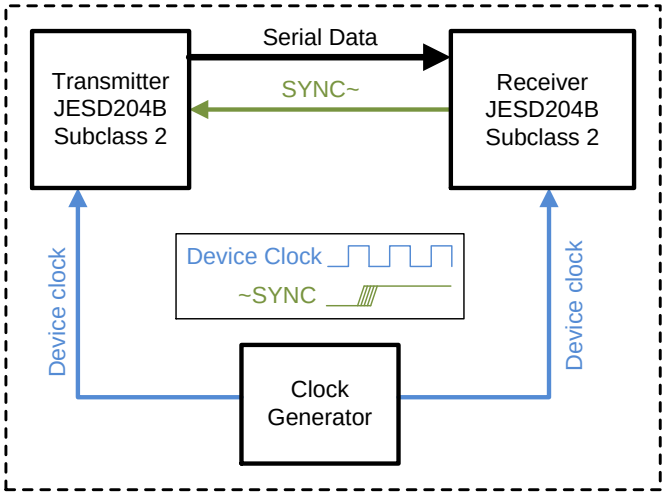
SUBCLASS 0



SUBCLASS 1



SUBCLASS 2



Choosing a Subclass

	Subclass 0	Subclass 1	Subclass 2
JESD204A Backward Compatible?	Yes	No	No
Deterministic Latency Supported?	No	Yes	Yes, but speed limited
SYSREF Required?	No	Yes	No
Clock and Sync Signals	Device Clock SYNC~	Device Clock SYSREF SYNC~	Device Clock SYNC~
SYNC~ is Timing Critical?	No	No	Yes
Interface Hardware Complexity	Least	Most	Moderate
Link Latency	8-100 sample clocks (non-deterministic) 15-120 sample clocks (deterministic)		

Subclass by Application Examples

	Subclass 0	Subclass 1	Subclass 2
Wireless Comms. Repeater - Narrowband (<125 MSPS ADC) - No DL requirements	✓	✓	✓
Software Defined Radio - Wideband - DL required		✓ >250 MSPS ADC	✓ <=250 MSPS ADC
Radar, Imaging Sensor - Wideband (>250 MSPS ADC) - DL required + Multi-Device Sync.		✓	
Oscilloscope, Spectrum Analyzer - Wideband (> 250 MSPS ADC)	✓ No DL Required	✓ DL Required	

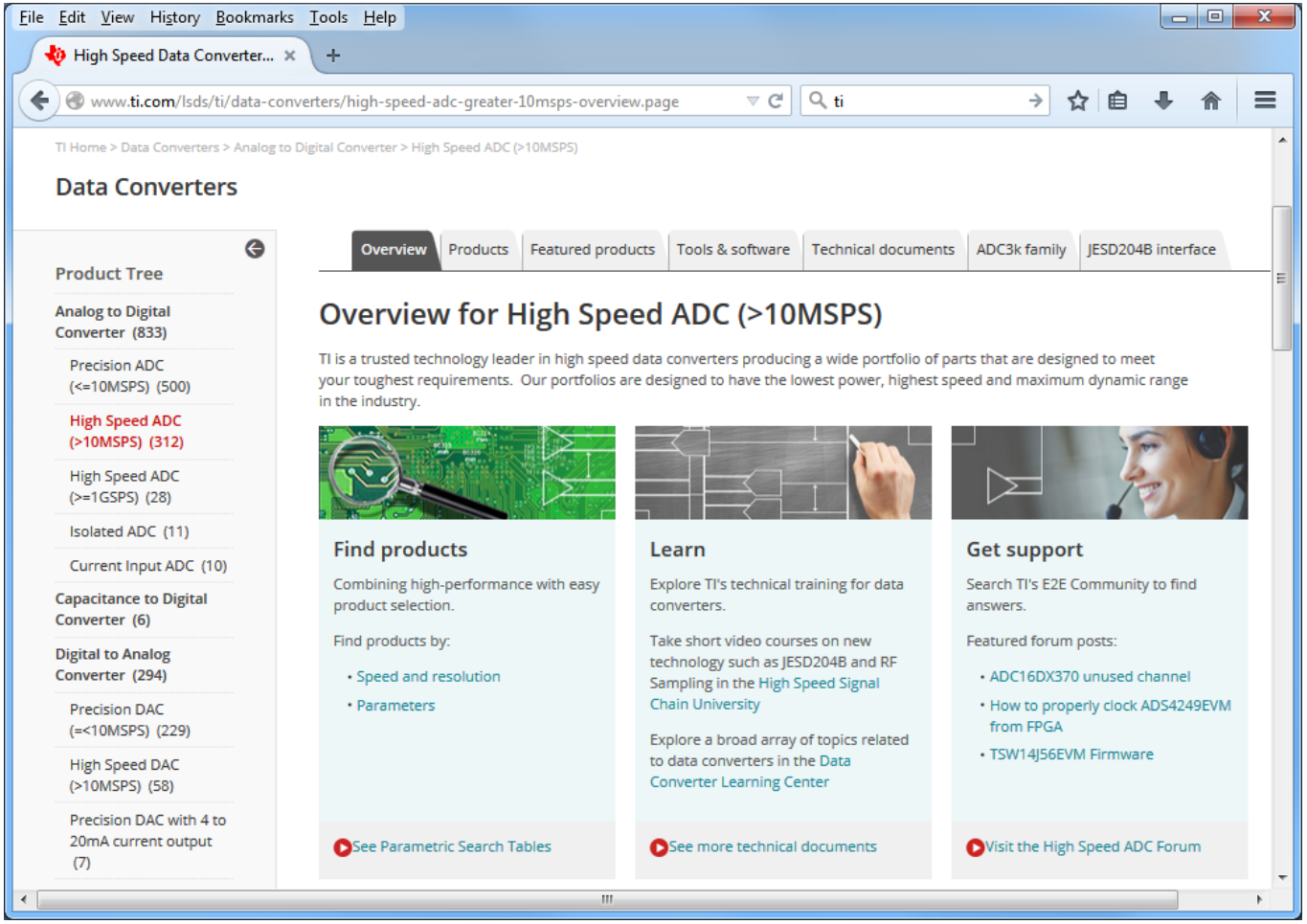
- Texas Instruments' JESD204B device all support subclass 1 while some support all 3 subclasses

Summary

- JESD204: Standard serial data interface for data converters
- JESD204B subclasses offer 3 implementation variations
- Transport Layer defines data framing into serial lanes
- Link layer defines encoding, synchronization and data monitoring
- Physical layer defines the electrical and timing performance
- Deterministic latency achieved with subclasses 1, 2 and is required for known/constant latency through link

More Educational Resources

www.ti.com/lsds/ti/data-converters/high-speed-adc-greater-10msps-jesd204b.page



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