AD9361 Gain Control

And

Received Strength Signal Indicator (RSSI)

User Guide

TABLE OF CONTENTS

Revision History 4
General Description 4
Abbreviations 4
Register and Bit Description Syntax 4
Quick Setup (Read this first!) 5
Gain Control 6
General Description 6
RF Port to Received Signal Level Conversion 6
Gain Control Threshold Detectors 7
Settling Times 9
Full and Split Gain Tables 9
Manual Gain Control (MGC) Mode 11
AGC Slow Attack 12
AGC Hybrid Mode 15
AGC Fast Attack Mode 15
Writing to and Reading From the Gain Table 20
External LNA 23
Fixed-Gain External LNA 23
Variable-Gain External LNA 23
RSSI 24
RSSI Mode Select 24
RSSI Measurement Duration 24
RSSI Weighting 24
RSSI Delay and RSSI Wait 24
RSSI Preamble and RSSI Symbol 25
RSSI RFIR 25
RSSI Gain Step Calibration 25
Appendix 1 — Register Settings for Example Applications 30
Application Example #1 – Full Table, Slow AGC, RSSI 30
Gain Control Application Example #2 — Split Table, Slow AGC 32
Gain Control Application Example #3 — Full Table, Fast AGC 32
Appendix 2 — Optimized Gain Tables 34
Full Gain Tables 34
Split Gain Table 41
Appendix 3--Noise Figure (NF) vs. Gain Index Plots 43

REVISION HISTORY

7/2010 — 2.0 Release

8/2011 — 2.1 Added gain tables, clarified external LNA section, added section on interferers

10/2011 — 2.2 Added gain tables, applications section

10/2011 — 2.3 Updated, clarified most sections

11/2011 — 2.4 Updated equations 1 & 2 to separate peak-to-average and average-to-rms into separate terms

11/2011 — 2.5 Final Release

1/2012 — 2.6 Added NF plots, added description of registers that contain gain index values

6/2012 — 2.7 Corrected Gain Step Cal error word readback script to read Rx1. Corrected Slow AGC Gain Update Counter clock to ClkRF.

6/2012 — 2.8 Added programming of LNA gain difference words and Max LNA gain to Gain Step Cal sequence for use in the field

3/2013 – 2.9 Correction to 0x12D description.

GENERAL DESCRIPTION

The versatile and highly configurable AD9361 transceiver has several gain control modes that enable its use in a variety of applications. Fully automatic gain control (AGC) modes are available that address time division duplex (TDD) as well as frequency division duplex (FDD) scenarios. In addition, the AD9361 has manual gain control (MGC) options that allow the baseband processor (BBP) to control the gain.

Given the wide variety of applications for which the AD9361 is suited, the received strength signal indicator (RSSI) many be setup in one of several configurations, allowing the user to optimize the RSS I to produce extremely accurate results with a minimum of BBP interaction. RSSI accuracy is inherently very good but can be improved through various means, including a . “ Gain Ste

This user guide explains the gain control, RSSI, and Gain Step Calibration functions in detail but it is also highly recommended that the AD9361 Register Map be near at hand when reading this user guide.

ABBREVIATIONS

AGC Automatic Gain Control where an algorithm in the AD9361 controls the receive path gain

BBP Baseband Processor (or digital baseband)

FDD Frequency Division Duplex in which transmit and receive signals can be present at the same time but use different frequencies

MGC Manual Gain Control where the BBP controls some or all of the gain control parameters in the AD9361

TDD Time Division Duplex in which transmit and receive signals can be present on the same frequency but at different times

REGISTER AND BIT DESCRIPTION SYNTAX

When a register with absolute bit locations are described in this document, the format is always in hex for the register and [Dx:Dy] for the bits. This format is best described by an example such as 0x0FA[D1:D0] which equates to register 0FA (hex), and only the lowest 2 significant bits of this register. Thus, the register and the bit locations are specifically delineated. A single bit such as the lowest significant bit in register 0x0FA is described as 0x0FA[D0].

When a register bit field is described, the format is different and does not reference specific registers or bits. As an example, the Gain Update Counter bit field would be referred to as “ Gain Update Counter <15:0> ”. This is a field of 16 bits that is called the Gain Update Counter. This format is most often used in equations.

When describing the value of just a few bits, the following format is used: x ’byyy. In this case, “x” equals th “b” indicates binary and “yyy” represents three digital bits with values of 0 or 1. As an example, if two bits equal 2 and the next higher bit = 0. A common expression might be 0x0FA[D1:D0] = 2b ’00.

The following example encompasses all three concepts:

Gain Update Counter<15:0> is stored in 0x124[D7:D0] and 0x125[D7:D0]. Setting 0x128[D5] = 1 ’b1 doubles the effective Gain Update Counter.

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AD9361 Gain Control & RSSI User Guide

GAIN CONTROL

GENERAL DESCRIPTION

The AD9361 receive signal path can be broken up into several blocks as shown in the figure below. The gain of almost all of the blocks is variable as shown by the arrows through the shapes in the figure. The figure below shows only one receiver path but there are two paths in the AD9361, each of which has its own independent gain.

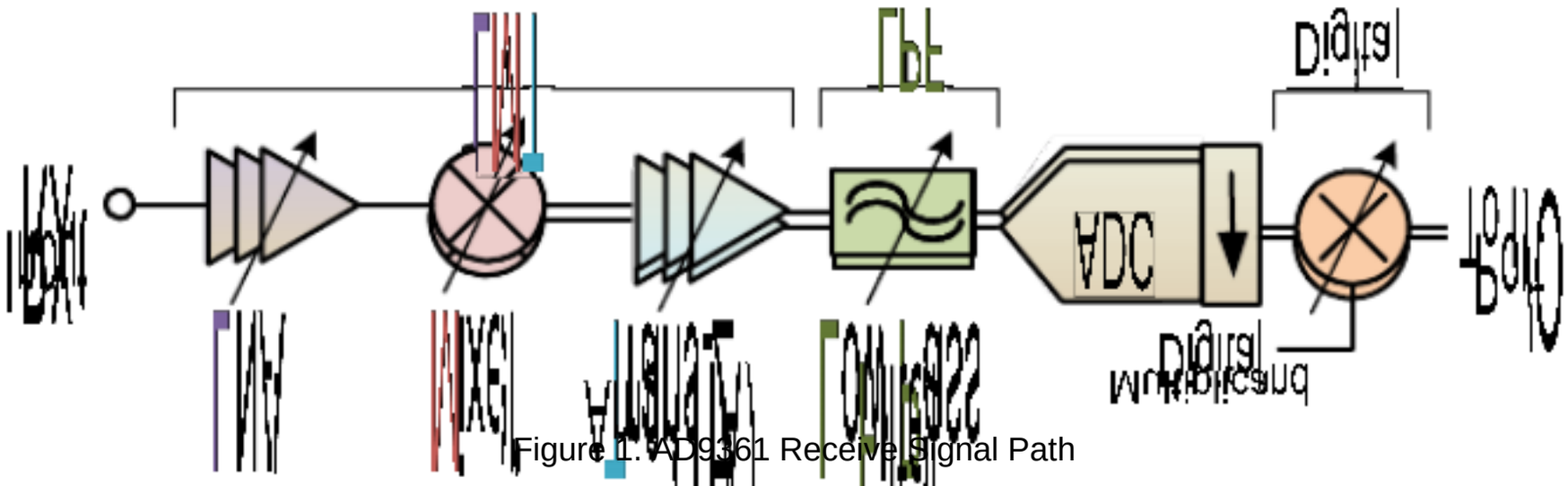

Figure 1. AD9361 Receive Signal Path

Each receiver has its own “Gain Table” that maps a gain control word to each of the variable gain blocks in the figure above. A pointer to the table determines the control word values sent to each block as shown in the figure below. Whether automatic gain control (AGC) or manual gain control (MGC) is used, the pointer moves up and down the table, which changes the gain in one or more of the blocks shown above.

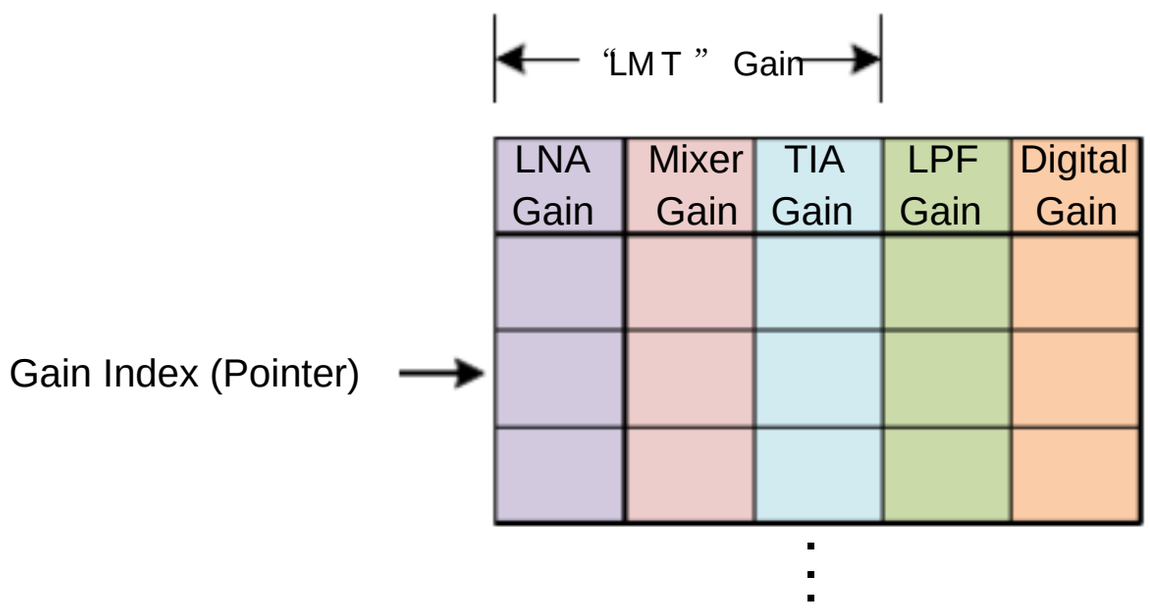

Figure 2. AD9361 Gain Table Mapping

RF PORT TO RECEIVED SIGNAL LEVEL CONVERSION

The ADC maximum input (0dBFS) is 0.625Vpk. dBm may be converted to dBFS(peak) at the I/O port with the following equation.

4.1

Equation 1

Rearranging yields an equation that determines input power at the RF port given the received signal level and the gain of the AD9361.

4.1 13

Equation 2

Where

Rev. .

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Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

Pin(dBm) is the power at the AD9361 receive port in dBm

Analog Gain(dB) is the total gain in dB of the LNA, Mixer, TIA, and LPF stages

The “ 4.1dB ” factor converts the maximum ADC peak voltage to dBVpeak. The maximum ADC level is 0.625Vpk and 20 ? log 0.625 . An input of 0.625Vpk results in a full scale digital output code. While the true maximum ADC level is 0.625Vpk, at that level, the ADC is in compression. To avoid compression, the maximum recommended peak input level to the ADC is 0.5Vpk, which is 1.9dB lower than full scale.

PAR(dB) is the peak to average ratio (usually referred to as the PAR, peak-to-average ratio or the crest factor) which for a sine wave is 3dB.

ARC(dB) converts from average power to RMS power. Depending on the waveform, RMS and average are not necessarily the same value.

The “ 13dB ” factor converts dBm to dBVrms as shown in the following derivation. 0 dBm is by definition 1mW dissipated in 50

0 0.001 —— Equation 3

Rearranging yields

$\sqrt{0.001 ? 50}$ 0.223 Equation 4

And calculating dBV from the voltage in volts results in

20 ? 0.223 Equation 5

GAIN CONTROL THRESHOLD DETECTORS

The AD9361 uses detectors to determine if the received signal is overloading a particular block or if the signal has dropped below programmable thresholds. “ LMTA”DC and Overload detectors (also referred to as “ Peak Detectors ”) react to nearly instant overload events. In contrast, a power measurement in the AD9361 occurs over 16 or more Rx samples. Figure 3 shows where these detectors are located in signal path.

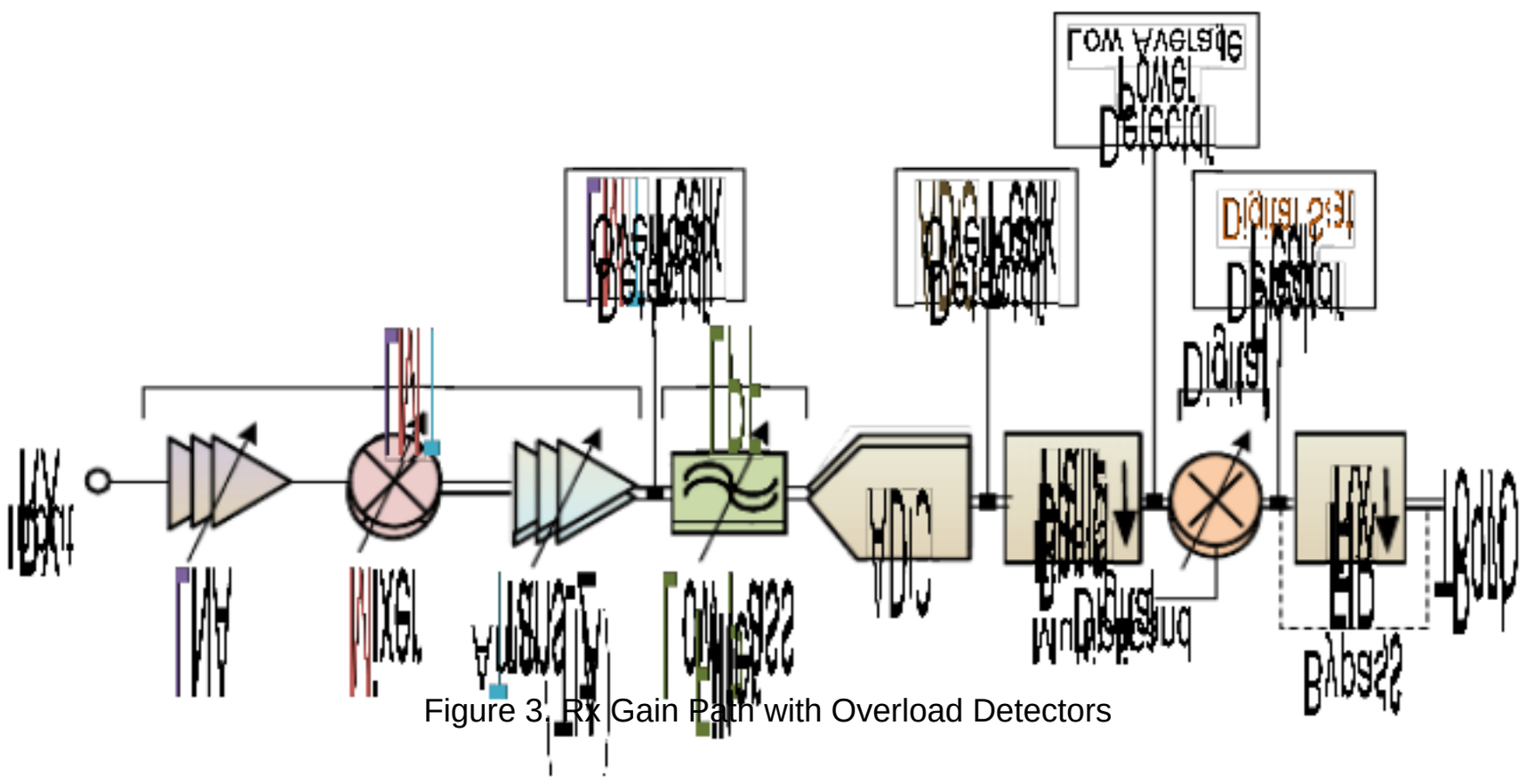

Figure 3. Rx Gain Path with Overload Detectors

LMT Overload Detector

The LNA/Mixer/Trans-Impedance Amplifier (LMT) overload detector is an analog peak detector used to determine if the received signal is overloading the blocks before the analog Low Pass Filter. If an LMT overload occurs but the ADC does not overload, it may indicate that an out-of-band interfering signal is resulting in the overload condition.

There are two different LMT overload thresholds, one used to indicate larger overloads and one used to indicate smaller overloads. Both thresholds are programmable, with the small overload threshold stored in register 0x107 and the large overload threshold stored in register 0x108. The thresholds are common to both receivers. The thresholds map to register values per the equation below. The threshold should be set such that it is lower (or equal to) the “large” threshold since the AGC will be affected differently dep which threshold is exceeded. In MGC mode, the BBP can monitor the overload flags via the Control Output pins. Equation 6 describes both large and small thresholds.

?
Equation 6

5: 0

ADC Overload Detector

The ADC is a highly oversampled sigma-delta modulator (SDM) with an output ranging from +4 to -4. A particular ADC output sample does not necessarily represent the input signal at a particular time. Rather, a positive value indicates that the input signal is more positive since the last sample and a negative value indicates that the input signal is more negative since the last sample. Note that since the ADC is highly oversampled, the ADC clock is much faster than the receive sample rate. Decimating and low pass filtering result in digital samples that represent the analog signal.

When the ADC is overloaded, the error between its samples and the input signal will cause the ADC to output more samples with values of +4 or -4 as it struggles to track the input signal.

The following figure shows how the ADC overload detector processes signals and how the thresholds are used.

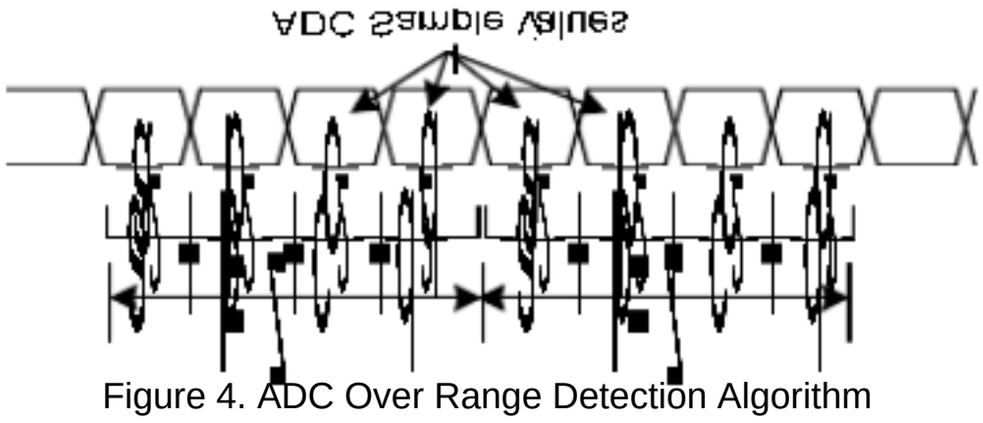

Figure 4. ADC Over Range Detection Algorithm

There are two programmable thresholds. The “Small ADC Overload” threshold is stored in register 0x104 and the “L Overload” threshold is stored in register 0x105. The thresholds are common to both receivers. The number of samples to use in the sum-of-squares calculation is set in register 0x0FC[D2:D0]. The resulting value “z” shown in the figure above is compare two thresholds and if a particular threshold is exceeded, a flag is set. In MGC mode, the BBP can monitor the overload flag(s) via the Control Output pins.

Low Power Threshold

The Low Power Threshold is an absolute threshold measured in – dBFS with a resolution of 0.5dBFS per LSB. The range is 0 to -63.5dBFS. The value is stored in register 0x114 and is common to both receivers. The AD9361 uses this threshold in the Fast Attack AGC mode and it can also be used in MGC mode, both of which are described later in this document. In Fast Attack AGC Mode, the Low Power Flag does not assert immediately after the average signal power drops below the Low Power Threshold. The flag only asserts once the signal power has remained below the Low Power Threshold for a time equal to the “Increment Time” in register Increment Time value is measured in ClkRF cycles (the clock used at the input of the Receive FIR Filter). In MGC mode, the Increment Time value is not used and the Low Power flag asserts as soon as the power drops below the Low Power Threshold.

Average Signal Power

When measuring power (such as forLow Power Threshold), the measurement is an average of a certain number of samples set by the “ Decimated Power Measurement Duration ” in register 0x15C[D3:D0]. The duration is common to both receivers. At the end of each measurement period, the average signal power value updates. The actual duration in Rx Sample Periods is per the following equation:

16

Equation 7

SETTLING TIMES

After a gain change, the AD9361 must reset overload detectors and power measurement circuits and wait for the receive path to settle before re-enabling detectors and power measurement blocks.

Peak Overload Wait Time

All Gain Control Modes use Peak Overload Wait Time. After a gain change, the AD9361 waits for the time set by this register before re-enabling its LMT and ADC overload detectors, which allows the signal in the analog path and the ADCs to settle. The default is fine for all applications unless anexternal LNA with a bypass mode is part of the signal path. The Peak Overload Wait Time is stored in register 0x0FE[D4:D0] and is clocked at the ClkRF rate (the input to the Rx FIR Filter clock rate).

Settling Delay

All AGC modes use Settling Delay, which is the time that the AGC holds the power measurement blocks in reset after a gain change. Power measurement occurs at the output of the Receive HB1 Filter (which is the input to the Receive FIR Filter) so all stages up to the Rx FIR must have settled before power measurement resumes after a gain change. The delay is equal to the value in register 0x111[D4:D0] multiplied by 2 and is clocked at the ClkRF rate. The default of 20 ClkRF cycles should work for all situations.

FULL AND SPLIT GAIN TABLES

As mentioned at the beginning of the document, the AD9361 uses a pointer to a row in a gain table. That row contains the gain values of each independent gain block. In this way, a “ gain index ” value (pointer) maps to a set of gain values for each gain block. How are two different ways that the AD9361 can implement the gain table. In “ Full Table ” mode, there is one table for eac Table ” mode, the AD9361 splits the LMT and LPF tables apart and controls each independently with separate pointers. If digital gain is enabled, there is a third table that is independently controlled, also with its own pointer. Each receiver has its own set of two (or three) tables. Bit D3 in register 0x0FB selects whether the AD9361 uses a full contiguous table or a split table scheme. The table architecture affects all gain control modes and is a common setting for both receivers. Table 1 shows the table mode to bit mapping.

Mode 0x0 F	B[D3]
Full Table	1
Split Table	0

Table 1. Table Mode vs. Bit Setting

Full Table Mode

The Full Table Mode is useful for most situations. For this mode, set 0x0FB[D3] high. A single gain table consists of all variable gain blocks in the Rx signal path. The figure below shows a portion of a full gain table. The figure also shows the gain of each block next to each gain index. If the gain index moves up or down, the gain indices of one or more blocks will change. If the gain index pointer moves up one step (to a table index of 57), both the LNA gain and the LPF gain will change. These changes allow the AD9361 to handle widely varying signal levels while still optimizing noise figure and linearity.

To read back the full table gain index in any gain control mode, read SPI register 0x2B0[D6:D0] for Rx1 and 0x2B5[D6:D0] for Rx2.

The Maximum Full Gain Table Index, set in register 0x0FD (common to both receivers), limits the maximum index allowed.

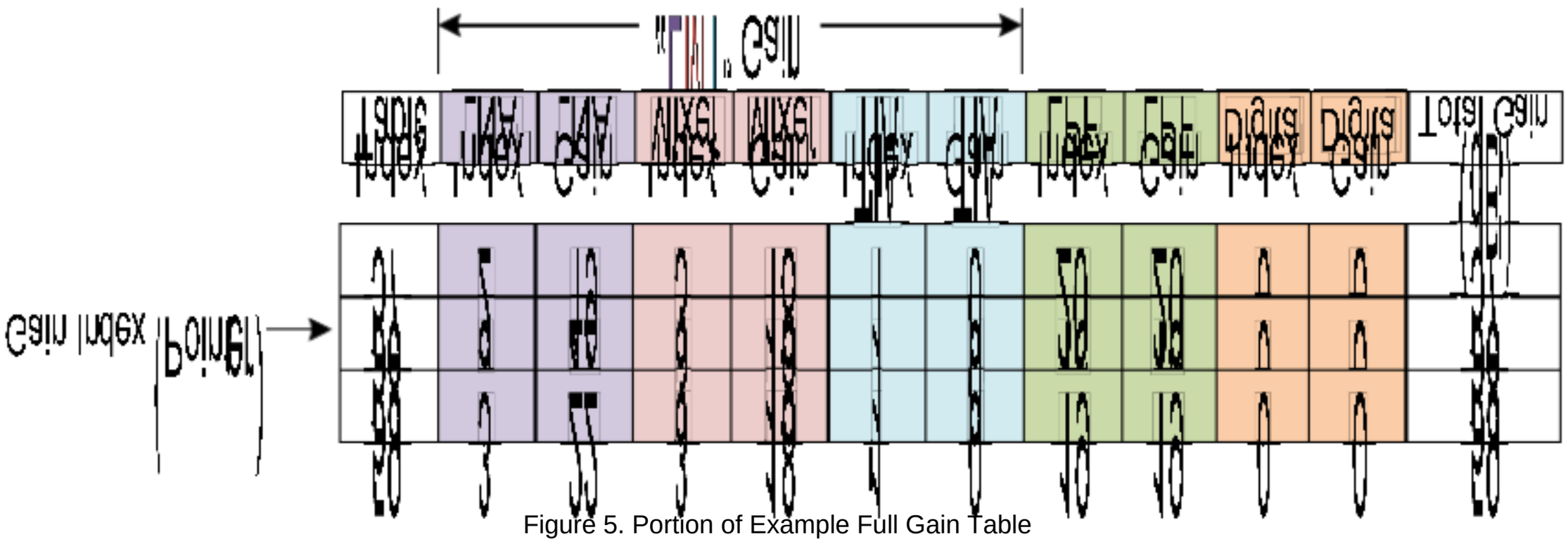

Figure 5. Portion of Example Full Gain Table

Split Table Mode

In situations where high power out-of-band interfering signals are often present, it can be advantageous to split the gain table to optimize noise figure in the presence of these interferers In this case, separate pointers control the LMT gain and the LPF gain independently (and digital gain if it is enabled). This allows the gain to be changed in the area of the receive path that is overloading. Recall that for the full gain table, gain changes could affect any or all of the gain blocks in the receive path regardless of where the overload occurs.

The architecture of the LMT table depends on which gain control mode is used so this aspect is covered in the next sections which cover the various gain control modes in detail. Clearing bit D3 of 0x0FB enables the split table mode. An LMT table must be written to the AD9361. This process is described in the “ Writing to and Reading From the Gain Table ” section later in this document. An L se does not exist. Instead, the LPF index directly translates to LPF gain in dB. The same is true of digital gain (if it is enabled). LPF gain (index) ranges from 0 to 24(d) while digital ranges as mentioned previously from 0 to 31(d).

The total gain in dB of the AD9361 is not necessarily equal to the LMT and LPF indices added together. The actual gain of the LMT stages vary with LO frequency and in addition some of the LMT steps are larger than one dB. Thus, changing the LMT index by one may not change the gain by 1dB. This concept is easier to understand when looking at the tables in the appendices.

The maximum index when using the split table mode is 40(d). The maximum index used by the gain table must be programmed into register 0x0FD.

To read back the split table gain indices in any gain control mode, read the following SPI registers:

Register(hex) F	unction
2B0[D6:D0]	Rx1 LMT Gain Index
2B1[D4:D0]	Rx1 LPF Gain Index
2B2D4:D0][	Rx1 Digital Gain Index (if enabled)
2B5[D6:D0]	Rx2 LMT Gain Index
2B6[D4:D0]	Rx2 LPF Gain Index
2B7D4:D0][	Rx2 Digital Gain Index (if enabled)

Table 2.Reading Split Table Gain Indices

Digital Gain

All modes (MGC , AGC) and both Gain Table modes allow for the addition of digital gain (set by D2 in register 0x0FB). The maximum allowable index for a full gain table is 90(d). The maximum digital index is 31(d). A standard full gain table with only analog gain has a maximum index of 76(d). For the gain tables provided by ADI, this leaves 24(d) indices left over for digital gain. Alternative gain tables that reach their maximum analog gain at an index lower than 76(d) can accommodate more digital gain steps (up to 31). 0x100[D4:D0] sets the maximum digital gain (any value equal to or less than 31(d)).

It is important to point out that digital gain does not increase signal-to-noise (SNR) ratio as it is merely multiplies the digital word by a factor. In this way, both noise and signal are increased and thus SNR remains the same. For many applications, digital gain is not needed. Further, modifying the gain table and sacrificing analog gain in order to add more digital gain will decrease the performance of the system.

In some cases, however, it is desired that the signal power received by the BBP be equal to some nominal value. For very low signal levels in which the maximum analog gain is still not high enough to achieve this goal, digital gain can be used.

Alternatively, a fixed amount of digital gain may be applied. In all gain control modes, setting bit D5 in registers 0x10B and 0x10E enables this function. The BBP writes the digital gain index itself in 0x10B (Rx1) and 0x10E (Rx2). If bit(s) D5 are set, the digital gain never changes.

MANUAL GAIN CONTROL (MGC) MODE

In MGC mode, the BBP controls the gain index pointer(s). In its simplest form, the BBP evaluates the digital signal level at the I/O port and then adjusts the gain appropriately. In this situation, the BBP needs no other information other than the digital signal level that it receives. For the full (single) gain table, this is all that is needed — an overload requires that the gain be decreased.

However, described above, the AD9361 has programmable thresholds that indicate the condition of the signal in each receiver. Routing these signals to the Control Output pins and then connecting them to the BBP inputs allows the BBP to determine the status of the received signals in more detail. For a split gain table, this information allows the BBP to adjust the gain in the area which is overloading because it indicates where the overload is occurring (LMT, LPF, Digital).

The lower nibble of 0x0FA sets the mode of each receiver independently. Bits D3 and D2 set the mode for Rx2 and bits D1 and D0 set the mode for Rx1. Setting those bits to zero enables MGC mode.

MGC Gain Control Methods

The BBP can control manual gain in one of two ways. The default method uses SPI writes of the gain indices. Clearing bit D1 (Rx2) and bit D0 (Rx1) of register 0x0FB sets this mode of control. Alternatively, the BBP can pulse the Control Input pins to move the gain indices. CTRL_IN0 causes the gain index to increase for Rx1 and CTRL_IN1 causes the gain index to decrease for Rx1. Similarly, CTRL_IN2 causes the gain to increase for Rx2 and CTRL_IN3 causes the gain to decrease for Rx2. Setting bits D1 (Rx2) and D0 (Rx1) high enable this control method. Bits D7:D5 of register 0x0FC set the number of gain indices to increase and bits D7:D5 of register 0x0FE set the number of gain indices to decrease. The pulse is asynchronous so setup and hold are not relevant but the time high and low must be at least two ClkRF cycles for the AD9361 to detect the event. ClkRF is the clock used at the input of the Receive FIR Filters.

MGC Full Table Mode

In Full Table Mode, a single index for each receiver controls the gain. If SPI writes are used to control the gain, then writing registers 0x109 (Rx1) and 0x10C (Rx2) set the gain index directly. If Control Input pins are used to control the gain, then pulsing the various pins moves the gain index pointer(s) up and down the full tables.

MGC Split Table Mode

If the BBP uses SPI writes to control the gain, then registers 0x109 (Rx1) and 0x10C (Rx2) control LMT gain while registers 0x10A (Rx1) and 0x10D (Rx2) control LPF gain. Digital gain (if enabled) is controlled by registers 0x10B (Rx1) and 0x10E (Rx2). The split table architecture looks like Figure 6.

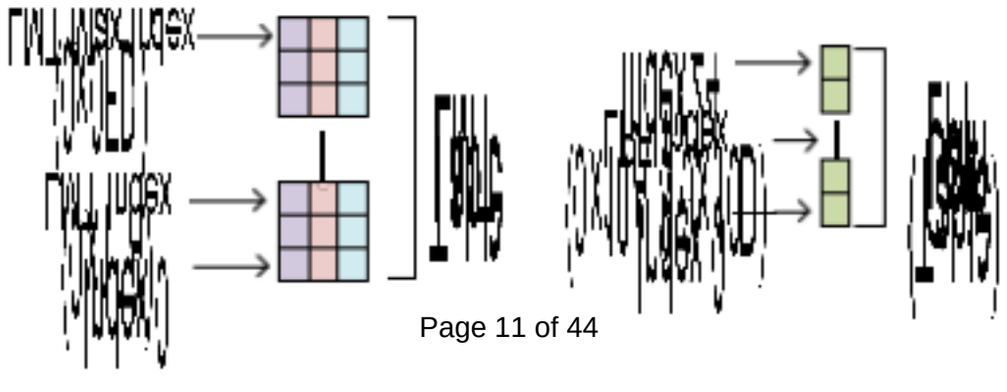

Figure 6.Split Table in Manual Gain Mode, SPI Writes Control Gain Indices

If the BBP uses the Control Inputs to change the gain, then there are two options. There are only four Control Inputs but there are eight different analog gain adjustments to make (LPF, LMT, Rx1, Rx2, increment and decrement for each). One option is to use a SPI bit to determine where the gain index changes (LMT or LPF). Clearing bit 0x0FC[D3] enables this option and 0x0FC[D4] is the bit that selects the gain change location. For this option, the gain table architecture still looks like Figure 6. If digital gain is enabled, the BBP changes this gain by via SPI writes. The CTRL_IN pins do not change digital gain in split table mode.

Alternatively, if bit 0x0FC[D3] is set, the AD9361 peak detectors determine where the gain changes. With this option, the architecture of the split table changes as shown in Figure 7. Note that the LMT table has been split into two sections, an “upper LMT table. The dividing line is at the “LMT Index Limit” which is set in register 0x11A and this setting is common to both receiver

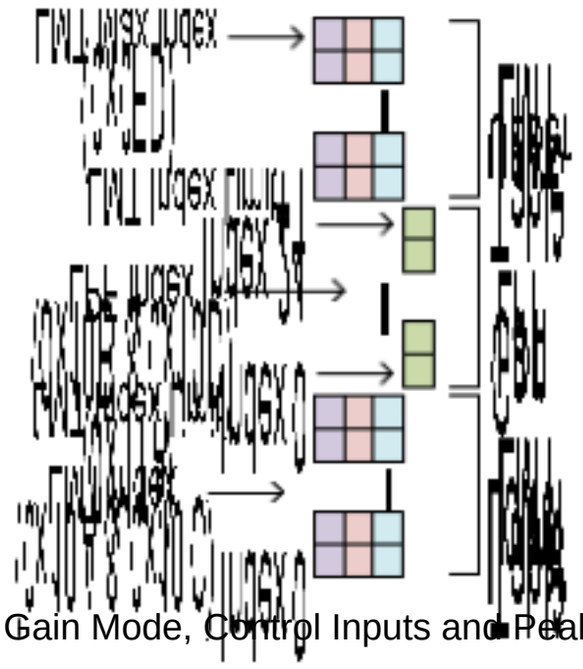

Figure 7. Split Table in Manual Gain Mode, Control Inputs and Peak Detectors Control Gain Indices

Additionally, where overloads occur and where the gain indices are currently pointing affects where the gain changes as noted in Table 3. As the table demonstrates, the algorithm decreases LMT gain first and then, when the LMT index reaches the LMT Index Limit, the type of overload determines where the gain decreases. Increment and decrements registers 0x0FC and 0x0FE set the amount of gain change.

Overload Type	Gain Index Position(s)	Change Gain in
Large LMT	LMT Index > 0	LMT Table
Large LMT	LMT Index = 0	LPF Table
Large or Small ADC	LMT Index is in Upper LMT Table (Index > “Initial LMT Gain Limit”	LMT Table)
Large or Small ADC	LMT Index is in Lower LMT Table (Index ≤ “Initial LMT Gain Limit”	LPF Table)
Digital Saturation	N/A	Digital Table

Table 3.Manual Gain Split Table Gain Change Location vs. Index Position and Overload Location

If more than one overload condition occurs simultaneously, then LMT overloads are first priority, ADC overloads are second, and Digital Saturation is third.

AGC SLOW ATTACK

Slow Attack Mode is intended for slowly changing signals such as those found in some FDD applications such as WCDMA and FDD LTE. The Slow Attack AGC uses a 2nd order control loop with hysteresis that changes the gain in order to keep the average signal power within a programmable window. The power is measured between HB1 and the Rx FIR filter. This is the same location as the Detector” in Figure 3. In addition, the BBP can set bits to enable faster reactions for signals that exceed the LMT and ADC thresholds. Enable AGC Slow Attack Mode by setting bits D3:D2 (Rx2) to 2’b10 and/or bits D1:D0 (Rx1) to 2’b10 in register 0x0FA and the “Slow Attack Hybrid Mode” bit D4 in 0x0FA is clear.

AGC Slow Attack Control Loop

The figure below demonstrates the concept of the control loop.

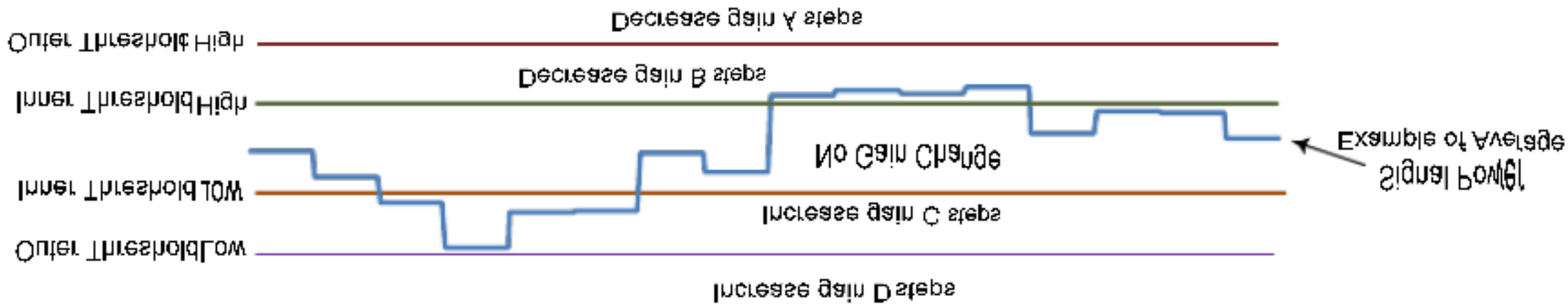

Figure 8.Slow Attack AGC Control Loop Limits and Step Sizes

Where

“ Inner Threshold High ” is stored in register 0x101 in – dBFS

“ Inner Threshold Low ” is stored in register 0x120 in – dBFS

Register 0x129[D7:D4] stores the absolute value of the difference in dB between the “ Inner Threshold High ” and

Register 0x129[D3:D0] stores the absolute value of the difference in dB between the “ Inner Threshold Low ” and th
Low ”

The “ A ”, “ B ”, and “ D ” step sizes are stored in registers 0x12A[D7:D4], 0x123[D6:D4], 0x123[D2:D0], and 0x12A[D3:D0] respectively.

The step sizes above determine how much the gain index pointer(s) change after the average signal power exceeds a threshold. Seethe “Average Signal Power” section for details on how signal power is measured.

Note that the AD9361 does not have default thresholds or step sizes. The BBP must write all of these values.

Setting the Gain Update Time

When the average signal power exceeds a threshold, the gain does not necessarily change immediately. In FDD systems, there are typically brief periods (such as those around slot boundaries) that accommodate gain changes or other system parameter updates. To accommodate this aspect of FDD protocols, the AD9361 gain will only update after the “ Gain Update Counter ” store and 0x125 expires. The counter is clocked at the ClkRF rate (the input rate of the RFIR). The depth of the counter is equal to double the value in these registers. Or, if bit D5 of 0x128 is set, it is equal to 4x the value in these registers.

The counter clock begins running three clock cycles after the AD9361 enters the receive state. Since the BBP is responsible for moving the AD9361 among its states, it can determine when the gain update counter will expire. In this way, the Counter can be set such that it always expires at slot (or other) boundaries.

If the “ Enable Sync for Gain Counter ” bit D4 in register 0x128 is set, the BBP can reset the counter (synchronize it) by transitioning CTRL_IN2pin high. The gain will also update.

The slow AGC is typically configured to have multiple power measurement cycles within each gain update period. The last power measurement performed before a gain update boundary determines whether (and by how much) the gain should change.

LMT , ADC, and Digital Saturation Overloads in Slow Attack AGC Mode

In addition to the control loop discussed above, the Slow Attack/Hybrid AGC can react more quickly to “ peak ” ov the LargeLMT and LargeADC overloads.

In the slow attack mode, the AD9361 counts the number of times a particular overload event occurs. Only if the event(s) occur more than a programmable number of times will the gain change. Even for these peak overloads, the gain only changes when the Gain Update Counter expires. The counters are stored in registers 0x121 (LMT) and 0x122 (ADC). The AD9361 does not have default values for these counters so the BBP must write all of these values.

During the a gain change event, the highest priority is given to the large LMT detector, followed by the large ADC detector, and followed lastly by the power detectors used by the 2nd order window control loop.

It is also possible to setup the AD9361 such that Large LMT Overloads and/or Large ADC Overloads result in an immediate gain change, ignoring the Gain Update Counter. Bit D7 of 0x123 high sets this mode for Large LMT Overloads and bit D3 of the same register sets this mode for Large ADC Overloads. These bits do not have defaults in the AD9361 so the BBP must set or clear them for desired operation.

If the average signal power exceeds one or both of the control loop “ Low Thresholds ” (which would normally result in a gain one or both of the Small Peak Overload detectors (LMT or ADC) has tripped, setting bit D7 of 0x120 will prevent the gain from increasing. This bit does not have a default in the AD9361 so the BBP must set or clear it for desired operation.

Like LMT and ADC overloads, the AD9361 uses a counter (0x128[D3:D0]) to determine how many times digital saturation has occurred. If this counter is exceeded, the gain index is reduced.

Slow Attack AGC Full Gain Table

In this mode, a single table controls the gain of all Rx signal path stages. The table below shows the effect of Peak Overloads (after their associated counters are exceeded).

Peak Overload	Reduce Gain by this many Indices (Step Size)	Step Size stored in this Register
Large LMT	Dec Step Size for Large LMT Overload	0x103[D4:D2]
Large ADC	Decrement Step Size for Large LPF Gain Change	0x106[D3:D0]
Digital Saturation	Digital Gain Step Size + 1	0x100[D7:D5]

Table 4.Slow Attack/Hybrid AGC Full Gain Table Overload Steps

Recall that a particular overload condition results in the gain index moving a programmable number of steps but the gain may change in any number of different gain blocks.

Slow Attack AGC Split Gain Table

In this mode, the gain table is split as described in the Split Gain Table section earlier in the document and as shown in Figure 9.

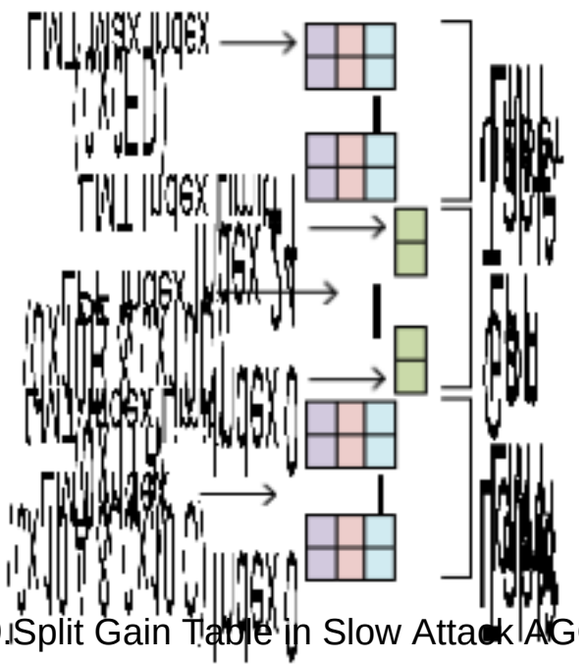

Figure 9.Split Gain Table in Slow Attack AGC Mode

In a split table, there are two independent index pointers for analog gain and one additional pointer for digital gain (if enabled). Table 5 describes the effect of various peak overload conditions, identical to split table shown in the manual gain section. If gain changes in the LPF table, the LPF step size is used in 0x106[D3:D0]. Similarly, if the gain is changed in the LMT table, the step size in 0x103[D4:D2] is used.

Overload Type	Gain Index Position(s)	Change Gain in
Large LMT	LMT Index > 0	LMT Table
Large LMT	LMT Index = 0	LPF Table
Large or Small ADC	LMT Index is in Upper LMT Table (Index > "Initial LMT Gain Limit")	LMT Table
Large or Small ADC	LMT Index is in Lower LMT Table (Index ≤ "Initial LMT Gain Limit")	LPF Table
Digital Saturation	N/A	Digital Table

Table 5.Slow Attack/Hybrid AGC Split Gain Table Overload Steps

AGC HYBRID MODE

The AGC hybrid mode is the same as the slow AGC mode with the exception that the gain update counter is not used. Instead, gain updates occur when the BBP pulls the CTRL_IN2 signal high. The "hybrid" term arises because the BBP has taken some co algorithm away from the AD9361 so gain control is no longer completely automatic. Hybrid mode is enabled by setting the Hybrid Mode" bit 0x0FA[D4] high and by setting the "Gain Control Mode" bits in the lower nibble of 0x0FA to D3:D2 = 2'b11 enables hybrid mode for Rx2 and D1:D0 = 2'b11 enables hybrid mode for Rx1.

AGC FAST ATTACK MODE

Fast Attack Mode is intended for waveforms that "burst" on and off, such as those found in TDD applications or GSM/EDGE FD applications. The AGC responds very quickly to overloads at the start of a burst so that the AGC can settle to an optimum gain index by the time the data portion of the signal arrives. The AGC also has an optional slow decay that allows the gain to increase if the signal power decreases while the AGC is locking to an optimum gain. Enable Fast Attack AGC Mode by setting bits D3:D2 (Rx2) to 2 and/or bits D1:D0 (Rx1) to 2'b01.

When the AD9361 enters the Rx state, the Fast Attack AGC State Machine leaves state 0 and enters state 1 as shown in Figure 10. Its goal is to adjust the gain index such that an optimum receive gain is realized in a very short period of time. The AGC progresses through several states on its way to "Gain Lock" state, in which the gain does not change ("unlock") unless large signal level changes occ burst ends. When the gain unlocks, the AGC State Machine moves back to its Reset State and starts over. The figure below shows a high-level diagram of the AGC states.

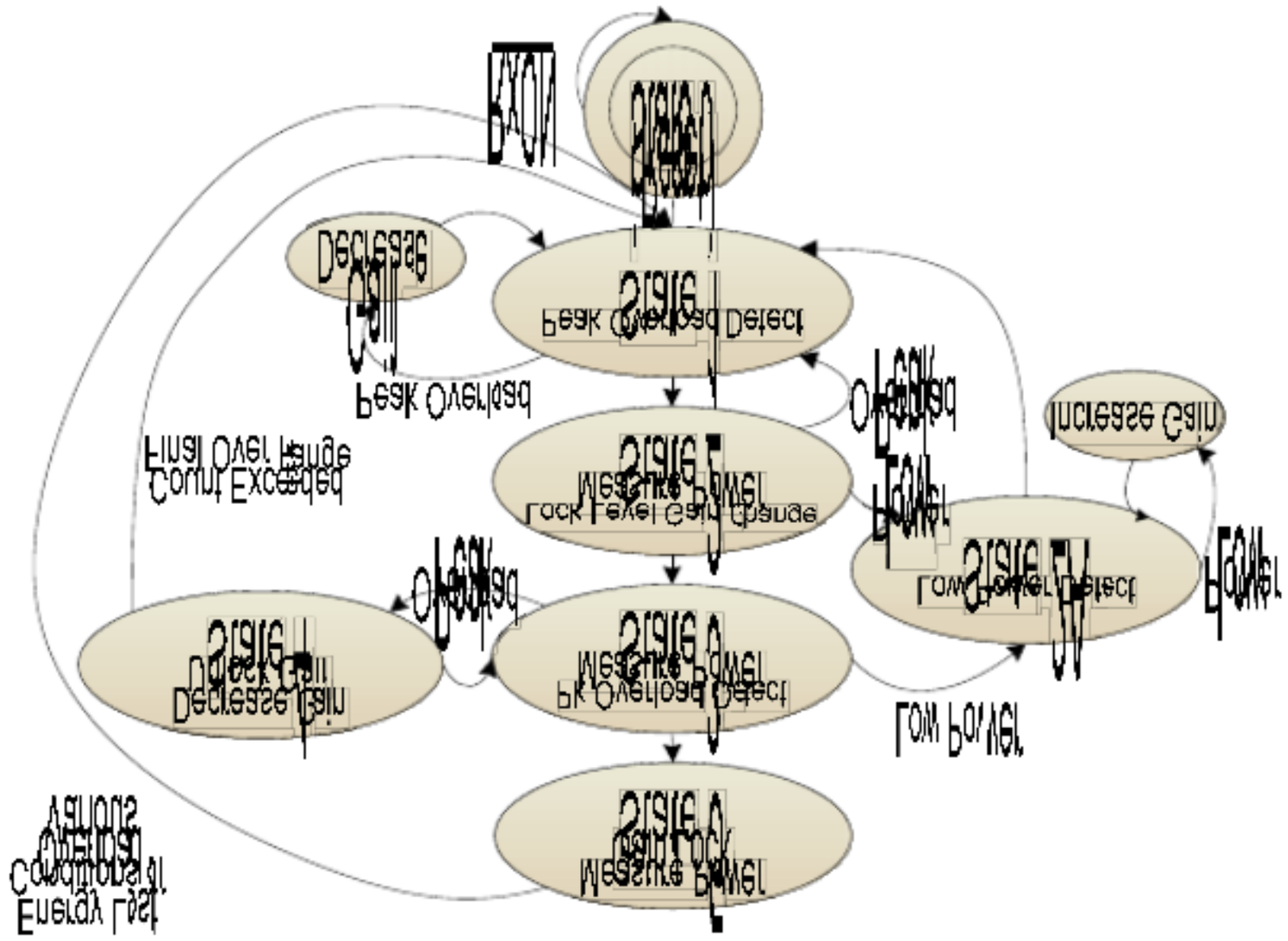

Figure 10.Fast Attack AGC High Level Stage Diagram

State 0 (Reset)

The AGC remains in this state when the AD9361 is not in the Rx state. The AGC performs no actions while in this state.

State 1 (Peak Overload Detect)

When the AD9361 enters the Rx state, the AGC first waits for a time in microseconds set by the "AGC Attack Delay" in register 0x022. This delay allows the receive path to settle before the AGC begins determining the optimum gain index.

After this delay, the AGC enters State 1, where it detects peak overloads (LMT and ADC) and adjusts the gain. The digital saturation detector is also enabled but in state 1the signal may not have enough time to reach the detector. Each time the gain changes, the AD9361 holds the peak detectors in a reset state until the"Peak Overload Wait Time" counter expires. If no peak overloads are detected for the "Energy Detect Count" time in register 0x117[D4:D0], then the AGC can proceed to state 2. The Energy Detect Counter is clocked at the ClkRF rate (the clock used at the input to the Rx FIR Filter).

The overloads affect the gain index in different ways for different gain table types as shown in the tables below. In Full Gain Table Mode, the AD9361 uses different step sizes (changes in gain index) for differing extremes of overload. Table 6 shows where the step sizes are stored for the fast attack AGC in full table mode. The case #1 step size is typically larger than case #2 which itself is typically larger than case #3.

Table 7 shows the effects of various overloads when using a split table. Figure 11 shows the split table architecture. Note that the gain first decreases from the LMT table regardless of where the overload occurs. When the gain index reaches the LMT Index Limit, the gain decreases where the overload occurs.

Peak Overloads	Reduce Gain by this many Indices (Step Size)	Step Size set by
Large ADC Λ (Large LMT V Digital Sat)	"Decrement Step Size for Full Table Case #1"	0x106[D3:D0]
Large ADC V Large LMT V Digital Sat	"Fast Attack Only. Decrement Step Size for Full Table Case #2"	0x106[D6:D4]
Small ADC	"Dec Step Size for Full Table Case #3"	0x103[D4:D2]

Table 6.Fast Attack AGC Peak Overload Step Sizes for Full Gain Table

Overload Type	Gain Index Position	Change Gain in
Large LMT	N/A	LMT Table
Large or Small ADC	LMT Index is in Upper LMT Table (Index > “Initial LMT Gain Limit”)	LMT Table
Large or Small ADC	LMT Index is in Lower LMT Table (Index ≤ “Initial LMT Gain Limit”)	LPF Table
Digital Saturation	N/A	Digital Table

Table 7. Fast Attack AGC Peak Overload Step Sizes for Split Gain Table

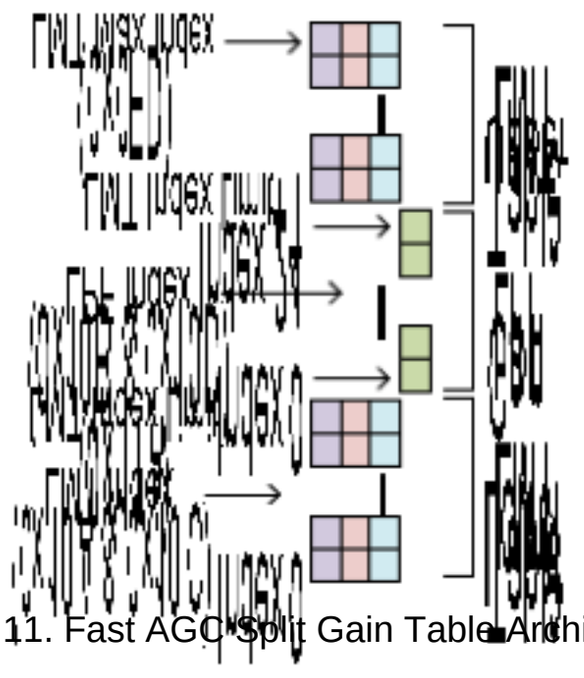

Figure 11. Fast AGC Split Gain Table Architecture

State 2 (Measure Power & Lock Level Gain Change)

Upon entering State 2, the AGC waits for a time equal to Settling Delay – “Energy Detect Count”. Recall that the Settling Delay in ClkRF cycles is equal to twice the value in register 0x111[D4:D0]. The subtraction is performed because the AGC has already waited for the Energy Detect Counter to expire in order to exit State 1. Thus, the delay before measuring power does not need to count through this delay again. After the delay calculated above, the AGC measures average signal power at the output of the HB1 filter.

The AGC keeps the LMT, ADC, and Digital Saturation overload detectors enabled while it is in State 2. If overloads occur, the AGC will go back to State 1 to reduce the gain.

If the “Enable Incr Gain” bit (D0 of 0x110) is set, then the AGC is allowed to increase gain if the average signal power stays below th Low Power Threshold for a time greater than the “Increment Time”. The gain step size used equals the value in register 0x117[D7:D5] + 1. The gain continues to increase until the signal does not remain below the Low Power Threshold longer than the Increment Time. The state diagram above shows this as State 2A. The AGC exits State 2A by going back to State 1 to check again for Peak Overloads.

If the AGC has entered State 2 and does not detect a Low Power condition (or “Enable Incr Gain” is cleared), then th power is compared against the “AGC Lock Level (Fast)” setting in register 0x101. The AGC then adjusts the gain to match the average signal power to the AGC Lock Level setting. The Lock Level is stored in – dBFS in a resolution of 1dB/LSB. If the gain ne to achieve the lock level setting, then there is a maximum amount that it can increase, set by “AGC Max Increase” in 0x118.

In the Full Gain Table mode, the AGC simply changes the Gain Index such that the signal power matches the lock level (unless limited by 0x118). In Split Table mode, if the “Enable LMT Gain Inc for Lock Level” bit (D6 of 0x111) is set high, the actions are per

If gain needs to	Do this first	And if	Then Do This
Decrease	Reduce LPF Gain Index	LPF Gain Index = 0	Reduce LMT Gain Index
Increase	Increase LMT Gain up to LMT Step Size	Total Gain Change > LMT Step Size	Increase LPF Gain Index

Table 8.Fast Attack AGC Lock Level Gain Index Change for Split Gain Table

If 0x111[D6[is not set high, then only LPF gain can be used for gain increases. In addition, regardless of the setting of 0x111[D6], if a small LMT overload occurs during the lock level calculation, LMT gain will not be allowed to increase to meet the Lock Level.

State 3 (Measure Power & Peak Overload Detect)

When the AGC enters State 3, it locks the Gain. This state can affect other portions of the AD9361 such as DC Offset Tracking updates and RSSI measurement start times.

The AGC continues to measure power and it keeps its Large LMT, Large ADC, and Digital Saturation overload detectors enabled.

If the "Enable Gain Inc after Gain Lock" bit (D7 of 0x110) is set (and "Enable Incr Gain" bit (D0 of 0x110) is set), then to see if a Low Power condition occurs. The method used is the same as that used in State 2 (including the transition to State 1 if the gain must increase). If 0x110[D7] is low, then the AGC does not perform the low power test in State 3. If the AGC exits State 3 due to a Low Power condition, the Gain Unlocks.

If the thresholds have been set correctly, then the overload detectors should not assert even after the lock level adjustment unless the signal-of-interest level increases or an out-of-band blocker is suddenly present. To guard against these possibilities, the AGC monitors its overload detectors. If overloads occur after the lock level adjustment, the AGC uses different step sizes to change the gain.

In Full Gain Table Mode, regardless of the type of overload, the step size (number of indices reduced) is always the "Post Lock Level Step Size for Full Table" value in 0x112[D7:D6]. In Split Gain Table Mode, the step size is the "Post Lock Level Step Size for LPF Table" (0x112[D7:D6] for ADC overloads and the "Post Lock Level Step for LMT Table" (0x113[D7:D5]) for LMT overloads. These step sizes are usually smaller than those used in States 1 and 2. States 1 and 2 overload step sizes are designed to respond to large overloads very quickly. The overload that may occur in State 3 would normally be smaller and require less adjustment.

If these overloads occur, the AGC decreases gain in State 4. The Gain Unlocks while the AGC is in State 4. The AGC then returns to State 3.

The AGC counts the number of overload conditions that occur after the Lock Level adjustment. If this number exceeds the Range Count" in 0x16[D7:D5], then the AGC goes back to State 1 and resets its peak detectors.

State 5 (Gain Lock and Measure Power)

When the AGC reaches State 5, the AGC locks the Gain (if it was unlocked). The AGC also measures the average signal power when the gain locks and stores this value as a reference power level. This value is used for comparisons against other thresholds, which can unlock the gain. State 5 is the final state in the AGC algorithm and is intended to maintain the same gain unless a large change in signal amplitude occurs (such the end of the burst or subframe or a large interfering signal suddenly arrives or deaparts). In states 2 and 3, the setting in 0x15C[D3:D0] controls the power measurement duration. In state 5, 0x109[D7] and 0x10A[D7:D5] control the power measurement duration. The mapping of bits to duration is the same for both sets of registers and is defined in Equation 8. The reason for the difference is that in earlier states, the object is to lock the gain as quickly as possible. This would mean that a shorter measurement time may be used for earlier states but a longer time can be used once the gain has locked.

$$16$$

Equation 8

When the gain unlocks, the AGC can reset the gain to maximum gain or to one of several other gain positions as shown in Table 9. When the gain unlocks, the AGC returns to State 1 (or State 0 if the AD9361 exits the Rx state). When the AGC returns to State 1, it sets the digital gain to 0dB (unless the digital gain is forced as described in the digital gain section). Optimize Gain and Set Gain both can reduce the time required for gain lock since they both use the previous burst gain index information.

Gain Index when Reset	Set by	Definition
Max Gain	Maximum Full Table or Maximum LMT Table Index (0x0FD) and Maximum LPF of 0x18	Maximum Analog Gain
Optimize Gain	AGC Gain Lock Index at end of last burst Plus Optimize Gain Offset (0x116[D3:D0])	An optimized value that reduces the amount of steps the AGC should typically take to Lock the gain for each burst
Set Gain	AGC Gain Lock Index at the start of the last burst Or	Similar to Optimize Gain but allows use of front of burst gain or end of burst gain setting

	AGC Gain Lock Index at the end of the last burst	
No Gain Change	N/A	No change to the Gain Index

Table 9.Gain Unlock Index Options

Bit D7 of 0x111 determines whether Set Gain uses the beginning or ending Gain Lock Index of the previous burst. Setting the bit causes the AGC to use the ending Index. The front of the burst would typically be used if a preamble or boosted portion of the signal occurs at the beginning of the burst. The AGC should lock on that boosted portion. If the entire burst uses the same nominal power level, then the AGC should use the end of the burst gain index.

If the thresholds are set correctly, then the most likely scenario is for the AGC to unlock the gain at the end of the burst (if the AD9361 exits the Rx State. In addition to the unlock conditions just mentioned, the Test for a “ Stronger and unexpected change in the signal of interest power (usually due to an unexpected interfering signal). Unlocking the gain for an ADC overload is similar to the stronger signal test but is a peak detector rather than a power detector. Unlocking the gain for a large LMT overload checks for large interfering signals and is a peak detector. All of these tests are recommended for a typical fast AGC configuration. Even in this simple case, there are options for what happens to the Gain Index when the gain unlocks. Table 10 shows these options.

Condition that Unlocks the Gain	Gain Index Type*	Set Bits	Clear Bits
Exit Rx State	Max Gain	None Required	0x110[D4], 0x110[D2]
Exit Rx State	Optimize Gain	0x110[D2]	0x110[D4]
Exit Rx State	Set Gain	0x110[D4]	0x110[D2]
Energy Lost Threshold Exceeded	Max Gain	None Required	0x110[D6]. 0x110[D3] only if 0x0FB[D6] set
Energy Lost Threshold Exceeded	Optimize Gain	0x110[D6]	0x110[D3] only if 0x0FB[D6] set
Stronger Signal Threshold Exceeded	No Change	None Required	0x115[D7] if 0x0FB[D6] set
Large ADC Overload	No Change	None Required	0x114[D7] and 0x110[D1] if 0x0FB[D6] set
Large LMT Overload	No Change	None Required	0x110[D1] if 0x0FB[D6] set

Table 10.Gain Unlock Condition vs. Gain Index

*A gain index type of “ No Change ” indicates that the gain index does not immediately change but the AGC algorithm does start over so the gain index will very likely change after the AGC moves through its states and re-locks. For other gain index types such as , the AGC first changes the gain index to the proper position and then restarts the algorithm.

When comparing the signal power with the energy lost threshold, there is also a time factor as well. Each time the signal power value updates, the AGC computes the difference between the power measured at the beginning of Gain Lock and the current signal power. This difference is compared against the Energy Lost Threshold stored in register 0x112[D5:D0]. If the difference exceeds the threshold for a time equal to twice the “ Gain Lock Exit Count ” stored in 0x119, the gain unlocks as shown in the table above. The Gain L Counter is clocked at the ClkRF rate. The same comparison is made for the “ Stronger Signal Threshold ” stored in and which appears in the table below.

The large ADC threshold is stored in 0x105 and the large LMT threshold is stored in 0x108. For the peak detectors, there are no time requirements. A single overload will unlock the gain.

Generally, the AGC is the best arbiter of when the gain should unlock. However, in some situations, it may be advantageous for the BBP to initiate an unlock condition. If the BBP pulls the EN_AGC pin high, the gain will unlock and the AGC algorithm will restart. The BBP cannot force the gain to lock at a certain time but it can control when the gain unlocks. Table 11 shows how to use this feature.

Condition that Unlocks the Gain	Gain Index Type	Set Bits	Clear Bits
EN_AGC pulled High	Max Gain	0x0FB[D6], 0x111[D5]	0x110[D6:D5]
EN_AGC pulled High	Optimize Gain	0x0FB[D6], 0x110[D6], 0x111[D5]	0x110[D5]

EN_AGC pulled High	Set Gain	0x0FB[D6], 0x110[D5]	0x111[D5]
EN_AGC Pulled High	No Gain Change	0x0FB[D6]	0x110[D5], 0x111[D5]

Table 11.Full List of Gain Unlock Conditions vs. Target Gain Index

If the thresholds are set correctly, the typical setup which unlocks the gain when the AD9361 exits Rx mode or if the burst/subframe ends is sufficient for most applications. However, if desired, it is also possible to prevent the gain from unlocking in some instances. Table 12 shows these options. The settings are dependent on whether the BBP will use the EN_AGC pin to unlock the gain. If this is the case, then the EN_AGC pin should be low except when the gain should be unlocked. If the EN_AGC pin is not used, then the Delay ” bit (0x014[D1]) must be set high.

EN_AGC Pin Used?	Don’t Unlock Gain Even If:	Set Bits
N	Energy Lost Threshold Exceeded	0x0FB[D6], 0x014[D1], 0x110[D3]
N	Stronger Signal Threshold Exceeded	0x0FB[D6], 0x014[D1], 0x115[D7]
N	Large ADC or Large LMT Overload	0x0FB[D6], 0x014[D1], 0x110[D1]
Y	Energy Lost Threshold Exceeded	0x0FB[D6], 0x110[D3]
Y	Stronger Signal Threshold Exceeded	0x0FB[D6], 0x115[D7]
Y	Large ADC or Large LMT Overload	0x0FB[D6], 0x110[D1]

Table 12.Preventing Gain Unlock Conditions in State 5

WRITING TO AND READING FROM THE GAIN TABLE

This section shows how to modify the gain tables (one for each receiver path) that the AD9361 uses for all gain control modes. In Split Table Mode, the LPF gain not programmed. LPF gain equals the LPF index and this relationship cannot be modified.

The gain table is an indirectly addressable set of registers in the AD9361, accessed by SPI registers 0x130 through 0x137. Table 13 shows the registers used for reading and writing.

REG ADDR	NAME	D7	D6	D5	D4			D3	D2	D1	D0	F	DE AULT	R/W
130	G ain Table Word Address	Open	G	ain Table Word Address<6:0>									--h	R/W
131	G ain Table Word Write Data1	LNA Ext Ctrl		LNA Gain <1:0>		Mixer Gm Gain <4:0>							--h	R/W
132	G ain Table Word Write Data2	Open				TIA Gain	LPF Gain <4:0>						--h	R/W
133	G ain Table Word Write Data 3	Open				RF DC Cal	Digital Gain <4:0>						--h	R/W
134	G ain Table Word Read Data 1	LNA Ext Ctrl		LNA Gain <1:0>		Mixer Gm Gain <4:0>							--h	R
135	G ain Table Word Read Data 2	Open				TIA Gain	LPF Gain <4:0>						--h	R
136	G ain Table Word Read Data 3	Open				RF DC Cal	Digital Gain <4:0>						--h	R
137	G ain Table Config	Open						Receiver Select<1:0>	Write Gain Table	Start Gain Table Clock	Open		08h	R/W

Table 13.Gain Table Registers

The gain table index to be accessed is the “ Gain Table Word Address ” in register 0x130.

The various gain block indices map to actual gain per the following tables. Note that these are nominal values and some variation with carrier frequency, temperature, and process is expected for the LNA and mixer tables.

Internal LNA Index	Internal LNA Gain (dB)
0 3	
1 14	
2 17	
3 21	

Table 14.LNA Gain vs. Index

Mixer Gm Index (d)	Mixer Gm Index Gain (dB)
0 0	
1 3	
2 9	
3 – 15	= Index + 11

Table 15.Mixer Gm Gain vs. Index

TIA Index	Internal LNA Gain (dB)
0 -6	
1 0	

Table 16. TIA Gain vs. Index

LPF Index (d)	LPF Gain (dB)
0 – 24	= Index

Table 17. LPF Index vs. Gain

Digital Index (d)	Digital Gain (dB)
0 – 31	= Index

Table 18. Digital Index vs Digital Gain

Table 19 shows a small portion of an example full gain table.

It is important to note that the BBP only uses the values in the “Total Index” column as well as the green columns when programming a gain table into the AD93

Starting at the far left of Table 19, “Table Index” is the index or pointer to the table. When the AD9361 is in the FDD or recei index controls the receive path gain and the BBP sets it by writing to register 0x109 for Rx1 and 0x10C for Rx2.

The next column to the right is the external LNA index. The next section describes in detail how the AD9361 can control an external LNA. Briefly, a bit in the gain table can be output to a GPO and used to control the gain of an external LNA. The next column to the right is the external LNA gain. This column has no purpose except to indicate total receive path gain when using an external LNA.

Moving to the right again leads to the iLNA Index. This is the internal LNA index, which controls LNA gain. iLNA Gain in dB is next to iLNA Index which is only used to add to other stages gains and which result in the total receive path gain. Note that the gain tables map gain index accurately to the actual gain of the stage. Table 14 and Table 15 are for reference since the internal LNA and the mixer gains vary with LO frequency.

Again moving to the right results in the Mixer Index and next to that column is the Mixer Gain, both of which are analogous to the iLNA Index and iLNA Gain described previously.

The “0x131” column to the right is the digital word that is a concatenation of all of the previous indices. When writing a gain table to the AD9361, after writing the “Table Index” value into register 0x130, the BBP would write the value in the 0x131 column at that Table Index into register 0x131. See the programming example below for specific details.

The TIA Index and TIA Gain are related as described previously for other gain stages. The LPF Index is always equal to the LPF gain in dB so only the index column is shown. “0x132” is a concatenation of the TIA and LPF indices.

The “DC Cal” bit is described in the paragraph after Table 20.

Digital gain, like the LPF gain, is equal to the digital index so only the index column is shown. “0x133” is a conc
bit and the Digital Index.

Finally, the total gain column shows the total Rx path gain of the AD9361 for each gain index.

Table Index	eLNA Index	eLNA Gain	iLNA Index	iLNA Gain	Mixer Index	Mixer Gain	0x131	TIA Index	TIA Gain	LPFIndex	0x132	DC Cal	Digital Index	0x133	Total Gain
0	0	0	0	5	0	0	0	0	-6	0	0	1	0	20	-1
1	0	0	0	5	0	0	0	0	-6	0	0	0	0	0	-1
2	0	0	0	5	0	0	0	0	-6	0	0	0	0	0	-1
3	0	0	0	5	0	0	0	0	-6	1	1	0	0	0	0
4	0	0	0	5	0	0	0	0	-6	2	2	0	0	0	1
5	0	0	0	5	0	0	0	0	-6	3	3	0	0	0	2
6	0	0	0	5	0	0	0	0	-6	4	4	0	0	0	3
7	0	0	0	5	0	0	0	0	-6	5	5	0	0	0	4
8	0	0	0	5	1	3	1	0	-6	3	3	1	0	20	5
9	0	0	0	5	1	3	1	0	-6	4	4	0	0	0	6
10	0	0	0	5	1	3	1	0	-6	5	5	0	0	0	7
11	0	0	0	5	1	3	1	0	-6	6	6	0	0	0	8
12	0	0	0	5	1	3	1	0	-6	7	7	0	0	0	9
13	0	0	0	5	1	3	1	0	-6	8	8	0	0	0	10

Table 19. Portion of Example Gain Table

Table 20 shows how to write Table Index Entries 10(d) and 11(d) of the table shown in Table 19 into Rx1.

Operation	Address (hex)	Data(hex)	Comment
SPI Write	137	0A	Start Clock, Accessing Rx1
SPI Write	130	0A	Gain Index = 10(d)
SPI Write	131	01	Ext LNA Index = 0, Int LNA Index = 0, Mixer Index = 1
SPI Read	132	05	TIA Index = 0, LPF Index = 5 For Split Table, LPF gain is don’t care
SPI Read	133	00	No DC Cal* at this index, Digital Index = 0 For Split Table, the DC Cal bit is ignored (all LMT indices force a DC Cal)
SPI Write	137	0E	Set Write Bit
WAIT			Wait a duration of at least 2 Rx sample periods (at the Rx data rate) for the written values to latch into the AD9361
SPI Write	130	0B	Gain Index = 11(d)
SPI Write	131	00	Ext LNA Index = 0, Int LNA Index = 0, Mixer Index = 1
SPI Write	132	06	TIA Index = 0, LPF Index = 6 For Split Table, LPF gain is don’t care
SPI Write	133	00	No DC Cal* at this index, Digital Index = 0 For Split Table, the DC Cal bit is ignored (all LMT indices force a DC Cal)
SPI Write	137	0E	Set Write Bit
WAIT			Wait a duration of at least 2 Rx sample periods (at the Rx data rate) for the written values to latch into the AD9361

Table 20.Example Gain Table Access

RF DC Cal Bit

*The “RF DC Cal” bit is set for unique combinations of LMT gains. Setting this bit forces the RF DC Calibration algorithm to reduce RF DC offset at those gain indices that involve unique LMT gain settings. In a split gain table, each index will have this bit set as each index

is likely a unique LMT gain configuration. In a full table, each index will not have a unique LMT gain setting. There may be several gain indices using the same LMT configuration while the LPF gain changes for each index. In this case, set the RF DC Cal bit in the lowest index of the unique LMT gain. In Table 19, note that the RF DC Cal bit is set for index 0 but not set for indices 1 through 7. In all of these indices, only LPF gain is changing so the RF DC Cal bit is only set for one index. The RF DC offset correction words used for index 0 is also used for the higher indices.

Maximum Full Table/LMT Table Index

All ADI suggested gain tables have a maximum full table index of 0x4C. The split table maximum index is 0x28. The table/LMT table index ” in register 0x0FD sets the highest gain table index that is calibrated as described in the RF DC Cal Bit section. The chip default is 0x4C so if a suggested full table is used, no change is required for 0x0FD. If the BBP programs a gain table with a different maximum index or a split table is used, 0x0FD must be changed to the proper maximum index value.

EXTERNAL LNA

An external LNA may be added to the receive path to improve the system noise figure. All gain control modes work seamlessly with external LNAs, whether they are fixed gain devices or devices that can be bypassed with the use of a control signal. Note that the maximum level allowed at an AD9361 RF pin is +2.5dBm peak. The system engineer should perform an analysis of the maximum possible signal at the external LNA input added to the external LNA gain to determine if the external LNA gain is acceptable. If the signal level at the AD9361 RF input will be greater than the maximum allowable level, then an external LNA with lower gain or an attenuator must be used.

FIXED-GAIN EXTERNAL LNA

Fixed-gain LNAs are external amplifiers that always provide a nominal amount of gain. This gain is not controllable and the LNA cannot be bypassed. In this case, there are no programming changes necessary for the AD9361.

VARIABLE-GAIN EXTERNAL LNA

Variable-gain external LNAs use a control signal to select between two different gains. Usually one is the “ hig is the “ low gain ” or “ bypass ” setting (which is typically a loss). The external LNA would use high gain in most conditions unless the to the internal LNA is too high (+2.5dBm peak). For those conditions, the external LNA would use low gain (bypass mode).

If manual gain mode is used, then there are two methods of controlling the external LNA gain. In the first method, the BBP controls the gain using a GPO pin connected to the external LNA. Since the BBP controls the gain in the AD9361, it also can control the gain of the external LNA. In the second method, the gain table in conjunction with an AD9361 GPO controls the external LNA. A bit in the gain table (0x131[D7]) drives GPO0 for Rx1 and GPO1 for Rx2. Writing this bit to a zero results in a low GPO output level while a one results in a high GPO output level. See the Accessing the Gain Table” section for more information about gain table bits and modifying gain tables. To route the external LNA bits set in the gain table to GPO pins, set bit D5 (for Rx1) and/or D6 (for Rx2) of 0x026 high.

For AGC modes, the AD9361 must control the external LNA gain since the changes will occur quickly and the BBP will not have knowledge of the gain index that is used until it is selected by the AGC.

Every time the gain changes, the gain control algorithm waits for a duration equal to the Peak Wait Time” while the analog signal path settles. This value should be increased to allow for the settling time of the external LNA, otherwise, the peak detectors will be enabled before the analog stages have settled.

If the AD9361 will be used to measure RSSI, then register 0x12C should be programmed with the external LNA high gain value and register 0x12D should be programmed with the external LNA low gain value. The part considers both values to represent positive gain in the front end prior to the AD9361. Both registers use 0.5dB/LSB resolution and range from 0 to 31.5dB.

In order to account for a low gain value that its negative, register 0x12C can be programmed with the high gain value less the low gain value (e.g. high gain value = 15dB, low gain value = -5dB, program 0x12C = 20dB). This will prevent a step in the RSSI value when the external LNA goes from an ON to an OFF condition. Register 0x12D can therefore be left at its default value, 0x00.

RSSI

The AD9361 measures RSSI by measuring the power level in dB and compensating for the receive path gain. The various options available support both TDD and FDD applications. Note that the RSSI value is not in absolute units. Equating the RSSI read-back value to an absolute power level (e.g., in dBm) requires a system factory or bench calibration. To calibrate the RSSI word to an absolute reference, inject a signal into the antenna port of the completed system and read the RSSI word. From this test, generate a correction factor that equates the RSI word to the injected signal level at the antenna port. This calibration is not to be confused with the Gain Step Calibration mentioned later in this document.

RSSI MODE SELECT

The RSSI Mode Select bits (0x158[D4:D2] determine what event starts or restarts the RSSI algorithm and clears the accumulator, per the following table.

RSSI Mode Select	The RSSI Algorithm will (re)start when:	Useful For
000	AGC in Fast Attack Mode Locks the Gain	TDD
001	EN_AGC pin is pulled High	TDD, measuring a symbol late in the burst
010	AD9361 Enters Rx Mode	TDD
011	Gain Change Occurs	FDD
100	SPI Write to Register 0x158[D5]	FDD
101	Gain Change Occurs OR EN_AGC pin pulled High	FDD

Table 21.RSSI Mode Select

RSSI MEASUREMENT DURATION

If the “Default RSSI Meas Mode” bit (0x158[D0]) bit is set high, then the duration is a simple power-of-two value shown in Equation 9 “Measurement Duration 0” is stored in 0x150[D3:D0]. All other bits in 0x150 and 0x151are ignored.

$$2$$

Equation 9

If 0x158[D0] is low, then non-power-of-two durations are possible perEquation 10. The four duration values are stored in 0x150 and 0x151.

$$\sum \quad 2$$

Equation 10

Duration is always Rx sample-rate cycles.

RSSI WEIGHTING

If the “Default RSSI Meas Mode” bit (0x158[D0])is low, then the RSSI measurement duration consists of up to 4 values summed together. Since each value can be different, each value must be correctly weighted by its duration in Rx samples. Weighting is calculated per Equation 11. Weighted multiplier values are programmed in 0x152 through 0x155. If the “Default RSSI Meas Mode” b AD9361 automatically populates multiplier 0 with 0xFF and the other multipliers with 0x00. When calculated correctly, the total of all four weights added together will be 255 (d).

$$? \quad \text{———————————}$$

Equation 11

RSSI DELAY AND RSSI WAIT

When the RSSI algorithm (re)starts, the AD9361 first waits for the Rx signal path to settle. This delay is the “R 0x156 and clocked at the Rx sample rate divided by 8. From this point on, the RSSI algorithm alternates between measuring RSSI and

waiting to measure RSSI. The purpose of the RSSI Wait value is to align the RSSI measurement start with boundaries (such as slot boundaries) and is most useful in FDD applications. The following figure shows the use of RSSI Wait, RSSI Delay, and the measurement duration.

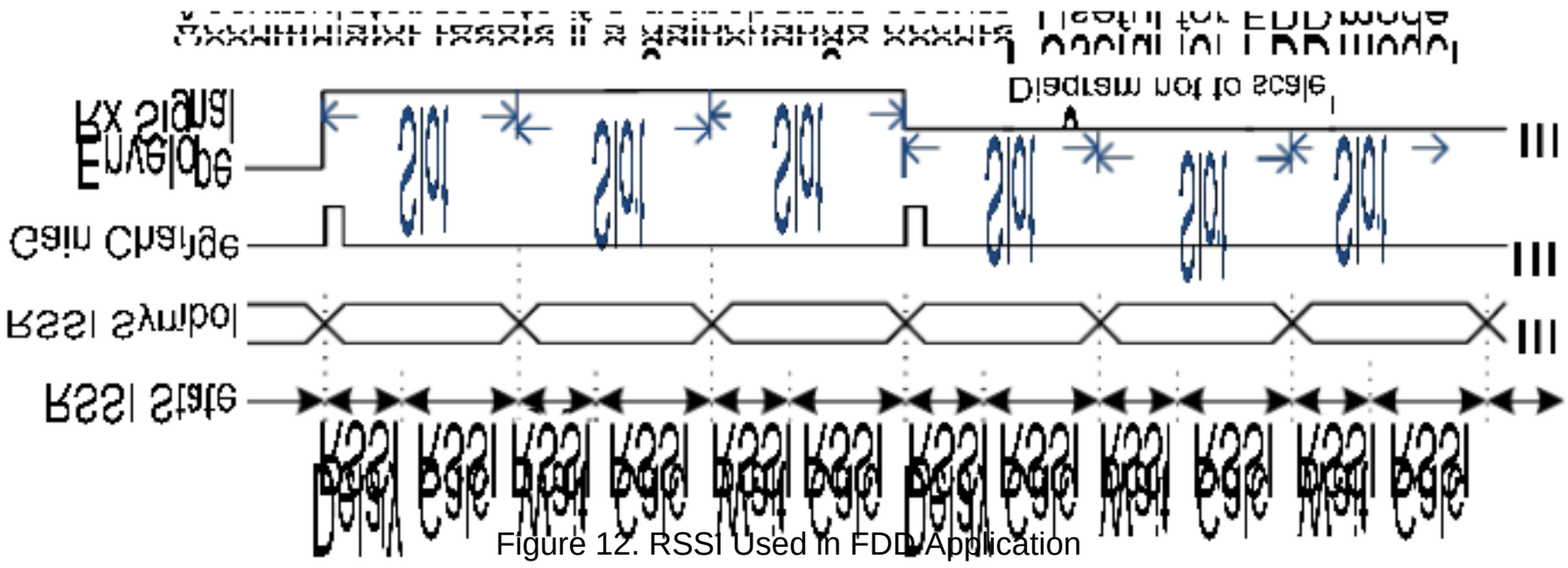

Figure 12. RSSI Used in FDD Application

RSSI PREAMBLE AND RSSI SYMBOL

The first RSSI calculation performed after the RSSI Delay counter expires is stored in both the RSSI Symbol and RSSI registers (0x1A7 through 0x1AC). The RSSI Preamble value remains fixed and does not continue to update unless the algorithm restarts. The RSSI symbol value updates at the end of each calculation as shown in the figure above. An exception to the statements above is that the RSSI preamble words do not update after a gain change (RSSI Mode Select settings 3'b011 and 3'b101).

The Rx1 RSSI Symbol value is stored in register 0x1A7 in 0.5dB/LSB resolution. An additional LSB is also available in bit D0 of 0x1AB. If this bit is also used, the resulting 9-bit word has a resolution of 0.25dB/LSB. In either case, the range is 0 to -128dB (note the negative sign). As the input signal power at the receiver increases, the RSSI value becomes less negative. Rx2 RSSI Symbol is stored in 0x1A9 and bit D1 of 0x1AB.

Rx1 RSSI Preamble can also be treated as an 8-bit or 9-bit word and is stored in register 0x1A8 and bit D0 of 0x1AC. Rx2 RSSI Preamble is stored in 0x1AA and bit D1 and 0x1AC. The range and format is the same as for RSSI Symbol

RSSI RFIR

If the Rx signal path RFIR is used, RSSI uses the data from this FIR for its calculation. If the Rx signal path RFIR is bypassed, then it is still possible to use the RFIR for the RSSI data. Bits D7:D6 of 0x158 set the RSSI RFIR operation per the following table.

0x158[D7:D6]	RSSI RFIR Decimation Factor & Filter Function
00	Decimate by 1 and Bypass Filter
01	Decimate by 1 and Enable Filter
10	Decimate by 2 and Enable Filter
11	Decimate by 4 and Enable Filter

Table 22.RSSI RFIR

RSSI GAIN STEP CALIBRATION

After the AD9361 digitizes and filters the signal, the RSSI algorithm subtracts the gain of the receive path. The resulting value is in dB and referenced to the input of the AD9361. If the actual gain of the AD9361 is different from the gain used by the RSSI algorithm, then as the receive path gain changes, the RSSI word may differ from an expected value. RSSI error typically is within 2dB of the expected value, which is satisfactory for most applications.

For greater RSSI accuracy, the AD9361 uses a Gain Step Calibration algorithm. Running this calibration does not change the actual gain of the receive path but instead only affects RSSI. LNA gain varies over frequency and the difference in gain from one step to another varies as well. The AD9361 stores gain steps as "maximum LNA gain" stored in register 0x15D and as differences from this m

LNA gain stored in an indirectly addressed internal table accessed by register 0x140-0x144. “ Maximum LNA Gain ” oc
gain index = 3.

In combination with an external single tone provided at the system input, the algorithm measures the actual gain steps to 0.25dB precision and creates error terms that are added to the calculated RSSI value. Error terms are calculated for each LNA and Mixer gain step. Each system runs this calibration as part of its factory test routine so that RSSI is optimized for each unit. The test fixture reads the resulting error terms out of the AD9361 and stores them in non-volatile BBP memory. In the field during initialization, the BBP writes the error terms back into the AD9361.

The first step, performed only once, is to determine the optimum single tone amplitude. Provide a single tone within the channel bandwidth and monitor the received data. Adjust the tone amplitude until the received data is within a few dB of full scale but not overloading. This will be the single tone amplitude used during factory test.

Factory Calibration

1. Initialize the AD9361, making sure that the BB DC and RF DC calibrations run as part of this routine. In addition, make sure that BB DC tracking is turned on as the last step of the initialization script.
2. Put the AD9361 into the Alert state
3. Table 23 shows the register values to use depending on the LO frequency used. The next steps that program the step values will use the values from this table.

LO Frequency Range	Step Description	Step Value	Register Value (hex)	Variable in Table 24, Table 25 and Table 27
600MHz to 1300MHz	Maximum LNA Gain	24dB	C0	Xx
	LNA Gain difference word for Index 0	23dB	2E	Aa
	LNA Gain difference word for Index 1	8dB	10	Bb
	LNA Gain difference word for Index 2	3dB	6	Cc
	LNA Gain difference word for index 3	0dB	0	Dd
1300MHz to 3300MHz	Maximum LNA Gain	24dB	C0	Xx
	LNA Gain difference word for Index 0	22dB	2C	Aa
	LNA Gain difference word for Index 1	8dB	10	Bb
	LNA Gain difference word for Index 2	3dB	6	Cc
	LNA Gain difference word for index 3	0dB	0	Dd
2700MHz to 4100MHz	Maximum LNA Gain	23dB	B8	Xx
	LNA Gain difference word for Index 0	22dB	2C	Aa
	LNA Gain difference word for Index 1	8dB	10	Bb
	LNA Gain difference word for Index 2	3dB	6	Cc
	LNA Gain difference word for index 3	0dB	0	Dd
4000MHz to 6000MHz	Maximum LNA Gain	20dB	A0	Xx
	LNA Gain difference word for Index 0	18dB	24	Aa
	LNA Gain difference word for Index 1	8dB	10	Bb
	LNA Gain difference word for Index 2	3dB	6	Cc
	LNA Gain difference word for index 3	0dB	0	Dd

Table 23. Gain Step Calibration Register Values vs. LO Frequency

4. Program the directly-addressable register values as shown in Table 24

Line Number	Command	Addr/Data	Comment
1	SPIWrite	145,0F	//Set maximum mixer gain index (always 0x0F)
2	SPIWrite	148,0E	//Maximum measurement time
3	SPIWrite	147,3F	//Maximum settling time
4	SPIWrite	158,0D	//Default RSSI measurement mode
5	SPIWrite	150,0E	//Maximum RSSI measurement time
6	SPIWrite	15D,xx	//Maximum LNA Gain (from Table 23)

Table 24. Configure LNA Gain Step Parameters

5. Program the LNA gain step words into the internal table.

Command Addr/Data		Comment
SPIWrite	143,61	//Write R1 and R2 internal LNA tables & start clock
SPIWrite 140,00		//LNA index
SPIWrite	141,aa	//LNA gain step from Table 23
SPIWrite 143,63		//Write data
WAIT	3us	//Wait for data to fully write to internal table
SPIWrite 140,01		//LNA index
SPIWrite	141,bb	//LNA gain step from Table 23
SPIWrite 143,63		//Write data
WAIT	3us	//Wait for data to fully write to internal table
SPIWrite 140,02		//LNA index
SPIWrite	141,cc	//LNA gain step from Table 23
SPIWrite 143,63		//Write data
WAIT	3us	//Wait for data to fully write to internal table
SPIWrite 140,03		//LNA index
SPIWrite	141,dd	//LNA gain step from Table 23
SPIWrite 143,63		//Write data
WAIT	3us	//Wait for data to fully write to internal table
SPIWrite	143,01	//Clear write bit
SPIWrite 143,00		//Stop clock

Table 25. Programming the LNA Gain Steps into the internal table

6. Turn on the external single tone at the amplitude determined previously and inject it into Rx1
7. Run the calibration by setting 0x016[D3]
8. The calibration completes when 0x016[D3] clears
9. Read the LNA and Mixer error terms as shown in Table 26 into non-volatile memory

Line Number	Command	Addr/Data	Comment
1	SPIWrite	143,30	//Setup to read LNA error words from Rx1
2	SPIWrite	140,00	//Set LNA index address to 0
3	SPIRead	142	//Read LNA error for index 0. Store in non-volatile table
4	Repeat steps 2 & 3 for 3 remaining LNA indices		
5	SPIWrite	143,20	//Setup to read Mixer Error Words from Rx1
6	SPIWrite	140,00	//Set Mixer Index address to 0
7	SPIRead	142	//Read Mixer error for index 0. Store in non-volatile table
8	Repeat steps 6 & 7 for 14 remaining Mixer indices		
9	SPIWrite	143,00	//Put calibration register back to default

Table 26. Reading gain step error words from the AD9361

Programming Gain Step Errors in the Field

During initialization (while the transceiver is in the Alert or Wait states), program the two configuration registers as shown in the table below (again, “xx” is the value from Table 23).

Line Number	Command	Addr/Data	Comment
1	SPIWrite	145,0F	//Set maximum mixer gain index (always 0x0F)
2	SPIWrite	15D,xx	//Maximum LNA Gain (from Table 23)

Table 27. Config Registers

Program the indirectly-addressable LNA gain difference words exactly as done in step 5 above. Finally, program the error words back into the AD9361 as described in Table 28.

Line Number	Command	Addr/Data	Comment
1	SPIWrite	143,61	//Setup to write both Rx1 and Rx2 and start clock
2	SPIWrite	140,00	//Set LNA index address to 0
3	SPIWrite	141,ff	//Write LNA index 0 error word from non-volatile memory
4	SPIWrite	143,65	//Write data into address 0
5	Repeat steps 2-4 for 3 remaining LNA indices		
6	SPIWrite	143,61	//Setup to write both Rx1 and Rx2 and start clock
7	SPIWrite	140,00	//Set Mixer Index address to 0
8	SPIWrite	141,gg	//Write Mixer index 0 error word from non-volatile memory
9	SPIWrite	143,69	//Write data into address 0
10	Repeat steps 7-9 for 14 remaining Mixer indices		
11 SPIWrite		143,00	//Stop clock

Table 28. Programming gain step errors into the AD9361 in the field

In the processes and scripts shown above, Rx1 is calibrated and then the error word results are programmed into Rx1 and Rx2. The resulting RSSI errors are expected to be within approximately 0.5dB for Rx2 when using Rx1 error words. For maximum accuracy, each receiver should be calibrated independently with error words saved to non-volatile memory for each receiver. When programming in the field, the words would be programmed into the internal tables for each receiver separately.

APPENDIX 1 — REGISTER SETTINGS FOR EXAMPLE APPLICATIONS

APPLICATION EXAMPLE #1 – FULL TABLE, SLOW AGC, RSSI

As an example, assume that the application is for an LTE (Long Term Evolution) FDD (Frequency Division Duplexing) UE (User Equipment) product targeted at LTE frequency band 7 using a 2x2 multiple in multiple out scheme. These register settings will assume that the AD9361 is initialized for LTE 10MHz operation. The AGC will be used and the AD9361 RSSI function will be used.

Important information:

Let the initial settings be for the 10MHz RF BW option for LTE. The example will also show what needs to change to address BW (and sample rate) changes

The AD9361 will use a full gain table. Since the system supports band 38, the 1300MHz to 4000MHz table will be used.

The power level of a received FDD waveform usually changes very slowly. Thus, the slow AGC is a good fit.

The protocol is LTE and the product is UE so the received signal will be a downlink (DL). Thus, the Peak-to-Average Ratio (PAR) probability is approximately 300 for 11dB. This information indicates that one for every 300 samples will have a peak amplitude that is 11dB higher than the average power level. The PAR probability is approximately 10^{-4} for 12dB. The slow AGC is a 2^{nd} order window comparator with hysteresis. A good starting point for the window would be an inner upper limit of -10dBFS and an inner lower limit of -12dBFS. This will result in a small amount of rare compression which helps keep EVM low and SNR as high as possible.

There are several options allowing the BBP to force when the gain changes. For this example, assume that the gain update counter will be used, the gain will update at 500us intervals (on slot boundaries), and that the gain update counter can be reset when the BBP transitions the Control Input 2 signal high.

LTE has blocker testing requirements and a real-world system will have to handle blockers as well. Depending on the input signal level and the blocker signal level, a blockers can overload LNA, Mixer, and TIA stages without overloading the ADC. Thus, the LMT overload needs to be set such that it will reduce the gain in the presence of blockers but the ADC peak detector and the window comparator will handle desired signal overloads. Thresholds for the LMT and ADC overload detectors have been determined through testing of real-world signals.

Register Configuration example. Address to the left, data to the right, separated by a comma, all in hex, and then a comment to the right. To help clarify why the BBP needs to program some registers but not others, this section lists all gain control registers. Some are commented out which indicates that they are not used and the comment explains why. The register map contains more details for each register.

0FA,EA //Bits D7-D5 are not used for the slow AGC so are unchanged from the chip default. Bit D4 is only set for Hybrid mode so is left clear. The lower nibble selects slow AGC mode for Rx1 and Rx2.

0FB,08 //Bit D7 is the soft reset which should be left low. Bit D6 is not used for the slow AGC. Bits D5 & D4 are open. Bit D3 selects the full gain table so is set. Bit D2 enables digital gain which is not used in the suggested ADI gain tables so this bit is clear. Bits D1 and D0 are not used in the slow AGC mode.

0FC,07 //Bits D7-D3 are not used for the slow AGC. Bits D2-D0 set the number of ADC samples used by the ADC overload detector. The actual number of samples is this value + 1 so 8 samples will be used, which is the suggested value for the slow AGC.

//0FD Bit D7 is open. Bits D6-D0 set the maximum gain index. For the ADI suggested gain table, the maximum gain index is equal to the chip default so it is not necessary to write this register

0FE,48 //Bits D7-D5 are not used by the slow AGC. After a gain changes, the peak overload detectors are held in the reset state while the analog and ADC signal path settles. Bits D4-D0 specify the wait time.

//0FF Open

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//100 Not used with a full gain table and also only used if digital gain is enabled

101,0A //Bit D7 is only used if digital gain is enabled. Bits D6-D0 set the inner high threshold for the slow AGC window comparator in -dBFS

//102 Not used when the HB1 or FIR output is used to calculate power (see 0x15C).

103,08 //Bits D7-D5 set the settling time of the LMT detector. The chip default of 0 (fastest settling time) is recommended for all gain control modes so these bits do not need to be changed. Bits D4-D2 set how far the index moves (“ step size large LMT overload. Bits D1-D0 are part of the noise factor setting in 0x102 so are not used

//104 The ADC small overload threshold is not used in this example (0x120[D7] must be set for the small ADC overload to prevent gain increases). This feature is not required.

105,80 //ADC large overload threshold. All 8 samples must be ±4 (fully saturated)

106,22 //Bit D7 is open. Bits D6-D4 are not used for slow AGC. Bits D3-D0 set the step size when there is a large ADC overload

//107 Bits D7-D6 are test bits. Bits D5-D0 set the small LMT overload threshold but it is not used in this example (0x120[D7] must be set). The “ prevent gain increases ” feature is not required.

108,37 //Bits D7-D6 are open. Bits D5-D0 set the large LMT overload threshold to 896mV

//109 through 10E are not used for the slow AGC

//110 not used for slow AGC

111,0A //Bits D7-D5 are not used for the slow AGC. Bits D4-D0 set the Settling Delay long enough for the Rx path through the filters to settle

//112through 119 are not used for the slow AGC

//11A is not used for full table operation

//11B is not used for the slow AGC

120,0C //These bits set the inner low threshold for the slow AGC window comparator in − dBFS. 0x101 and 0x120 toget the inner window which in this example will hold the power of the digitized signal between -12dbFS and -10dBFS.

121,AA //The top nibble sets the number of times a large LMT overload must occur before the gain would be changed (and then only when the gain update counter expires). The lower nibble similarly applies to the small LMT overload which is not used

122,AA //The top nibble sets the number of times a large ADC overload must occur before the gain would be changed (and then only when the gain update counter expires). The lower nibble similarly applies to the small ADC overload which is not used

123,11 //Bits D7 and D4 allow large LMT or large ADC overloads respectively to affect the gain immediately (do not wait for the gain update counter to expire). Bits D6-D4 set the step size when the signal power exceeds the inner high threshold. Bits D2-D0 set the step size when the signal power drops below the inner low threshold.

124,F5 //These are the lower 8 bits of the gain update counter. See 0x125 for the full explanation.

125,1D //These are the upper 8 bits of the gain update counter. The total value of the counter is 2x the value in 0x124 and 0x125 so it is 0x1DF5. ClkRF (the input to the Rx FIR) clocks the counter.
The Rx data sample rate is 15.36MSPS and since the FIR decimates by 2, the ClkRF rate is 30.72MHz. For a counter time of 500us, the counter should be set to 30.72*10^6 / 2 = 15336. Due to a 2 cycle delay, the counter is actually set to 15338. The register value is ? of 15338 which is 7669(d) = 0x1DF5.

//126 & 127 are open

128,03 //Bits D7-D6 are open. Bit D5 set changes the gain update counter to be 4x the value in 0x124 & 0x125. This is not needed so this bit is clear. Bit D4 allows the gain update counter to be reset when the Control Input 2 signal transitions high which is required for this example.

129,56 //These nibbles set the slow AGC window comparator outer thresholds. The values in these registers are actually the differences between the inner thresholds and the outer thresholds. The inner thresholds are absolute (-dBFS) and the outer thresholds are relative to the inner thresholds.

12A,22 //These nibbles set the step sizes when the signal power exceeds the outer thresholds

150,0A //Since 0x158[D0] is set, the default RSSI measurement duration configuration is selected. Thus, 0x151 is not used and 0x150[D7-D4] is not used. The lower nibble sets the RSSI measurement duration to be 1024 Rx sample periods which is long enough for good accuracy and also allows the RSSI delay to add up to 7680 samples (see 0x156).

//151 through 155 are not used since 0x158[D0] is set

156,40 //This register sets the RSSI delay. After the gain changes, the algorithm waits (this register value * 8) in Rx sample periods before beginning to calculate the RSSI words. Waiting allows the receive path to settle and it also allows the RSSI time to be synchronized to slot boundaries so that the RSSI algorithm only calculates when valid data arrives (not across slot boundaries). Since a slot in this example is 500us, at 15.36MSPS, this is 7680 Rx sample periods. If the RSSI measurement duration is 1024 sample periods, then 7 calculation periods results in 7168 samples. If RSSI delay is 512 samples, the total will be 7680 samples.

//157 The RSSI wait period is not needed. It can also be used to make sure that the RSSI algorithm only measures when data arrives (not across slot boundaries).

158,0D //Bits D7-D6 are ignored since the FIR filter is used for data processing. Bit 5 is only used to manually start an RSSI measurement (not used in this example). Bits D4-D2 set the RSSI mode. For FDD, resetting the algorithm when the gain changes is preferred. Bit D1 is ignored if signal power is measured at the HB1 or FIR filter outputs. These outputs are very noisy and not recommended. Thus, this bit is ignored. Bit D0 enables the RSSI measurement method in which the duration is a simple power of 2 relationship with 0x150[D3:D0].

//159 – 15B are not used when signal power is measured at the output of the HB1 or the FIR filter.

15C,69 //Bit D7 is ignored if the signal power is measured at the output of the HB1 or FIR filter. If signal power is measured at the output of HB1 or the FIR filter, this bit selects which output to use. In this example, setting this bit selects HB1. Bit D5 set enables using HB1 and the FIR output for slow AGC power measurements (e.g. for comparing to the window comparator thresholds). Bit D4 is ignored when signal power is measured at HB1 or the FIR. Bits D3-D0 set the slow AGC power measurement duration.

GAIN CONTROL APPLICATION EXAMPLE #2 SPLIT TABLE, SLOW AGC

The next example is identical to the first with the exception that the system is a residential femtocell (BTS). Only changes from the scripting above are shown below.

Important Information

The decision to use a split table depends on the interferer scenarios likely to be encountered by the system. In this case, assume that the femtocell can be located in an apartment. Just on the other side of the wall from the BTS is a BTS and/or UE that interferers with our system, thus creating a very difficult blocking scenario. A split table allows the AD9361 to adjust the gain in a manner that handles these blockers better than if a full table is used.

0FB,00 //Bit D7 is the soft reset which should be left low. Bit D6 is not used for the slow AGC. Bits D5 & D4 are open. Bit D3 selects the split gain table when it is clear. Bit D2 enables digital gain which is not used in the suggested ADI gain tables so this bit is clear. Bits D1 and D0 are not used in the slow AGC mode.

0FD,28 //Bit D7 is open. Bits D6-D0 set the maximum gain index. For the ADI suggested split gain table, the maximum gain index equals 0x28

11A,0C // sets the index at which the LMT table splits. This index point affects where the gain will be changed for various overload conditions.

GAIN CONTROL APPLICATION EXAMPLE #3 FULL TABLE, FAST AGC

This example uses the same product as example #1 but changes its frequency coverage to band 38, a TD-LTE band.

Important information:

Since UL and DL data shares the same LO frequency, TDD waveforms burst on and off. This type of waveform requires the fast AGC to respond quickly to these bursts.
In this example, it will be assumed that the AGC needs to attack (change gain quickly) when a burst arrives, which will be perhaps 10us after the AD9361 enters the Rx state. About 10us after the burst ends, the AD9361 will exit the Rx state. Thus, the AD9361 will use the ENSM to control the lock and unlock behavior of the AGC.
In addition to the gain unlocking when the AD9361 exits the receive state, the gain will also unlock if the signal power increases or decreases significantly during the burst.
Using similar arguments regarding the PAR as in example #1, the AGC lock level will be set to -10dBFS, allowing a small amount of compression every few hundred samples.

Just like example #1, all registers are shown below with comments, even if they are not used in this example.

0FA,E5 //Bits D7-D5 set will force the AGC to use the output of HB1 or the FIR when measuring power in various conditions. Measuring power at these points has very low noise so is desirable, thus these bits are set. Bit D4 is only set for Hybrid mode so is left clear. The lower nibble selects Fast AGC mode for Rx1 and Rx2.

0FB,08 //Bit D7 is the soft reset which should be left low. Bit D6 allows for gain unlock control that is not needed for this example. Bits D5 & D4 are open. Bit D3 selects the full gain table so is set. Bit D2 enables digital gain which is not used in the suggested ADI gain tables so this bit is clear. Bits D1 and D0 are not used in the fast AGC mode.

0FC,03 //Bits D7-D3 are not used for the fast AGC. Bits D2-D0 set the number of ADC samples used by the ADC overload detector. The actual number of samples is this value + 1 so 4 samples will be used, which is the suggested value for the fast AGC.

//0FD Bit D7 is open. Bits D6-D0 set the maximum gain index. For the ADI suggested gain table, the maximum gain index is equal to the chip default so it is not necessary to write this register

0FE,44 //Bits D7-D5 are not used for the fast AGC. After a gain changes, the peak overload detectors are held in the reset state while the analog and ADC signal path settles. Bits D4-D0 specify the wait time.

//0FF Open

//100 Not used with a full gain table and also only used if digital gain is enabled

101,0A //Bit D7 is only used if digital gain is enabled. Bits D6-D0 set the AGC lock level to -10dBFS.

//102 Not used when the HB1 or FIR output is used to calculate power (see 0x15C).

103,08 //Bits D7-D5 set the settling time of the LMT detector. The chip default of 0 (fastest settling time) is recommended for all gain control modes so these bits do not need to be changed. Bits D4-D2 set how far the index moves (“ step size overload. Bits D1-D0 are part of the noise factor setting in 0x102 so are not used

104,2F //This register sets the small ADC overload to a value of 47(d) which requires at least 2 of the 4 ADC samples to be at max level and the other two samples to be at ±3.

105,3A //ADC large overload threshold set to 58(d) which requires all 4 ADC samples to be at max level.

106,22 //Bit D7 is open. Bits D6-D4 specify the step size when a large ADC overload occurs or a large LMT overload occurs. Bits D3-D0 set the step size when a large ADC overload and a large LMT overload occur.

10708 //Bits D7-D6 are test bits. Bits D5-D0 set the small LMT overload threshold which will not be used in this example. When it is used with the fast AGC, it only prevents gain increases; it does not decrease gain.

108,1F //Bits D7-D6 are open. Bits D5-D0 set the large LMT overload threshold

//109 through 10E are not used for the fast AGC

110,00 //Bits D7-D1 control how the gain unlocks and what the gain index changes to after unlock. In this example, the index will always go to its maximum value when the gain unlocks and it will only unlock if the signal power decreases or increases by 10dB after lock (see 0x112, 0x113), a large peak overload occurs, and when the AD9361 exits the receive state. Bit D0 enables gain increases which are typically not necessary (including in this example).

111,0A //Bits D7 & D5 are not used when the gain index goes to maximum after unlocking. Bit D6 is not used with a full gain table. Bits D4-D0 set the Settling Delay long enough for the Rx path through the filters to settle

112,4A //Bits D7-D6 set the step size if a large ADC or LMT overload occurs after the gain locks. This is set to 2 only small adjustments should be required after lock. As mentioned in the description of register 0x110, if the signal power decreases 10dB after the gain locks, the AGC will unlock. The 10dB threshold is set in bits D5-D0.

113,4A //Bits D7-D6 are not used with a full gain table. Bits D5-D0 set a similar threshold to 0x112[D5:D0] but in this case it is for a threshold that responds to signal power exceeding the lock level.

//114 Bit D7 prevents gain from unlocking for ADC overloads. In this example, the gain should unlock in this case so this bit is clear. Bits D6-D0 set the low power threshold which is used only if the gain is allowed to increase. In nearly all scenarios (including this example), the gain does not need to increase so these bits are unused.

//115 Bit D7 prevents gain from unlocking if the signal power increases during a burst. In this example, the gain should unlock so this bit is clear. All other bits are open.

116,65 //After gain lock, if a programmable number of large peak overloads occur, the AGC will start over. In this case, presumably a significant change in signal power has occurred which negates the current lock index. Bits D7-D5 set the number of overloads. Bit D4 is open. Bits D3-D0 are not used when the gain index will go maximum after unlocking.

117,08 //Bits D7-D5 are not used since the gain index is not allowed to increase. As described in 0x112 and 0x113, changes in signal power after gain lock can cause the gain to unlock. The power must exceed a threshold for a programmable number of rx sample periods before unlock occurs. The number of periods is set in bits D4-D0.

118,05 //Bits D7-D6 are open. When the fast AGC changes the gain index in order to make the signal power equal to the AGC lock level in 0x10, the setting of bits D4-D0 limit the number of gain index steps the gain can increase. Large amounts of gain increase can cause the AGC to have trouble locking in the presence of interfering signals.

119,08 //Bits D7-D6 are open. After gain lock but while the AGC is still in state 3, the AGC checks the peak detectors for overloads as described above in 0x112 & 0x113. If the gain decreases more than a programmable number of times, the AGC starts over. Bits D5-D0 determine how many times the gain can decrease before the AGC will force a restart.

//11A is not used for full table operation

//11B is not used because the gain is not allowed to increase

//120-12A are not used with the fast AGC

150,08 //Since 0x158[D0] is set, the default RSSI measurement duration configuration is selected. Thus, 0x151 is not used and 0x150[D7-D4] is not used. The lower nibble sets the RSSI measurement duration.

//151 through 155 are not used since 0x158[D0] is set

//156-157 are not needed in this example.

158,01 //Bits D7-D6 are ignored since the FIR filter is used for data processing. Bit 5 is only used to manually start an RSSI measurement (not used in this example). Bits D4-D2 set the RSSI mode. For TDD, resetting the algorithm when the gain locks is preferred. Bit D1 is ignored if signal power is measured at the HB1 or FIR filter outputs. These outputs are very noisy and not recommended. Thus, this bit is ignored. Bit D0 enables the RSSI measurement method in which the duration is a simple power of 2 relationship with 0x150[D3:D0].

//159 – 15B are not used when signal power is measured at the output of the HB1 or the FIR filter.

15C,62 //Bit D7 is ignored if the signal power is measured at the output of the HB1 or FIR filter. If signal power is measured at the output of HB1 or the FIR filter, this bit selects which output to use. In this example, setting this bit selects HB1. Bit D5 set enables using HB1 and the FIR output for slow AGC power measurements (e.g. for comparing to the window comparator thresholds). Bit D4 is ignored when signal power is measured at HB1 or the FIR. Bits D3-D0 set the slow AGC power measurement duration.

APPENDIX 2 — OPTIMIZED GAIN TABLES

FULL GAIN TABLES

The full gain tables provided by ADI have 77 (d) total entries with the index value ranging from 0 to 76(d). Each change of the index by 1 results in a gain change of 1dB. Since the AD9361 internal LNA gain and the mixer gain change with LO frequency, three different gain

tables are required to span the entire LO frequency range of the AD9361. As mentioned in the Writing to and Reading From the Gain Table section, the BBP only programs the values in columns "Table Index", "0x131", "0x132", "0x133" into the AD9361. The other columns allow the individual gain indices for each stage to be easily analyzed. The captions below each table show the effective range of each table. The effective ranges are not hard limits. As a table is used outside of its stated range, the gain steps will start to deviate from 1dB for each unit increment or decrement of the index. For manual gain operation, this the amount of allowable deviation is customer-dependent. For AGC modes, the AGC can oscillate among indices if the gain step is significantly different than 1dB. To use a gain table outside of its stated range with the AGC, please contact applications engineering. A typical system may only need one gain table to cover the entire range of its operation. None of these tables are loaded into the AD9361 by default so the BBP must load the proper table into the AD9361 in the field as part of initialization.

They are in .csv format so they do not have color-coded columns (unlike the previous examples in the Writing to and Reading From the Gain Table section.

Table Index	eLNA Index	eLNA Gain	iLNA Index	iLNA Gain	Mixer Index	Mixer Gain	0x131	TIA Index	TIA Gain	LPF Index	0x132	DC Cal	Digital Index	0x133	Total Gain
0	0	0	0	5	0	0	0	0	6	0	0	1	0	20	1
1	0	0	0	5	0	0	0	0	6	0	0	0	0	0	1
2	0	0	0	5	0	0	0	0	6	0	0	0	0	0	1
3	0	0	0	5	0	0	0	0	6	1	1	0	0	0	0
4	0	0	0	5	0	0	0	0	6	2	2	0	0	0	1
5	0	0	0	5	0	0	0	0	6	3	3	0	0	0	2
6	0	0	0	5	0	0	0	0	6	4	4	0	0	0	3
7	0	0	0	5	0	0	0	0	6	5	5	0	0	0	4
8	0	0	0	5	1	3	1	0	6	3	3	1	0	20	5
9	0	0	0	5	1	3	1	0	6	4	4	0	0	0	6
10	0	0	0	5	1	3	1	0	6	5	5	0	0	0	7
11	0	0	0	5	1	3	1	0	6	6	6	0	0	0	8
12	0	0	0	5	1	3	1	0	6	7	7	0	0	0	9
13	0	0	0	5	1	3	1	0	6	8	8	0	0	0	10
14	0	0	0	5	1	3	1	0	6	9	9	0	0	0	11
15	0	0	0	5	1	3	1	0	6	10	A	0	0	0	12
16	0	0	0	5	1	3	1	0	6	11	B	0	0	0	13
17	0	0	0	5	1	3	1	0	6	12	C	0	0	0	14
18	0	0	0	5	1	3	1	0	6	13	D	0	0	0	15
19	0	0	0	5	1	3	1	0	6	14	E	0	0	0	16
20	0	0	0	5	2	9	2	0	6	9	9	1	0	20	17
21	0	0	0	5	2	9	2	0	6	10	A	0	0	0	18
22	0	0	0	5	2	9	2	0	6	11	B	0	0	0	19
23	0	0	0	5	2	9	2	0	6	12	C	0	0	0	20
24	0	0	0	5	2	9	2	0	6	13	D	0	0	0	21
25	0	0	0	5	2	9	2	0	6	14	E	0	0	0	22
26	0	0	0	5	2	9	2	0	6	15	F	0	0	0	23
27	0	0	0	5	2	9	2	0	6	16	10	0	0	0	24
28	0	0	0	5	2	9	2	1	0	11	2B	1	0	20	25
29	0	0	0	5	2	9	2	1	0	12	2C	0	0	0	26

30	0	0	0	5	4	14	4	1	0	8	28	1	0	20	27
31	0	0	0	5	4	14	4	1	0	9	29	0	0	0	28
32	0	0	0	5	4	14	4	1	0	10	2A	0	0	0	29
33	0	0	0	5	4	14	4	1	0	11	2B	0	0	0	30
34	0	0	1	17	4	14	24	1	0	0	20	1	0	20	31
35	0	0	1	17	4	14	24	1	0	1	21	0	0	0	32
36	0	0	2	19	4	14	44	1	0	0	20	1	0	20	33
37	0	0	2	19	4	14	44	1	0	1	21	0	0	0	34
38	0	0	2	19	4	14	44	1	0	2	22	0	0	0	35
39	0	0	2	19	4	14	44	1	0	3	23	0	0	0	36
40	0	0	2	19	4	14	44	1	0	4	24	0	0	0	37
41	0	0	2	19	4	14	44	1	0	5	25	0	0	0	38
42	0	0	2	19	4	14	44	1	0	6	26	0	0	0	39
43	0	0	2	19	4	14	44	1	0	7	27	0	0	0	40
44	0	0	2	19	4	14	44	1	0	8	28	0	0	0	41
45	0	0	2	19	4	14	44	1	0	9	29	0	0	0	42
46	0	0	2	19	4	14	44	1	0	10	2A	0	0	0	43
47	0	0	2	19	4	14	44	1	0	11	2B	0	0	0	44
48	0	0	2	19	4	14	44	1	0	12	2C	0	0	0	45
49	0	0	2	19	4	14	44	1	0	13	2D	0	0	0	46
50	0	0	2	19	4	14	44	1	0	14	2E	0	0	0	47
51	0	0	2	19	4	14	44	1	0	15	2F	0	0	0	48
52	0	0	2	19	4	14	44	1	0	16	30	0	0	0	49
53	0	0	2	19	4	14	44	1	0	17	31	0	0	0	50
54	0	0	2	19	4	14	44	1	0	18	32	0	0	0	51
55	0	0	3	24	4	14	64	1	0	14	2E	1	0	20	52
56	0	0	3	24	4	14	64	1	0	15	2F	0	0	0	53
57	0	0	3	24	4	14	64	1	0	16	30	0	0	0	54
58	0	0	3	24	4	14	64	1	0	17	31	0	0	0	55
59	0	0	3	24	4	14	64	1	0	18	32	0	0	0	56
60	0	0	3	24	4	14	64	1	0	19	33	0	0	0	57
61	0	0	3	24	4	14	64	1	0	20	34	0	0	0	58
62	0	0	3	24	4	14	64	1	0	21	35	0	0	0	59
63	0	0	3	24	4	14	64	1	0	22	36	0	0	0	60
64	0	0	3	24	4	14	64	1	0	23	37	0	0	0	61
65	0	0	3	24	4	14	64	1	0	24	38	0	0	0	62
66	0	0	3	24	5	15	65	1	0	24	38	1	0	20	63
67	0	0	3	24	6	16	66	1	0	24	38	1	0	20	64
68	0	0	3	24	7	17	67	1	0	24	38	1	0	20	65
69	0	0	3	24	8	18	68	1	0	24	38	1	0	20	66
70	0	0	3	24	9	19	69	1	0	24	38	1	0	20	67
71	0	0	3	24	10	20	6A	1	0	24	38	1	0	20	68
72	0	0	3	24	11	21	6B	1	0	24	38	1	0	20	69

73	0	0	3	24	12	22	6C	1	0	24	38	1	0	20	70
74	0	0	3	24	13	23	6D	1	0	24	38	1	0	20	71
75	0	0	3	24	14	24	6E	1	0	24	38	1	0	20	72
76	0	0	3	24	15	25	6F	1	0	24	38	1	0	20	73

Table 29.Optimized Full Gain Table for 200MHz through 1300MHz Operation

Table Index	eLNA Index	eLNA Gain	iLNA Index	iLNA Gain	Mixer Index	Mixer Gain	0x131	TIA Index	TIA Gain	LPF Index	0x132	DC Cal	Digital Index	0x133	Total Gain
0	0	0	0	3	0	0	0	0	6	0	0	1	0	20	3
1	0	0	0	3	0	0	0	0	6	0	0	0	0	0	3
2	0	0	0	3	0	0	0	0	6	0	0	0	0	0	3
3	0	0	0	3	0	0	0	0	6	1	1	0	0	0	2
4	0	0	0	3	0	0	0	0	6	2	2	0	0	0	1
5	0	0	0	3	0	0	0	0	6	3	3	0	0	0	0
6	0	0	0	3	0	0	0	0	6	4	4	0	0	0	1
7	0	0	0	3	0	0	0	0	6	5	5	0	0	0	2
8	0	0	0	3	1	3	1	0	6	3	3	1	0	20	3
9	0	0	0	3	1	3	1	0	6	4	4	0	0	0	4
10	0	0	0	3	1	3	1	0	6	5	5	0	0	0	5
11	0	0	0	3	1	3	1	0	6	6	6	0	0	0	6
12	0	0	0	3	1	3	1	0	6	7	7	0	0	0	7
13	0	0	0	3	1	3	1	0	6	8	8	0	0	0	8
14	0	0	0	3	1	3	1	0	6	9	9	0	0	0	9
15	0	0	0	3	1	3	1	0	6	10	A	0	0	0	10
16	0	0	0	3	1	3	1	0	6	11	B	0	0	0	11
17	0	0	0	3	1	3	1	0	6	12	C	0	0	0	12
18	0	0	0	3	1	3	1	0	6	13	D	0	0	0	13
19	0	0	0	3	1	3	1	0	6	14	E	0	0	0	14
20	0	0	0	3	2	9	2	0	6	9	9	1	0	20	15
21	0	0	0	3	2	9	2	0	6	10	A	0	0	0	16
22	0	0	0	3	2	9	2	0	6	11	B	0	0	0	17
23	0	0	0	3	2	9	2	0	6	12	C	0	0	0	18
24	0	0	0	3	2	9	2	0	6	13	D	0	0	0	19
25	0	0	0	3	2	9	2	0	6	14	E	0	0	0	20
26	0	0	0	3	2	9	2	0	6	15	F	0	0	0	21
27	0	0	0	3	2	9	2	0	6	16	10	0	0	0	22
28	0	0	0	3	2	9	2	1	0	11	2B	1	0	20	23
29	0	0	0	3	2	9	2	1	0	12	2C	0	0	0	24
30	0	0	0	3	4	15	4	1	0	7	27	1	0	20	25
31	0	0	0	3	4	15	4	1	0	8	28	0	0	0	26
32	0	0	0	3	4	15	4	1	0	9	29	0	0	0	27
33	0	0	0	3	4	15	4	1	0	10	2A	0	0	0	28

34	0	0	0	3	4	15	4	1	0	11	2B	0	0	0	29
35	0	0	1	14	4	15	24	1	0	1	21	1	0	20	30
36	0	0	1	14	4	15	24	1	0	2	22	0	0	0	31
37	0	0	2	17	4	15	44	1	0	0	20	1	0	20	32
38	0	0	2	17	4	15	44	1	0	1	21	0	0	0	33
39	0	0	2	17	4	15	44	1	0	2	22	0	0	0	34
40	0	0	2	17	4	15	44	1	0	3	23	0	0	0	35
41	0	0	2	17	4	15	44	1	0	4	24	0	0	0	36
42	0	0	2	17	4	15	44	1	0	5	25	0	0	0	37
43	0	0	2	17	4	15	44	1	0	6	26	0	0	0	38
44	0	0	2	17	4	15	44	1	0	7	27	0	0	0	39
45	0	0	2	17	4	15	44	1	0	8	28	0	0	0	40
46	0	0	2	17	4	15	44	1	0	9	29	0	0	0	41
47	0	0	2	17	4	15	44	1	0	10	2A	0	0	0	42
48	0	0	2	17	4	15	44	1	0	11	2B	0	0	0	43
49	0	0	2	17	4	15	44	1	0	12	2C	0	0	0	44
50	0	0	2	17	4	15	44	1	0	13	2D	0	0	0	45
51	0	0	2	17	4	15	44	1	0	14	2E	0	0	0	46
52	0	0	2	17	4	15	44	1	0	15	2F	0	0	0	47
53	0	0	2	17	4	15	44	1	0	16	30	0	0	0	48
54	0	0	2	17	4	15	44	1	0	17	31	0	0	0	49
55	0	0	3	21	4	15	64	1	0	14	2E	1	0	20	50
56	0	0	3	21	4	15	64	1	0	15	2F	0	0	0	51
57	0	0	3	21	4	15	64	1	0	16	30	0	0	0	52
58	0	0	3	21	4	15	64	1	0	17	31	0	0	0	53
59	0	0	3	21	4	15	64	1	0	18	32	0	0	0	54
60	0	0	3	21	4	15	64	1	0	19	33	0	0	0	55
61	0	0	3	21	4	15	64	1	0	20	34	0	0	0	56
62	0	0	3	21	4	15	64	1	0	21	35	0	0	0	57
63	0	0	3	21	4	15	64	1	0	22	36	0	0	0	58
64	0	0	3	21	4	15	64	1	0	23	37	0	0	0	59
65	0	0	3	21	4	15	64	1	0	24	38	0	0	0	60
66	0	0	3	21	5	16	65	1	0	24	38	1	0	20	61
67	0	0	3	21	6	17	66	1	0	24	38	1	0	20	62
68	0	0	3	21	7	18	67	1	0	24	38	1	0	20	63
69	0	0	3	21	8	19	68	1	0	24	38	1	0	20	64
70	0	0	3	21	9	20	69	1	0	24	38	1	0	20	65
71	0	0	3	21	10	21	6A	1	0	24	38	1	0	20	66
72	0	0	3	21	11	22	6B	1	0	24	38	1	0	20	67
73	0	0	3	21	12	23	6C	1	0	24	38	1	0	20	68
74	0	0	3	21	13	24	6D	1	0	24	38	1	0	20	69
75	0	0	3	21	14	25	6E	1	0	24	38	1	0	20	70
76	0	0	3	21	15	26	6F	1	0	24	38	1	0	20	71

Table 30. Optimized Full Gain Table for 1300MHz through 4000MHz Operation

Table Index	eLNA Index	eLNA Gain	iLNA Index	iLNA Gain	Mixer Index	Mixer Gain	0x131	TIA Index	TIA Gain	LPF Index	0x132	DC Cal	Digital Index	0x133	Total Gain
0	0	0	0	4	0	0	0	0	6	0	0	1	0	20	10
1	0	0	0	4	0	0	0	0	6	0	0	0	0	0	10
2	0	0	0	4	0	0	0	0	6	0	0	0	0	0	10
3	0	0	0	4	0	0	0	0	6	0	0	0	0	0	10
4	0	0	0	4	0	0	0	0	6	0	0	0	0	0	10
5	0	0	0	4	0	0	0	0	6	1	1	0	0	0	9
6	0	0	0	4	0	0	0	0	6	2	2	0	0	0	8
7	0	0	0	4	0	0	0	0	6	3	3	0	0	0	7
8	0	0	0	4	1	3	1	0	6	1	1	1	0	20	6
9	0	0	0	4	1	3	1	0	6	2	2	0	0	0	5
10	0	0	0	4	1	3	1	0	6	3	3	0	0	0	4
11	0	0	0	4	1	3	1	0	6	4	4	1	0	20	3
12	0	0	0	4	1	3	1	0	6	5	5	0	0	0	2
13	0	0	0	4	1	3	1	0	6	6	6	0	0	0	1
14	0	0	0	4	1	3	1	0	6	7	7	0	0	0	0
15	0	0	0	4	1	3	1	0	6	8	8	0	0	0	1
16	0	0	0	4	1	3	1	0	6	9	9	0	0	0	2
17	0	0	0	4	1	3	1	0	6	10	A	0	0	0	3
18	0	0	0	4	1	3	1	0	6	11	B	0	0	0	4
19	0	0	0	4	1	3	1	0	6	12	C	0	0	0	5
20	0	0	0	4	2	8	2	0	6	8	8	1	0	20	6
21	0	0	0	4	2	8	2	0	6	9	9	0	0	0	7
22	0	0	0	4	2	8	2	0	6	10	A	0	0	0	8
23	0	0	0	4	2	8	2	0	6	11	B	1	0	20	9
24	0	0	0	4	2	8	2	0	6	12	C	0	0	0	10
25	0	0	0	4	2	8	2	0	6	13	D	0	0	0	11
26	0	0	0	4	2	8	2	0	6	14	E	0	0	0	12
27	0	0	0	4	2	8	2	0	6	15	F	0	0	0	13
28	0	0	0	4	2	8	2	1	0	10	2A	1	0	20	14
29	0	0	0	4	2	8	2	1	0	11	2B	0	0	0	15
30	0	0	0	4	4	13	4	1	0	7	27	1	0	20	16
31	0	0	0	4	4	13	4	1	0	8	28	0	0	0	17
32	0	0	0	4	4	13	4	1	0	9	29	0	0	0	18
33	0	0	0	4	4	13	4	1	0	10	2A	0	0	0	19
34	0	0	0	4	4	13	4	1	0	11	2B	0	0	0	20
35	0	0	0	4	4	13	4	1	0	12	2C	0	0	0	21
36	0	0	0	4	4	13	4	1	0	13	2D	0	0	0	22
37	0	0	1	10	4	13	24	1	0	0	20	1	0	20	23

38	0	0	1	10	4	13	24	1	0	1	21	0	0	0	24
39	0	0	1	10	4	13	24	1	0	2	22	0	0	0	25
40	0	0	2	13	4	13	44	1	0	0	20	1	0	20	26
41	0	0	2	13	4	13	44	1	0	1	21	0	0	0	27
42	0	0	2	13	4	13	44	1	0	2	22	0	0	0	28
43	0	0	2	13	4	13	44	1	0	3	23	0	0	0	29
44	0	0	2	13	4	13	44	1	0	4	24	0	0	0	30
45	0	0	2	13	4	13	44	1	0	5	25	0	0	0	31
46	0	0	2	13	4	13	44	1	0	6	26	0	0	0	32
47	0	0	2	13	4	13	44	1	0	7	27	0	0	0	33
48	0	0	2	13	4	13	44	1	0	8	28	0	0	0	34
49	0	0	2	13	4	13	44	1	0	9	29	0	0	0	35
50	0	0	2	13	4	13	44	1	0	10	2A	0	0	0	36
51	0	0	2	13	4	13	44	1	0	11	2B	0	0	0	37
52	0	0	2	13	4	13	44	1	0	12	2C	0	0	0	38
53	0	0	2	13	4	13	44	1	0	13	2D	0	0	0	39
54	0	0	2	13	4	13	44	1	0	14	2E	0	0	0	40
55	0	0	3	14	4	13	64	1	0	14	2E	1	0	20	41
56	0	0	3	14	4	13	64	1	0	15	2F	0	0	0	42
57	0	0	3	14	4	13	64	1	0	16	30	0	0	0	43
58	0	0	3	14	4	13	64	1	0	17	31	0	0	0	44
59	0	0	3	14	4	13	64	1	0	18	32	0	0	0	45
60	0	0	3	14	4	13	64	1	0	19	33	0	0	0	46
61	0	0	3	14	4	13	64	1	0	20	34	0	0	0	47
62	0	0	3	14	4	13	64	1	0	21	35	0	0	0	48
63	0	0	3	14	4	13	64	1	0	22	36	0	0	0	49
64	0	0	3	14	4	13	64	1	0	23	37	0	0	0	50
65	0	0	3	14	4	13	64	1	0	24	38	0	0	0	51
66	0	0	3	14	5	14	65	1	0	24	38	1	0	20	52
67	0	0	3	14	6	15	66	1	0	24	38	1	0	20	53
68	0	0	3	14	7	16	67	1	0	24	38	1	0	20	54
69	0	0	3	14	8	17	68	1	0	24	38	1	0	20	55
70	0	0	3	14	9	18	69	1	0	24	38	1	0	20	56
71	0	0	3	14	10	19	6A	1	0	24	38	1	0	20	57
72	0	0	3	14	11	20	6B	1	0	24	38	1	0	20	58
73	0	0	3	14	12	21	6C	1	0	24	38	1	0	20	59
74	0	0	3	14	13	22	6D	1	0	24	38	1	0	20	60
75	0	0	3	14	14	23	6E	1	0	24	38	1	0	20	61
76	0	0	3	14	15	24	6F	1	0	24	38	1	0	20	62

Table 31. Optimized Full Gain Table for 4000MHz through 6000MHz Operation

SPLIT GAIN TABLE

The split gain table provided by ADI has 41 (d) total entries with the index value ranging from 0 to 40(d). Changing the index by 1 will not necessarily result in a 1dB change to the gain. For example, if the LNA index is changed by 1, the LNA gain can change by 9 or more dB. Without the LPF gain (in 1dB steps) to make up the difference, the LMT gain will change by 9dB. As of this edition of the document, the same split table is used across the entire usable range of the AD9361. This is because for split tables, the requirement of 1dB gain steps is no longer required and the minor differences in gain change from one index to another across frequency do lead to AGC or manual gain control issues.

As mentioned in the Writing to and Reading From the Gain Table section, the BBP only programs the values in columns , “ 0x131 ” “ 0x132 ” 0x133 ” into the AD9361. The other columns allow the table to be easily analyzed.

This table is not loaded into the AD9361 by default so the BBP must load the proper table into the AD9361 in the field as part of initialization.

*As mentioned in the Writing to and Reading From the Gain Table section, when writing a split table, only the LNA, Mixer, and TIA gains are written. LPF gain is not written since LPF gain is always equal to the LPF index. And, when using a split table, LPF gain is separately controlled by its own index pointer. Thus, the “ Total Gain ” column in the table below is correct but it necessa LPF gain is zero. In real operation, LMT and LPF gain pointers will be operated independently and the actual AD9361 gain will be the sum of the Total Gain column below (for LMT gain) and the LPF index.

Table Index	eLNA Index	eLNA Gain	iLNA Index	iLNA Gain	Mixer Index	Mixer Gain	0x131	TIA Index	TIA Gain	LPF Index	0x132	DC Cal	Digital Index	0x133	Total Gain*
0	0	0	0	5	0	0	0	0	6	0	0	1	0	20	-1
1	0	0	0	5	1	3	1	0	6	0	0	1	0	20	2
2	0	0	0	5	2	9	2	0	6	0	0	1	0	20	8
3	0	0	0	5	3	10	3	0	6	0	0	1	0	20	9
4	0	0	0	5	4	14	4	0	6	0	0	1	0	20	13
5	0	0	0	5	5	15	5	0	6	0	0	1	0	20	14
6	0	0	0	5	6	16	6	0	6	0	0	1	0	20	15
7	0	0	0	5	7	17	7	0	6	0	0	1	0	20	16
8	0	0	0	5	8	18	8	0	6	0	0	1	0	20	17
9	0	0	0	5	9	19	9	0	6	0	0	1	0	20	18
10	0	0	0	5	10	20	A	0	6	0	0	1	0	20	19
11	0	0	0	5	11	21	B	0	6	0	0	1	0	20	20
12	0	0	0	5	12	22	C	0	6	0	0	1	0	20	21
13	0	0	0	5	13	23	D	0	6	0	0	1	0	20	22
14	0	0	1	17	3	10	23	0	6	0	0	1	0	20	21
15	0	0	1	17	4	14	24	0	6	0	0	1	0	20	25
16	0	0	2	19	3	10	43	0	6	0	0	1	0	20	23
17	0	0	2	19	4	14	44	0	6	0	0	1	0	20	27
18	0	0	2	19	5	15	45	0	6	0	0	1	0	20	28
19	0	0	2	19	6	16	46	0	6	0	0	1	0	20	29
20	0	0	2	19	7	17	47	0	6	0	0	1	0	20	30
21	0	0	2	19	8	18	48	0	6	0	0	1	0	20	31
22	0	0	2	19	3	10	43	1	0	0	20	1	0	20	29

23	0	0	2	19	4	14	44	1	0	0	20	1	0	20	33
24	0	0	2	19	5	15	45	1	0	0	20	1	0	20	34
25	0	0	2	19	6	16	46	1	0	0	20	1	0	20	35
26	0	0	2	19	7	17	47	1	0	0	20	1	0	20	36
27	0	0	2	19	8	18	48	1	0	0	20	1	0	20	37
28	0	0	3	24	3	10	63	1	0	0	20	1	0	20	34
29	0	0	3	24	4	14	64	1	0	0	20	1	0	20	38
30	0	0	3	24	5	15	65	1	0	0	20	1	0	20	39
31	0	0	3	24	6	16	66	1	0	0	20	1	0	20	40
32	0	0	3	24	7	17	67	1	0	0	20	1	0	20	41
33	0	0	3	24	8	18	68	1	0	0	20	1	0	20	42
34	0	0	3	24	9	19	69	1	0	0	20	1	0	20	43
35	0	0	3	24	10	20	6A	1	0	0	20	1	0	20	44
36	0	0	3	24	11	21	6B	1	0	0	20	1	0	20	45
37	0	0	3	24	12	22	6C	1	0	0	20	1	0	20	46
38	0	0	3	24	13	23	6D	1	0	0	20	1	0	20	47
39	0	0	3	24	14	24	6E	1	0	0	20	1	0	20	48
40	0	0	3	24	15	25	6F	1	0	0	20	1	0	20	49

Table 32.Split Gain Table

APPENDIX 3--NOISE FIGURE (NF) VS. GAIN INDEX PLOTS

The following plots show NF vs. gain index for various configurations of table type (split or full) and LO frequency. The NF values are for the transceiver only. Balun, connector, and trace losses have been de-embedded. Note that a real system will have these losses as well as other such as switch, SAW, etc., losses so a "system" NF will naturally be higher than the transceiver itself. Losses due to non-optimiz matching will degrade affect NF as well so it is important to match all RF system impedances as closely as possible for minimum NF.

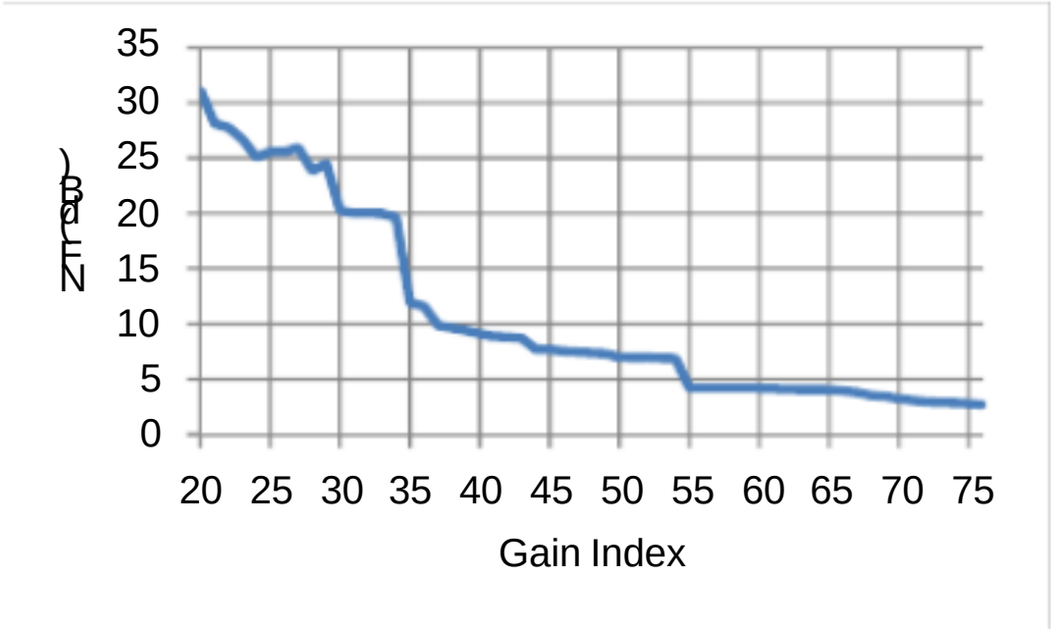

Figure 13.NF vs. Gain Index for Full Table at Rx LO = 920 MHz

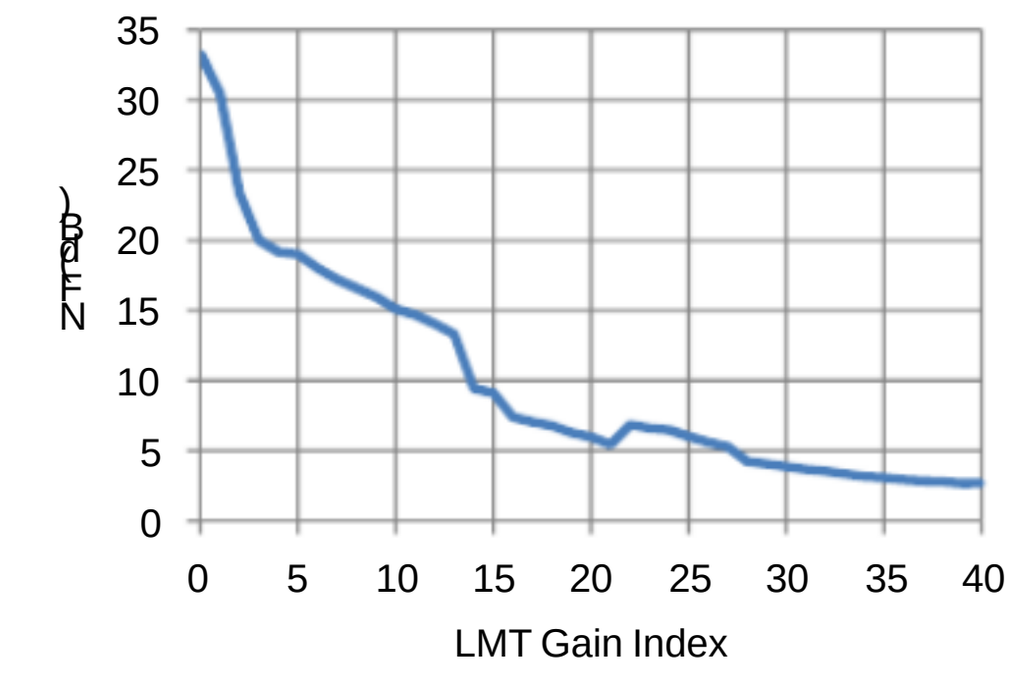

Figure 14. NF vs. LMT Gain Index for Split Table

at Rx LO = 920 MHz

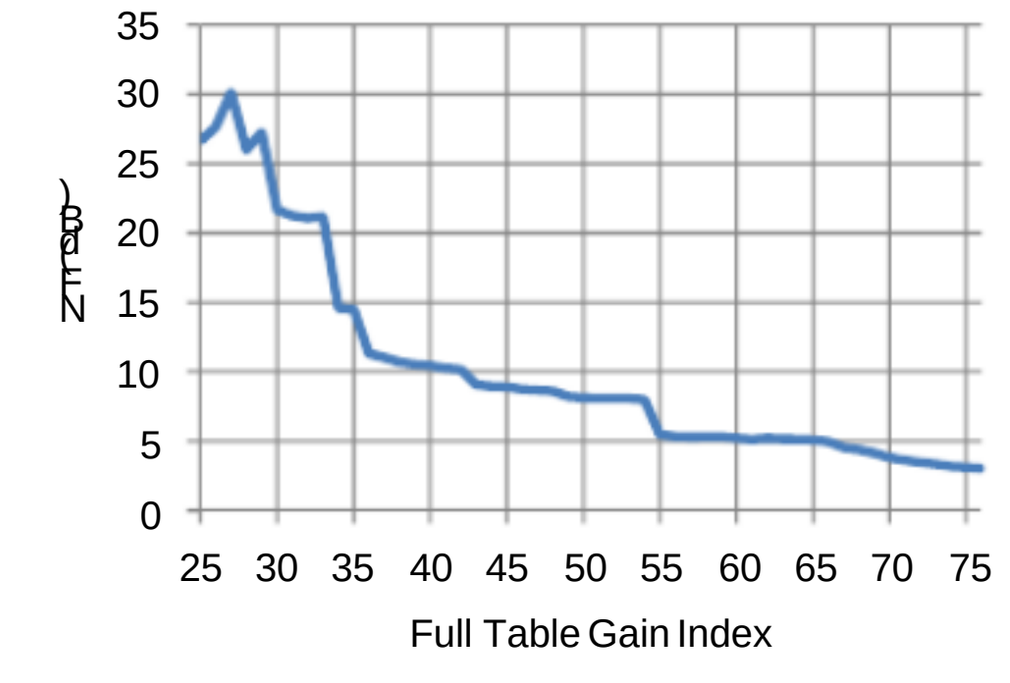

Figure 15.NF vs. Gain Index for Full Table at Rx LO = 2120 MHz

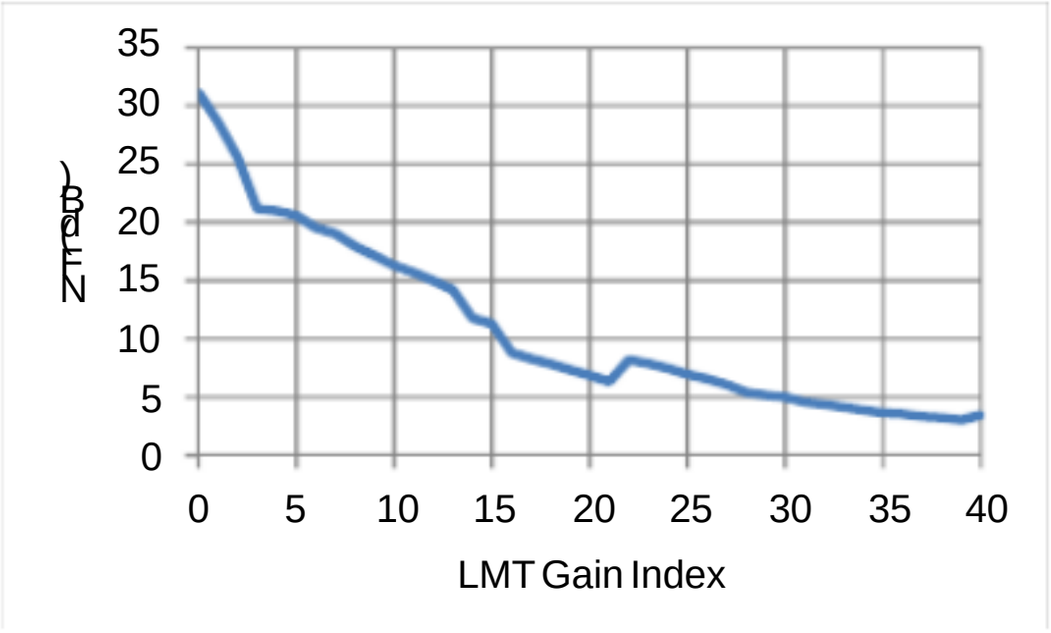

Figure 16. NF vs. LMT Gain Index for Split Table

at Rx LO = 2120 MHz

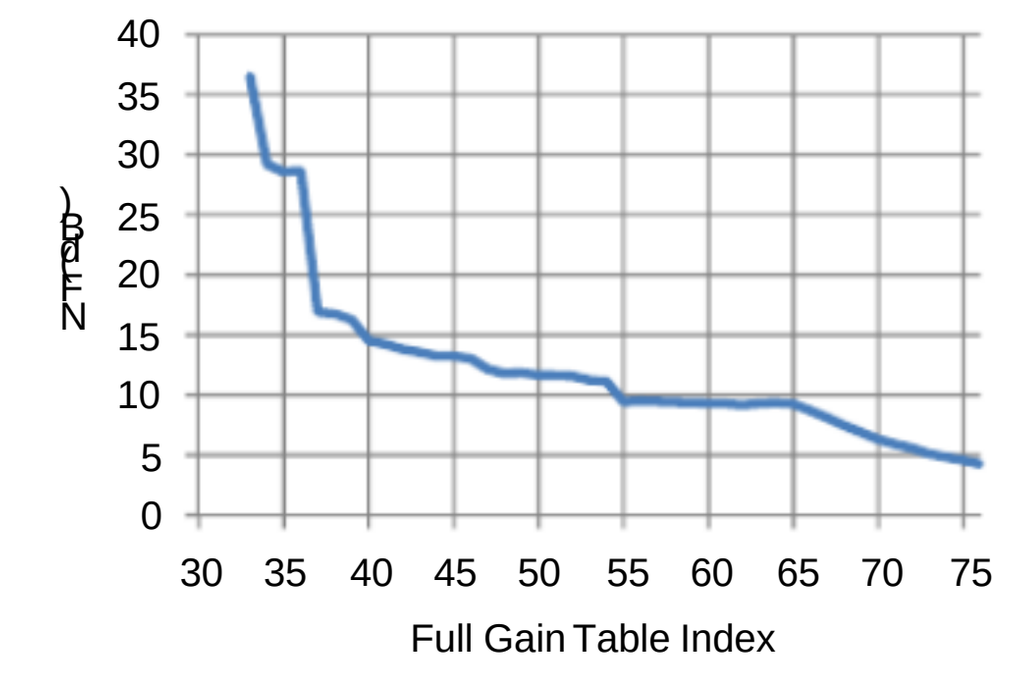

Figure 17. NF vs. Gain Table Index for Full Table

at Rx LO = 4920 MHz

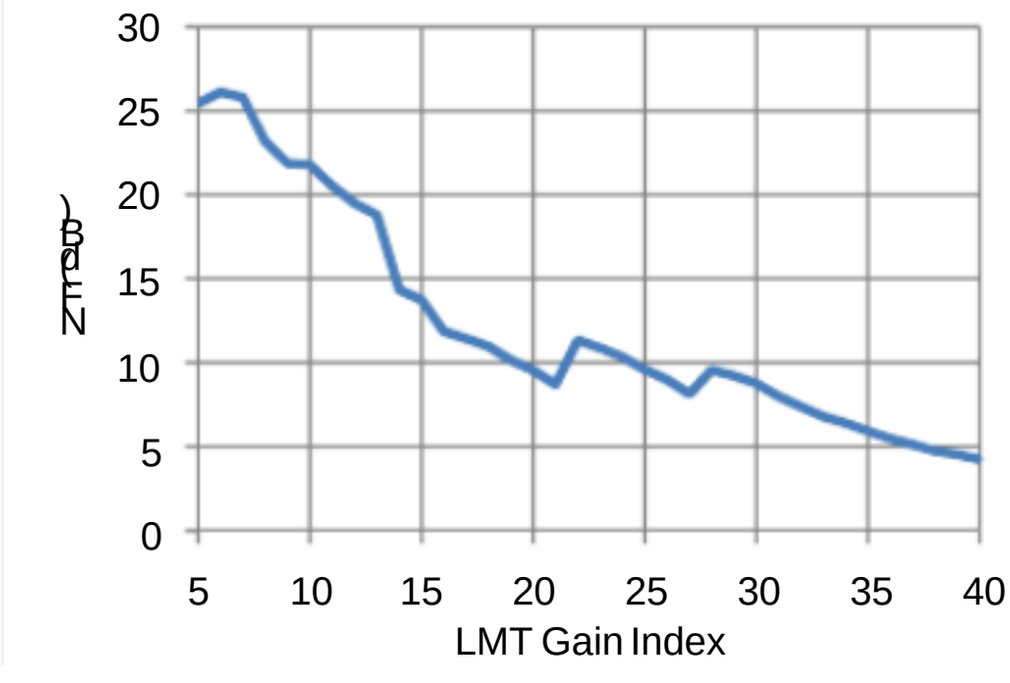

Figure 18.NF vs. LMT Gain Index for Split Table

at Rx LO = 4920 MHz