Peak Cancellation Crest Factor Reduction v7.2

PB008 (v7.2) October 27, 2022 LogiCORE IP Product Brief

Introduction

The Xilinx® LogiCORE™ IP peak cancellation crest factor reduction (PC-CFR) core is used to limit the dynamic range of the signals being transmitted in wireless communications and other applications. It is an efficient, flexible, and easy-to-use implementation that supports Virtex® UltraScale™, Kintex® UltraScale, Virtex-7, Kintex-7, Artix®-7, and Zynq® UltraScale+™ devices (Zynq SoC, MPSoC, and RFSoC). On a Zynq UltraScale+™ RFSoC DFE device, PC-CFR allows for selection of PL-only option or use of DFE-CFR Primitive along with PL resources.

Additional Documentation

A product guide is available for this core. To request access to this material, click this registration link: www.xilinx.com/member/forms/registration/pc_cfr_eval.html.

Features

The common features of the PC-CFR core and individual configuration features of both implementations of PC-CFR (using PL resources only and using DFE-CFR + PL resources) are as follows:

- Support for multiple air interface standards.
- Smart Peak Processing mode for supporting wide transmit bandwidth up to 400 MHz, processes incoming samples at >1.2 times instantaneous bandwidth (iBW) reducing resource utilization.
- Support for power and frequency dynamics.

For additional features see Features (cont.).

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family[1]	Zynq® UltraScale+™ RFSoC DFE UltraScale+™ Families UltraScale™ Architecture Zynq® UltraScale+ Devices 7 series FPGAs
Supported User Interfaces	AXI4-Stream, AXI4-Lite
Provided with Core	
Design Files	Encrypted RTL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Vivado XDC
Simulation Model	VHDL and Verilog Structural Simulation Model MATLAB® Model available
Supported S/W Driver	CFR Reference Design available at www.xilinx.com/products/intellectual-property/ef-di-pc-cfr.html
Tested Design Flows[2]	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
Release Notes and Known Issues	Master Answer Record: 54486
All Vivado IP Change Logs	Master Vivado IP Change Logs: 72775
Xilinx Support web page	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Features (cont.)

- Support for dynamic computation of cancellation pulse (CP).
- Meets performance requirements (EVM, PAPR, and ACLR) of all air interfaces.
- A maximum of five different RATs are supported. The total number of carriers using all RATs is 30. LTE 5 MHz and LTE 10 MHz are considered as different RATs because the corresponding base pulses are different.
- Support for data-path delay matched TUSER forwarding feature.
- Support for cancellation pulse read back in static mode and base pulse read back in dynamic mode.
- Support for read back of CFR configuration and statistics registers.

IMPORTANT: *Core's control interface address format is modified to support 8 MB of space. When upgrading from older core versions, you should adopt the new control interface address map mentioned in PC-CFR LogiCORE IP Product Guide (PG097) (*registration required*).*

PL Resources

When using PL resources only, the selectable configurations are as follows:

- Configurable clock-to-sample ratio of 1, 2, 3, and 4.
- Support for Smart Peak Processing.
- Support for 1 to 8 PC-CFR iterations.
- Configurable number of cancellation pulse generators (CPGs) of 1 to 12 per iteration.
- Support for 1, 2, 4, 8, and 16 antennas.
- Quantization support for 16 bits.
- Support for single or two pulse(s) of configurable coefficients with real or complex coefficients storage.
- Supports a standalone hard clipper.
- User selectable signal-agnostic window crest factor reduction (WCFR) available as a standalone or a post processing stage.
- Supports super sampling rate (SSR) WCFR standalone mode with poly-phase capability up to two phases (NUM_PHASES=2).

DFE-CFR Primitive

For Zynq UltraScale+ RFSoC DFE when leveraging DFE-CFR Primitive, the selectable configurations are as follows:

- Support for clock-to-sample ratio of 1.
- PC-CFR stages with Smart Peak Processing enabled.
- Support for 1, 2, 4, and 8 antennas.
- Post Processing stage fixed to WCFR.

Overview

Crest factor reduction (CFR) is used to limit the dynamic range of the signals being transmitted in wireless communications and other applications. Multi-user and multi-carrier signals often have a high peak-to-average ratio (PAR). This places high demands on the data converters and especially limits the efficiency of operation of the power amplifiers (PAs) used in cellular base stations. Reducing the PAR is therefore beneficial in increasing PA efficiency by allowing higher average power to be transmitted before saturation occurs.

In a modern transmit chain, CFR is often incorporated with digital pre-distortion (DPD), which acts to linearize the PA, allowing operation at maximum efficiency with spectral compliance. CFR complements DPD because it levels the signal peaks, making accurate correction estimation easier.

The Xilinx PC-CFR core is an efficient, flexible, and easy-to-use implementation that supports Virtex UltraScale, Kintex UltraScale, Virtex-7, Kintex-7, Artix-7, and Zynq UltraScale+ devices (Zynq SoC, MPSoC, and RFSoC). On a Zynq UltraScale+ RFSoC DFE device, the PC-CFR allows for selection of the PL-only option or use of the DFE-CFR Primitive along with PL resources. It is configurable both in function, supporting all major cellular wireless air interfaces, and in use, supporting many clocking and resource requirements. It can also handle dynamic power and frequency variations in the incoming data by computing the cancellation pulse coefficients dynamically.

General Description

The PC-CFR core processes control and data through industry-standard AXI4 interfaces that allow immediate logic-free connection to other Xilinx IP components and to any general environment. The control interface is AXI4-Lite compliant and the data interface is AXI4-Stream compliant. The control interface provides access to a set of configuration registers and a pulse coefficient RAM and the data interface is used for streaming data in/out of the core. The data flow is unidirectional with no rate or bit-width change. A typical CFR application consists of multiple iterations and multiple antennas that can be configured through the Vivado Integrated Design Environment (IDE).

The core is configured for a particular application through the control interface. In particular, the contents of the pulse coefficient RAM are related to the spectrum of the signal being transmitted.

The *PC-CFR LogiCORE IP Product Guide* (PG097) documents how to produce these coefficients, and specific details are provided for the WCDMA, CDMA2000, WiMAX, TD-SCDMA, GSM, LTE, and 5G-NR air interfaces. Mixed-mode signal operation is also supported. Pulse coefficients can be pre-configured at generation time through a `.coe` file or configured in operation through the control interface. There is also provision for a shadow bank of coefficients to be loaded, and then activated with a select signal, to cater to applications where fast dynamic switching is required. Functions that can be run with MATLAB® are supplied for simulation and design of the cancellation pulse.

The core can be configured for clock-to-sample ratios of 1, 2, 3, and 4 and for algorithmic complexity, allowing FPGA resources to be minimized for a given application. The algorithmic complexity is the number of hardware resources available to cancel the signal peaks. These are called cancellation pulse generators (CPGs).

IMPORTANT: *All the Clock-to-Sample Ratio related statements are applicable to PL-only IP. In case of CFR IP using DFE-CFR Primitive, all the CPGs are implemented inside the DFE CFR Primitive.*

Resource Requirements and Performance

The latest resource utilization and maximum clock frequency tables for various core configurations can be downloaded from PC-CFR evaluation lounge (registration required):

www.xilinx.com/member/forms/registration/pc_cfr_eval.html

Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for information about pricing and availability.

For more information, visit the PC-CFR product web page.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Evaluation

An evaluation license is available for this core. The evaluation version operates in the same way as the full version for several hours, dependent on clock frequency. Allocation of the cancellation pulse generators is then completely disabled, and the data output comprises a delayed version of the data input. If you notice this behavior in hardware, it probably means you are using an evaluation version of the core. The Xilinx tools warn that an evaluation license is being used during netlist implementation. If a full license is installed, delete the old XCO file, reconfigure and regenerate the core. More details on evaluation can be found in the PC-CFR evaluation lounge (registration required): www.xilinx.com/member/forms/registration/pc_cfr_eval.html.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
10/27/2022	7.2	Deprecated the support for datawidth of 18-bit
04/20/2022	7.1	Added support for super sampling rate WCFR standalone mode.
10/22/2021	7.0	• Core's control interface address format is modified to support 8MB of space. • Added support for Zynq UltraScale+ RFSoC DFE devices to use DFE-CFR Primitives. • Updated Features section. • Deprecated use of Data Rate = 8 when using PL CFR.
01/08/2021	6.4	Extended the LUT optimization features available for CPS=2 in PC-CFR v6.3 to *all* CPS cases. These optimizations must be seen in all smart peak processing cases.
05/22/2019	6.3	Enabled LUT optimization for SPP and Data Rate (clock-cycles/samples) = 2 scenarios at the cost of 3 DSP48s increase per iteration.
12/05/2018	6.2	Updated the Features section with a description of Dynamic mode.

Date	Version	Description of Revisions
06/20/2018	6.2	• Added 16 antenna support. • DSP48 optimization in CPGs. • Core is fully supported in Vivado 2018.2.
10/05/2016	6.1	• Added support to work as Stand-alone Hard Clipper. • Added optional feature to operate WCFR without smart peak processing. • Added TUSER forwarding feature. • Added Support for two more RATs (RATD and RATE) in dynamic CP computation mode.
11/18/2015	6.0	Added support for UltraScale+ families.
04/01/2015	6.0	Production release of PC-CFR v6.0 core.
10/01/2014	6.0	• Version 6.0 is Early Access, Lounge delivered to customers. • Added UltraScale Architecture support. • Updated Features. • Removed resource table and replaced with link to product page.
12/18/2013	5.0	• Revision number advanced to 5.0 to align with core version number. • Added dynamic support (dynamic power variation and frequency hopping) • Hard clipper support • Change in tool settings for characterization • New TUSER port added in Dynamic mode
03/20/2013	3.0	PC-CFR v4.0 is available only with Vivado; other changes are • Improved f_{max}, core can be clocked at 491.52 MHz for -2 devices • Core latency has changed
12/18/2012	2.0	Updated for 2012.4/14.4. • Real/Complex CP selection added • Number of CPGs/iteration increased to 12 • Core is fully supported in Vivado 2012.4 • Peak detect window is used in place of allocator spacing
06/22/2011	1.0	Initial Xilinx release. Previous version of this Product Brief is XMP039.

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